Petra
UMA Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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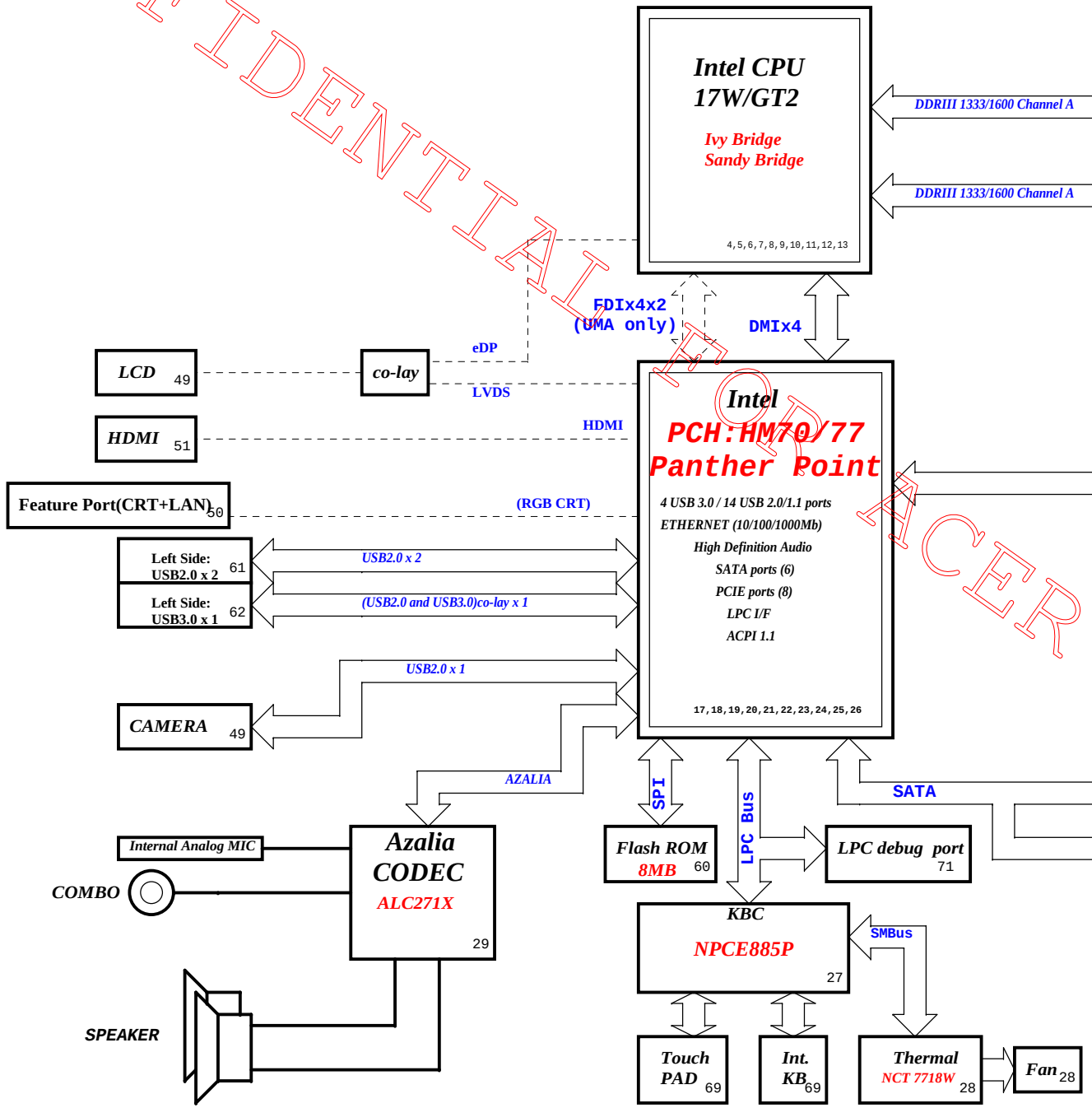
Date: Wednesday, February 22, 2012	Sheet 1 of 103	

Project code : 91.4VM01.001
PCB P/N : 48.4VM02.001
PCB No. : 11324
Revision : -1



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Monday, January 07, 2013 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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Title: Table of Content

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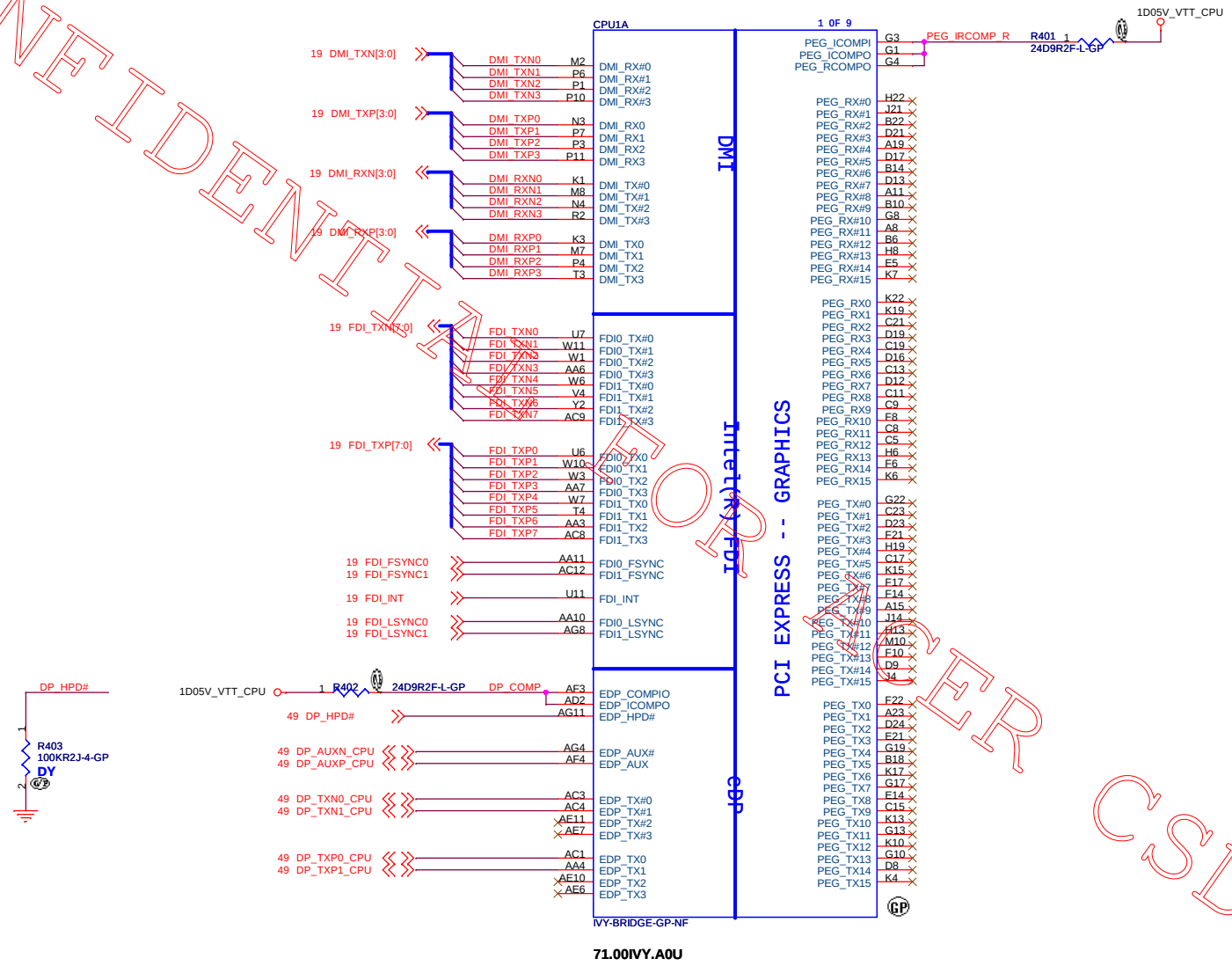
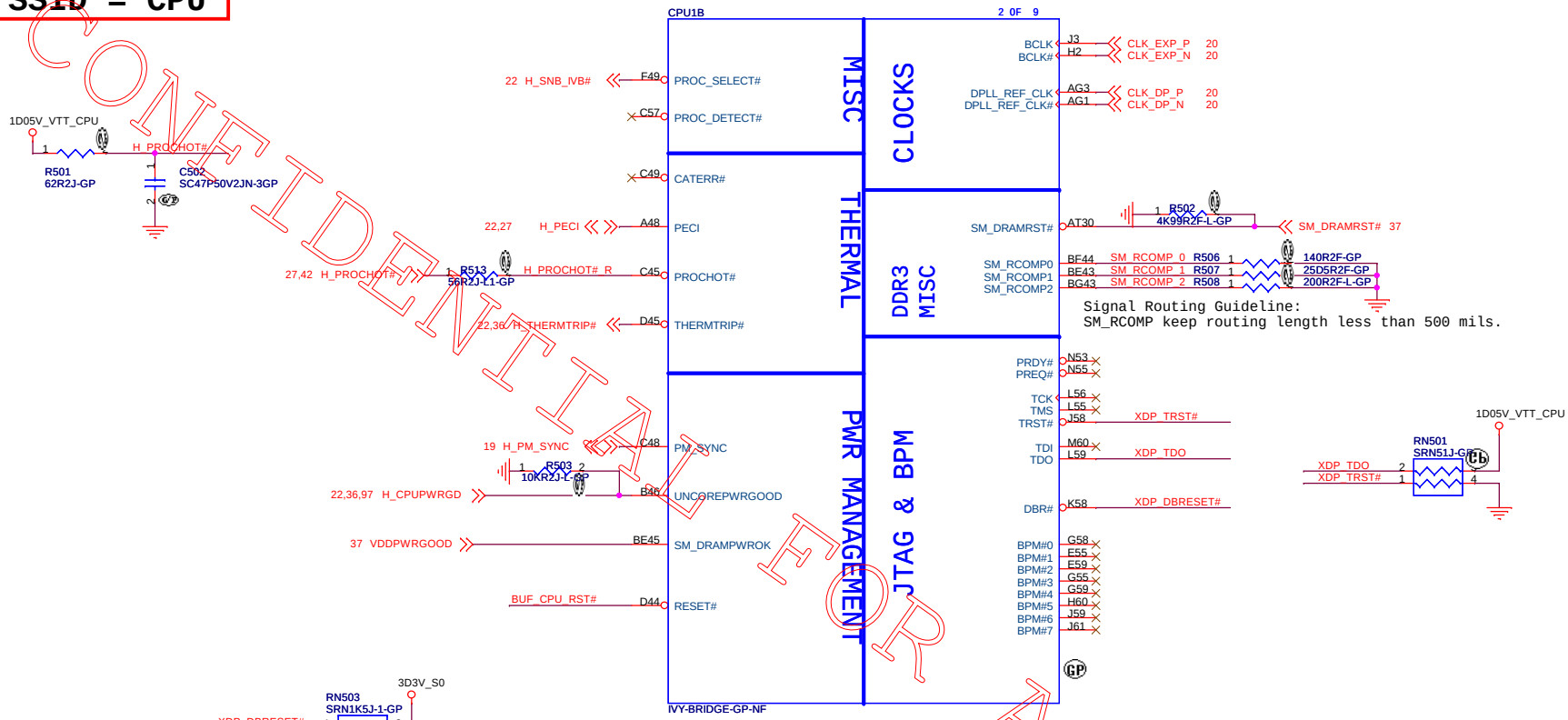
Date: Wednesday, February 22, 2012 | Sheet 3 of 103

SSID = CPU



Core Design	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (PCIE/DMI/FDI)
Size: A3	Document Number: Petra Uma
Rev	-1
Date: Tuesday, July 10, 2012	Sheet 4 of 103

SSID = CPU



<Core Design>

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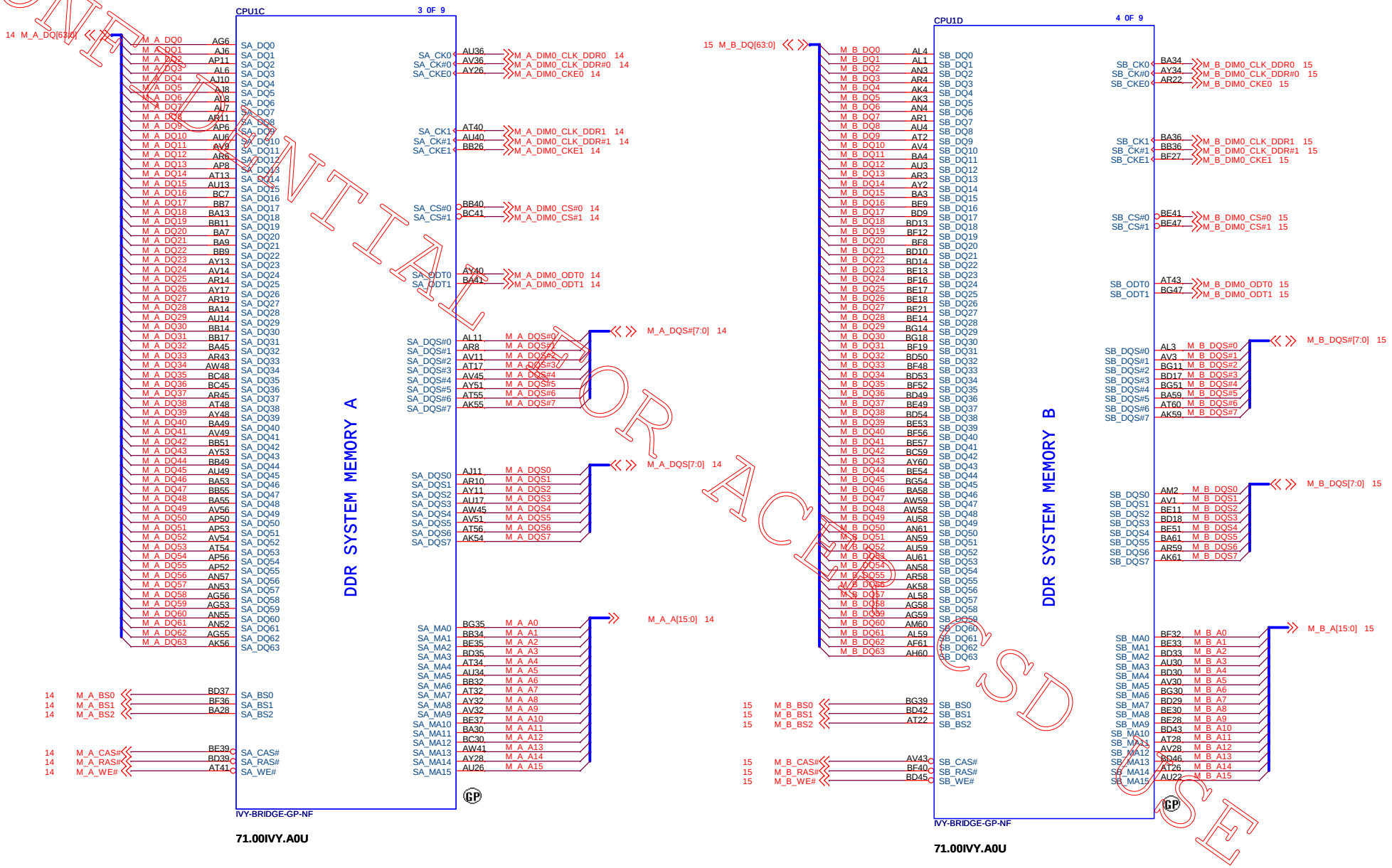
Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 5 of 103

SSID = CPU



<Core Design>

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Title: CPU (DDR)

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 6 of 103

SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG2
R702 1KR2J-L2-GP
DY

Enabl EDP function	
CFG4	1:Disable 0:Enable

CFG4
R703 1KR2J-L2-GP
EDP

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5
R704 1KR2J-L2-GP
DY

CFG6
R705 1KR2J-L2-GP
DY

CFG7
R706 1KR2J-L2-GP
DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

TPAD14-OP-GP TP701
TPAD14-OP-GP TP702
TPAD14-OP-GP TP703

CFG0_TP
CFG1_TP
CFG2
CFG3_TP
CFG4
CFG5
CFG6
CFG7

CPU1E
5 OF 9

B50	CFG0		BCLK_ITP	N59	
C51	CFG1		BCLK_ITP#	N58	
B54	CFG2				
D53	CFG3				
A51	CFG4		RSVD30	N42	
C53	CFG5		RSVD31	L42	
C55	CFG6		RSVD32	L45	
H49	CFG7		RSVD33	L47	
A55	CFG8				
H51	CFG9				
K49	CFG10		RSVD34	M13	
K53	CFG11		RSVD35	M14	
F53	CFG12		RSVD36	U14	
G53	CFG13		RSVD37	W14	
L51	CFG14		RSVD38	P13	
E51	CFG15				
D52	CFG16				
L53	CFG17		RSVD39	AT49	
			RSVD40	K24	
H43	VCC_VAL_SENSE				
K43	VSS_VAL_SENSE		RSVD41	AH2	
			RSVD42	AG13	
			RSVD43	AM14	
H45	VAXG_VAL_SENSE		RSVD44	AM15	
K45	VSSAXG_VAL_SENSE				
			RSVD45	N50	
F48	VCC_DIE_SENSE				
G48	RSVD47				
H48	RSVD6				
K48	RSVD7				
			DC_TEST_A4	A4	
			DC_TEST_C4	C4	
BA19	RSVD8		DC_TEST_D3	D3	
AV19	RSVD9		DC_TEST_D1	D1	
AT21	RSVD10		DC_TEST_A58	A58	
BB21	RSVD11		DC_TEST_A59	A59	
BB19	RSVD12		DC_TEST_C59	C59	
AY21	RSVD13		DC_TEST_A61	A61	
BA22	RSVD14		DC_TEST_C61	C61	
AY22	RSVD15		DC_TEST_D61	D61	
AU19	RSVD16		DC_TEST_BD61	BD61	
AU21	RSVD17		DC_TEST_BE61	BE61	
BD21	RSVD18		DC_TEST_BE59	BE59	
BD27	RSVD19		DC_TEST_BG61	BG61	
BD25	RSVD20		DC_TEST_BG59	BG59	
BD26	RSVD21		DC_TEST_BG58	BG58	
BG22	RSVD22		DC_TEST_BG4	BG4	
BE22	RSVD23		DC_TEST_BG3	BG3	
BG26	RSVD24		DC_TEST_BE3	BE3	
BE26	RSVD25		DC_TEST_BG1	BG1	
BF23	RSVD26		DC_TEST_BE1	BE1	
BE24	RSVD27		DC_TEST_BD1	BD1	

RESERVED

GP

IVY-BRIDGE-GP-NF

71.00IVY.A0U

<Core Design>

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Title: CPU (RESERVED)

Size: A3 | Document Number | Rev: -1

Date: Wednesday, February 29, 2012 | Sheet 7 of 103

Petra Uma

SSID = CPU

POWER

6 OF 9

CPU1F

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U

Place near processor

Place near processor

<Core Design>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 8 of 103

SSID = CPU

POWER

CPU1G 7 OF 9

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

BE7 and BG7 is NC ball in HR

Iccmax:5A

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

R906,R907 close to CPU

ICC_MAX:1.2A

ICC_MAX:6A

R902 need be close to pin U10.

VCCSA Voltage Select		
VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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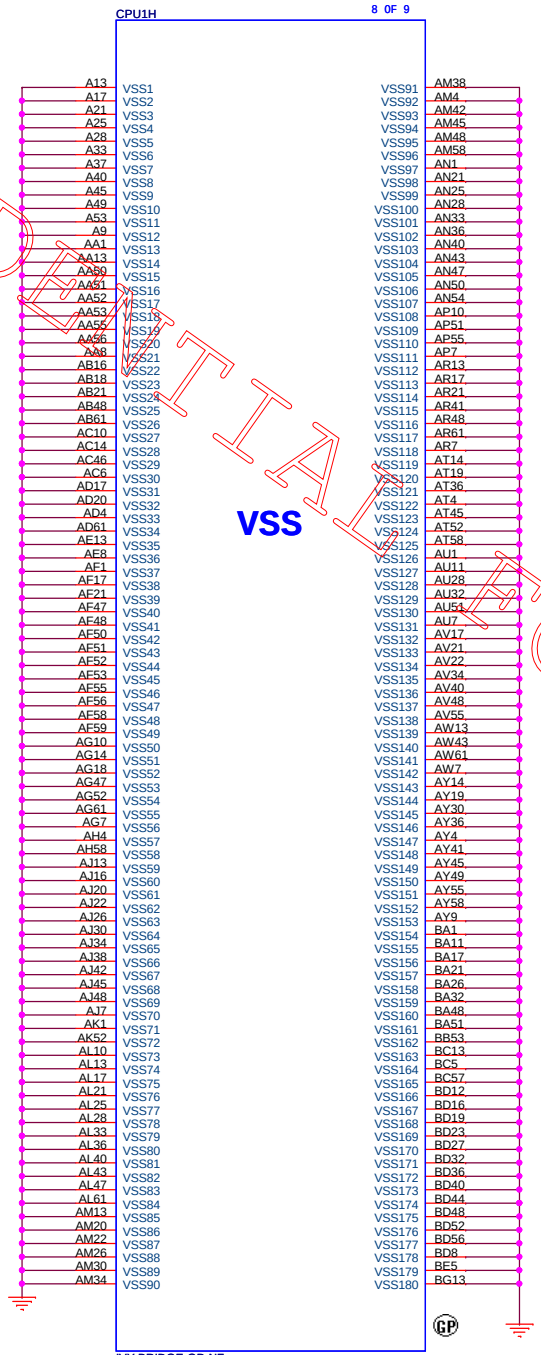
Title: CPU (VCC_GFXCORE)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 9 of 103

SSID = CPU



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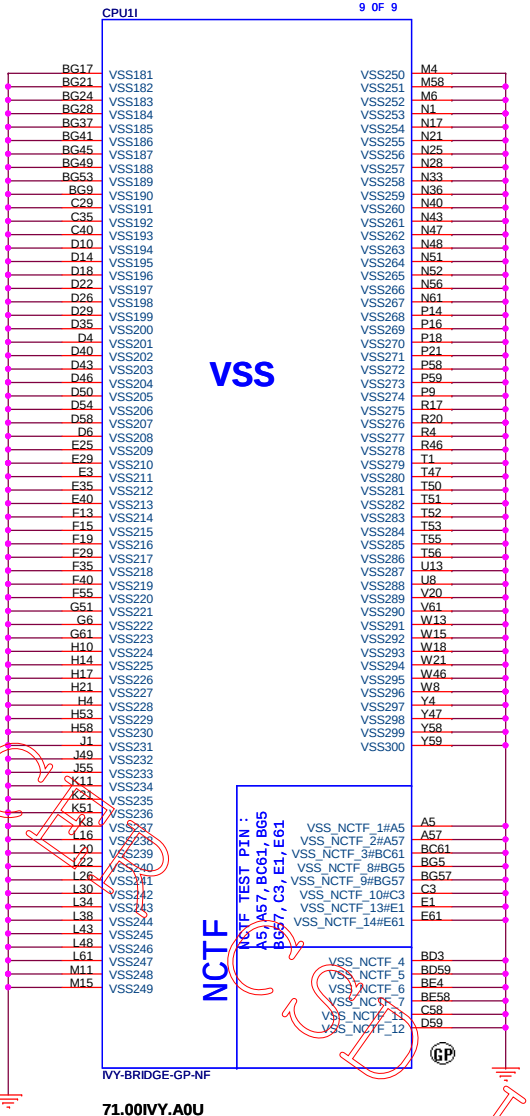

71.00IVY.A0U

<Core Design>

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Title: CPU (VSS)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 10 of 103

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<Core Design>

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Title: XDP

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 11 of 103

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<Core Design>

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Title: ***Reserved***

Size: A4 | Document Number: **Petra Uma** | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 12 of 103

(Blanking)

<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
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Date: Wednesday, February 22, 2012 Sheet 13 of 103

SSID = MEMORY

M_A_A[15:0] 6

M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6

DDR_VREF_S3
M_VREF_DQ_DIMM0

DDR3_DRAMRST# 15,37

0D75V_S0

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
	79	A16/BA2	
	109	BA0	
	108	BA1	
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
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M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
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M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
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M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
	116	ODT0	
	120	ODT1	
DDR_VREF_S3	126	VREF_CA	
M_VREF_DQ_DIMM0	1	VREF_DQ	
	30	RESET#	
0D75V_S0	203	VTT1	
	204	VTT2	

NP1	NP1	NP1	
NP2	NP2	NP2	
RAS#	110	M_A_RAS# 6	
WE#	113	M_A_WE# 6	
CAS#	115	M_A_CAS# 6	
CS0#	114	M_A_DIM0_CS#0 6	
CS1#	121	M_A_DIM0_CS#1 6	
CKE0	73	M_A_DIM0_CKE0 6	
CKE1	74	M_A_DIM0_CKE1 6	
CK0	101	M_A_DIM0_CLK_DDR0 6	
CK0#	103	M_A_DIM0_CLK_DDR#0 6	
CK1	102	M_A_DIM0_CLK_DDR1 6	
CK1#	104	M_A_DIM0_CLK_DDR#1 6	
DM0	11		
DM1	28		
DM2	46		
DM3	63		
DM4	136		
DM5	153		
DM6	170		
DM7	187		
SDA	200	PCH_SMBDATA 15,20,69	
SCL	202	PCH_SMBCLK 15,20,69	
EVENT#	198	TS#_DIMM0_1 15	
VDDSPD	199	3D3V_S0	
SA0	197		
SA1	201		
NC#1	77		
NC#2	122		
NC#/TEST	125	1D5V_S3	
	75	VDD1	
	76	VDD2	
	81	VDD3	
	82	VDD4	
	87	VDD5	
	88	VDD6	
	93	VDD7	
	94	VDD8	
	99	VDD9	
	100	VDD10	
	105	VDD11	
	106	VDD12	
	111	VDD13	
	112	VDD14	
	117	VDD15	
	118	VDD16	
	123	VDD17	
	124	VDD18	
	2	VSS	
	3	VSS	
	8	VSS	
	9	VSS	
	13	VSS	
	14	VSS	
	19	VSS	
	20	VSS	
	25	VSS	
	26	VSS	
	31	VSS	
	32	VSS	
	37	VSS	
	38	VSS	
	43	VSS	
	44	VSS	
	48	VSS	
	49	VSS	
	54	VSS	
	55	VSS	
	60	VSS	
	61	VSS	
	65	VSS	
	66	VSS	
	71	VSS	
	72	VSS	
	127	VSS	
	128	VSS	
	133	VSS	
	134	VSS	
	138	VSS	
	139	VSS	
	144	VSS	
	145	VSS	
	150	VSS	
	151	VSS	
	155	VSS	
	156	VSS	
	161	VSS	
	162	VSS	
	167	VSS	
	168	VSS	
	172	VSS	
	173	VSS	
	178	VSS	
	179	VSS	
	184	VSS	
	185	VSS	
	189	VSS	
	190	VSS	
	195	VSS	
	196	VSS	
	205	VSS	
	206	VSS	

DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.M51
3rd = 62.10024.G21

Thermal EVENT

TS#_DIMM0_1 — R1403 10KR2J-L-GP — 3D3V_S0

3D3V_S0
C1401 SCD1U10V2KX-L1-GP

1D5V_S3
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 SC10U10V5ZY-1GP
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP
C1416 SCD1U10V2KX-L1-GP
C1417 SCD1U10V2KX-L1-GP

0D75V_S0
C1419 SC1U6D3V2KX-L1-GP
C1421 SC1U6D3V2KX-L1-GP

DDR_VREF_S3
M_VREF_DQ_DIMM0
R1404 0R3J-4-GP SNB
R1405 0R3J-4-GP IVB
DDR_WR_VREF01_B4 37
C1411 SCD1U10V2KX-L1-GP
C1413 SCD1U10V2KX-L1-GP

Tracew should be at least 20 mils wide

<Core Design>

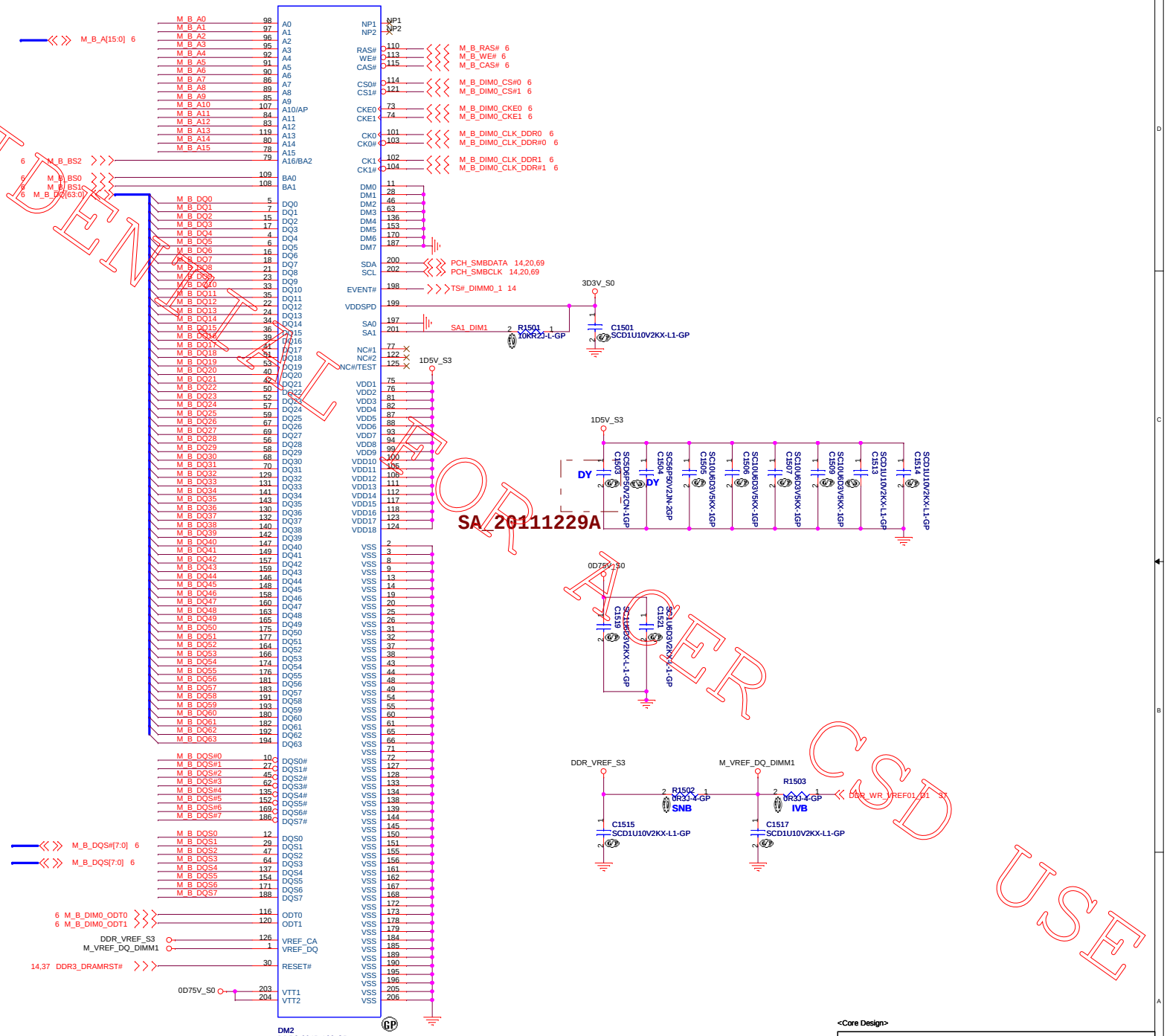
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 14 of 103

SSID = MEMORY



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 15 of 102

(Blanking)

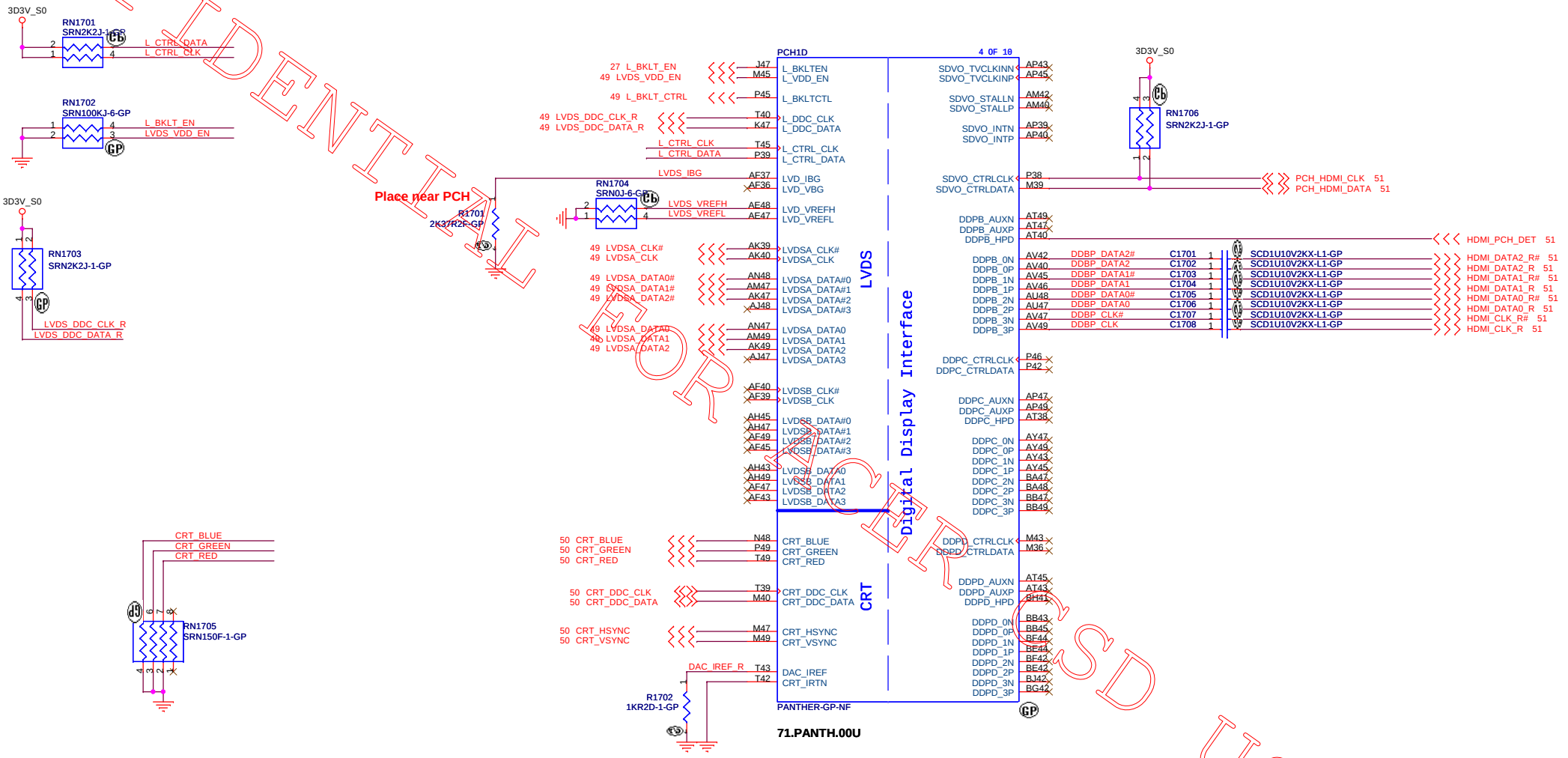
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 16 of 103



<Core Design>

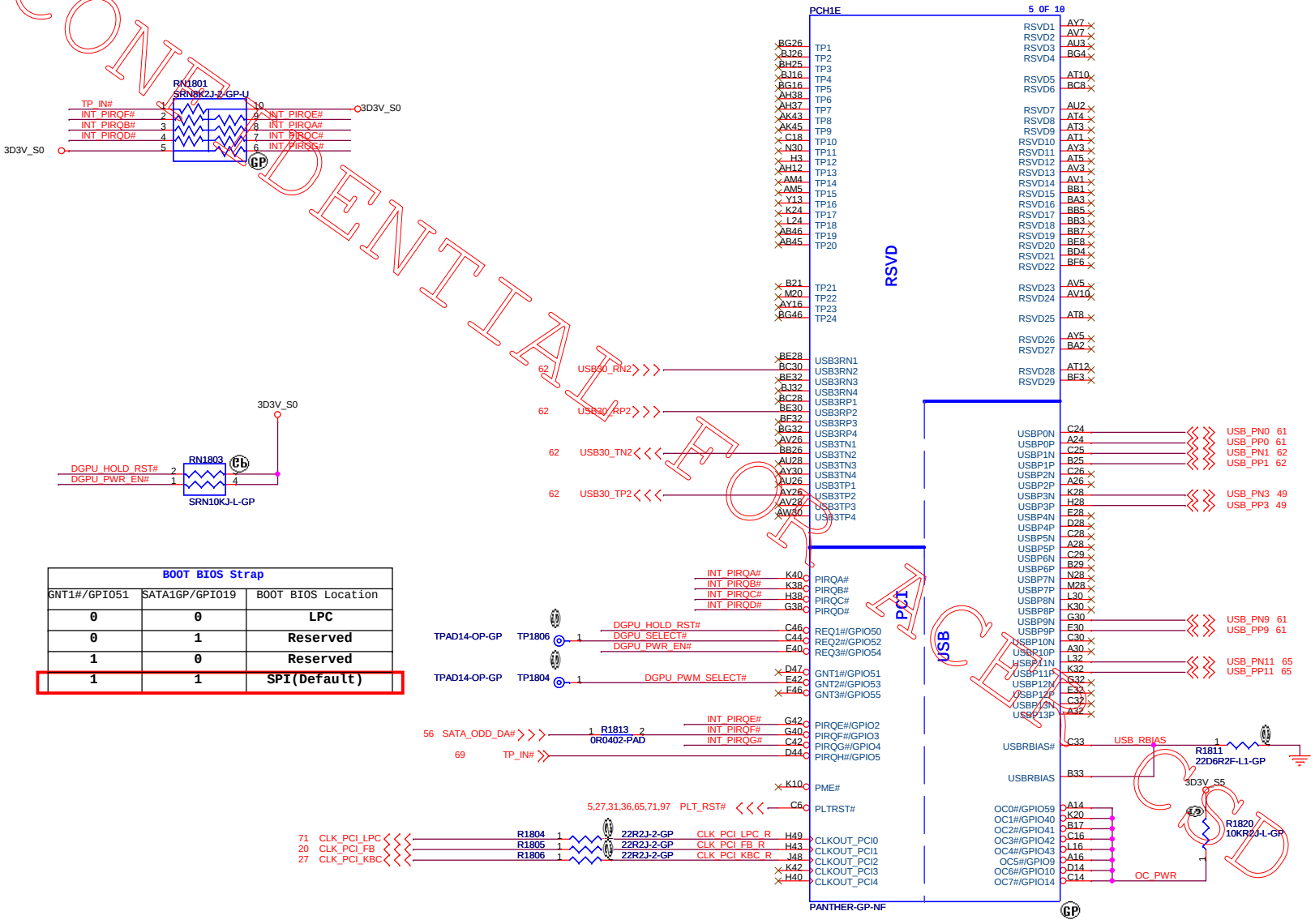
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI_RXN[3:0]
4 DMI_RXP[3:0]
4 DMI_TXN[3:0]
4 DMI_TXP[3:0]

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

PCH1C — 3 OF 10

DMI:
- DMI_RXN0 BC24 DMI0RXN
- DMI_RXN1 BE20 DMI1RXN
- DMI_RXN2 BG18 DMI2RXN
- DMI_RXN3 BG20 DMI3RXN
- DMI_RXP0 BE24 DMI0RXP
- DMI_RXP1 BC20 DMI1RXP
- DMI_RXP2 BJ18 DMI2RXP
- DMI_RXP3 BJ20 DMI3RXP
- DMI_TXN0 AW24 DMI0TXN
- DMI_TXN1 AW20 DMI1TXN
- DMI_TXN2 BB18 DMI2TXN
- DMI_TXN3 AV18 DMI3TXN
- DMI_TXP0 AY24 DMI0TXP
- DMI_TXP1 AY20 DMI1TXP
- DMI_TXP2 AY18 DMI2TXP
- DMI_TXP3 AU18 DMI3TXP

FDI:
- FDI_RXN0 BJ14 → FDI_TXN0 4
- FDI_RXN1 AY14 → FDI_TXN1 4
- FDI_RXN2 BE14 → FDI_TXN2 4
- FDI_RXN3 BH13 → FDI_TXN3 4
- FDI_RXN4 BC12 → FDI_TXN4 4
- FDI_RXN5 BJ12 → FDI_TXN5 4
- FDI_RXN6 BG10 → FDI_TXN6 4
- FDI_RXN7 BG9 → FDI_TXN7 4
- FDI_RXP0 BG14 → FDI_TXP0 4
- FDI_RXP1 BB14 → FDI_TXP1 4
- FDI_RXP2 BF14 → FDI_TXP2 4
- FDI_RXP3 BG13 → FDI_TXP3 4
- FDI_RXP4 BE12 → FDI_TXP4 4
- FDI_RXP5 BG12 → FDI_TXP5 4
- FDI_RXP6 BJ10 → FDI_TXP6 4
- FDI_RXP7 BH9 → FDI_TXP7 4
- FDI_INT AW16 → FDI_INT 4
- FDI_FSYNC0 AV12 → FDI_FSYNC0 4
- FDI_FSYNC1 BC10 → FDI_FSYNC1 4
- FDI_LSYNC0 AV14 → FDI_LSYNC0 4
- FDI_LSYNC1 BB10 → FDI_LSYNC1 4

1D05V_VTT
- R1901 1 49D9R2F-GP DMI_COMP_R → DMI_ZCOMP BJ24
- R1902 1 750R2F-GP RBIAS_CRT → DMI_IRCOMP BG25, DMI2RBIAS BH21

System Power Management

- DSWVRMEN A18 ← DSWODVREN
- DPWROK E22 ← PCH_DPWROK; R1910 0R0402-PAD, R1911 10KR2J-L-GP DY; PM_RSMRST# → RTC_AUX_S5
- WAKE# B9 → PCIE_WAKE#
- CLKRUN#/GPIO32 N3 → PM_CLKRUN# 27
- SUS_STAT#/GPIO61 G8
- SUSCLK/GPIO62 N14 → PCH_SUSCLK_KBC 27
- SLP_S5#/GPIO63 D10
- SLP_S4# H4 → PM_SLP_S4# 27,46
- SLP_S3# F4 → PM_SLP_S3# 27,29,30,37,47
- SLP_A# G10
- SLP_SUS# G16 → SLLP_SUS# TP 1 → TP1904 TPAD14-OP-GP
- PMSYNCH AP14 ← H_PM_SYNC 5
- SLP_LAN#/GPIO29 K14

- SUS_PWR_ACK# → SUSACK# C12
- 3D3V_S0 → R1905 10KR2J-L-GP → SYS_RESET# K3
- 36 SYS_PWROK → SYS_PWROK P12
- DY R1926 10KR2J-L-GP SYS_PWROK
- R1904 100KR2J-4-GP PWROK
- 27 S0_PWR_GOOD → R1924 0R0402-PAD → PWROK L22, APWROK L10
- 37 PM_DRAM_PWRGD → DRAMPWROK B13
- PM_RSMRST# → RSMRST# C21
- SUS_PWR_ACK_R → SUSWARN#/SUSPWRDNACK/GPIO30 K16
- 27,97 PM_PWRBTN# → PWRBTN# E20
- 27 AC_PRESENT → ACPRESENT/GPIO31 H20
- BATLOW# → BATLOW#/GPIO72 E10
- PM_RI# → RI# A10

PANTHER-GP-NF

71.PANTH.00U

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
- R1917 1 330KR2J-L1-GP
- DSWODVREN R1918 1 DY 330KR2J-L1-GP

3D3V_S0
- PM_CLKRUN# 1 R1919 8K2R2J-3-GP

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

3D3V_S5
- RN1901 SRN10KJ-6-GP
  - 8 1 BATLOW#
  - 7 2 PM_RI#
  - 6 3 AC_PRESENT
  - 5 4 SUS_PWR_ACK_R
- R1921 1 10KR2J-L-GP PCIE_WAKE#
- R1922 1 10KR2J-L-GP SUS_PWR_ACK#
- R1908 1 100KR2J-4-GP PM_RSMRST#

3D3V_AUX_S5
- R1909 1 100KR2J-4-GP
- R1916 10KR2J-L-GP
- 3V_5V_POK_# → Q1901 2N7002KDW-GP
- PM_RSMRST# 1 R1912 1KR2J-L2-GP 2 → RSMRST#_KBC 27
- 3V_5V_POK 41

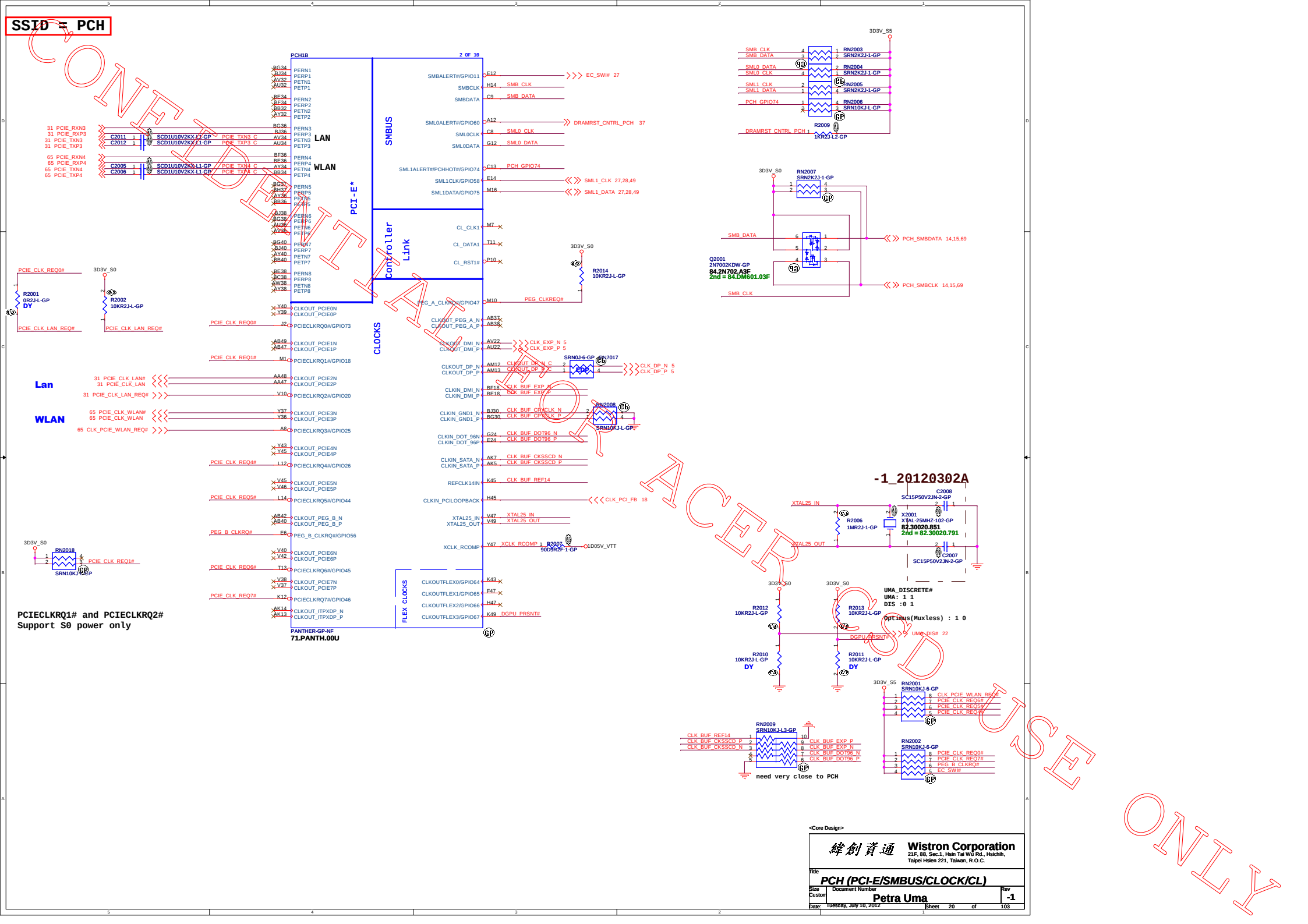
84.2N702.A3F
2nd = 84.DM601.03F

<Core Design>

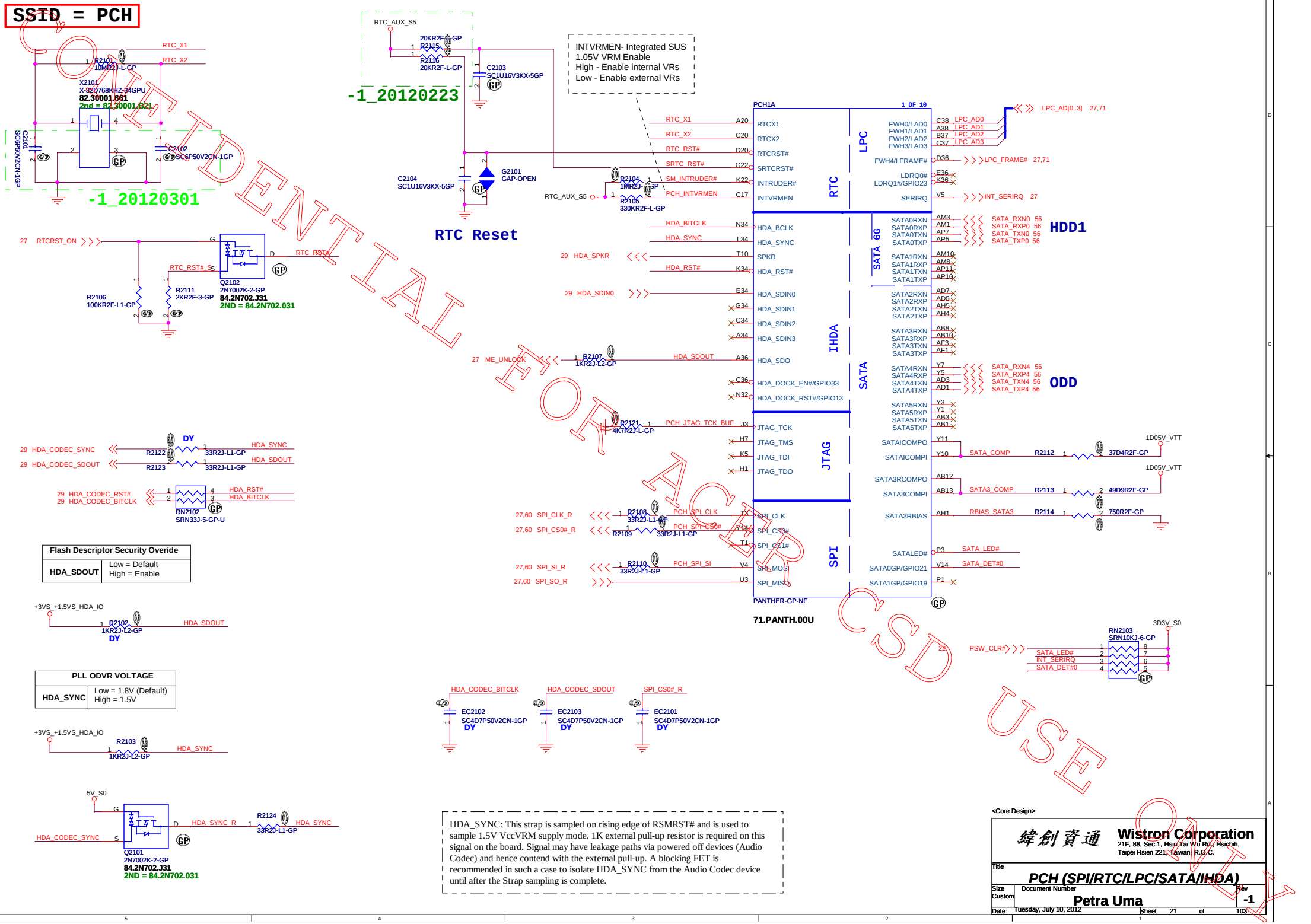
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: Petra Uma | Rev: -1
Date: Tuesday, July 10, 2012 | Sheet 19 of 103

SSID = PCH



SSID = PCH



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

<Core Design>

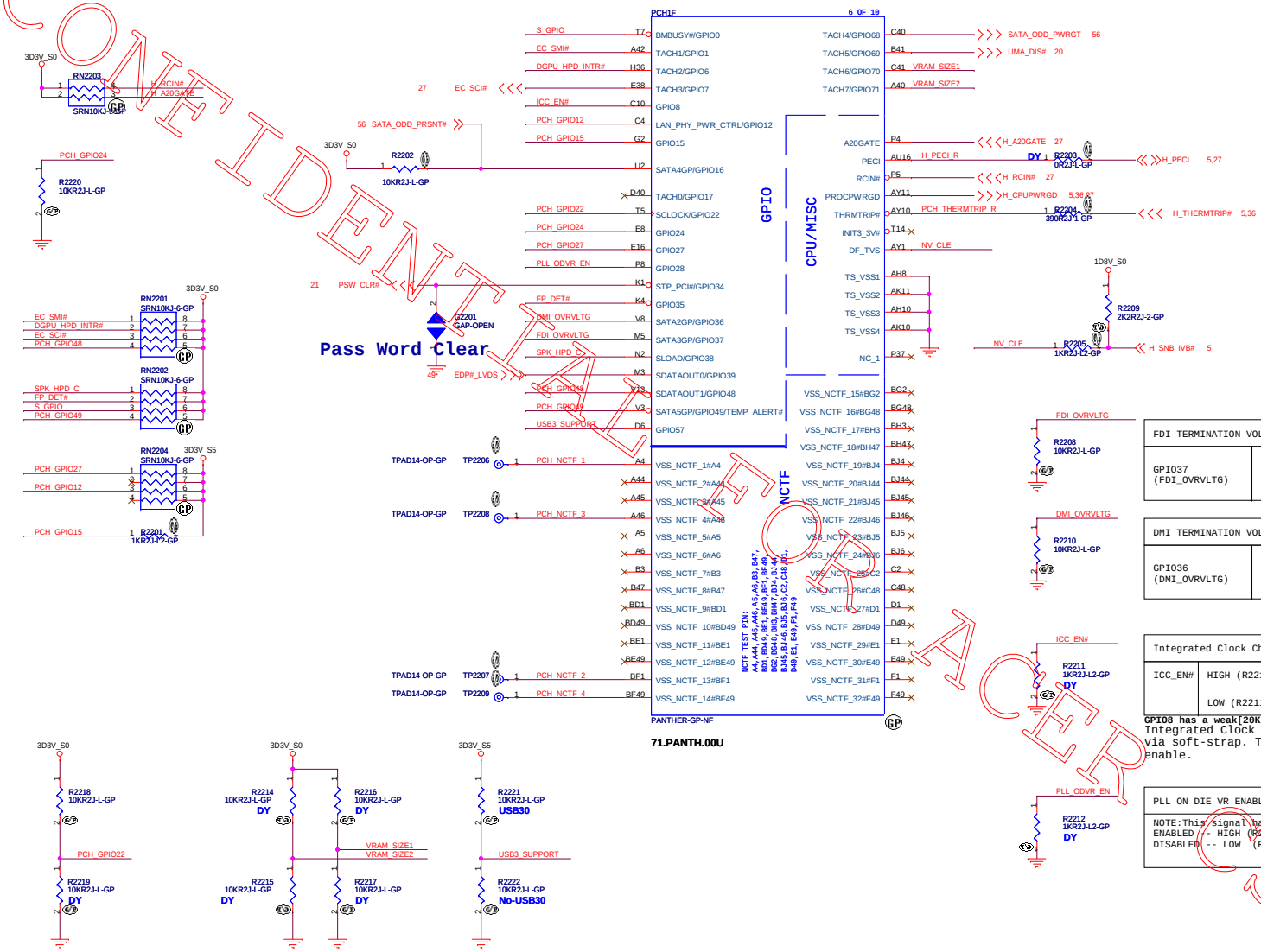
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

<Core Design>

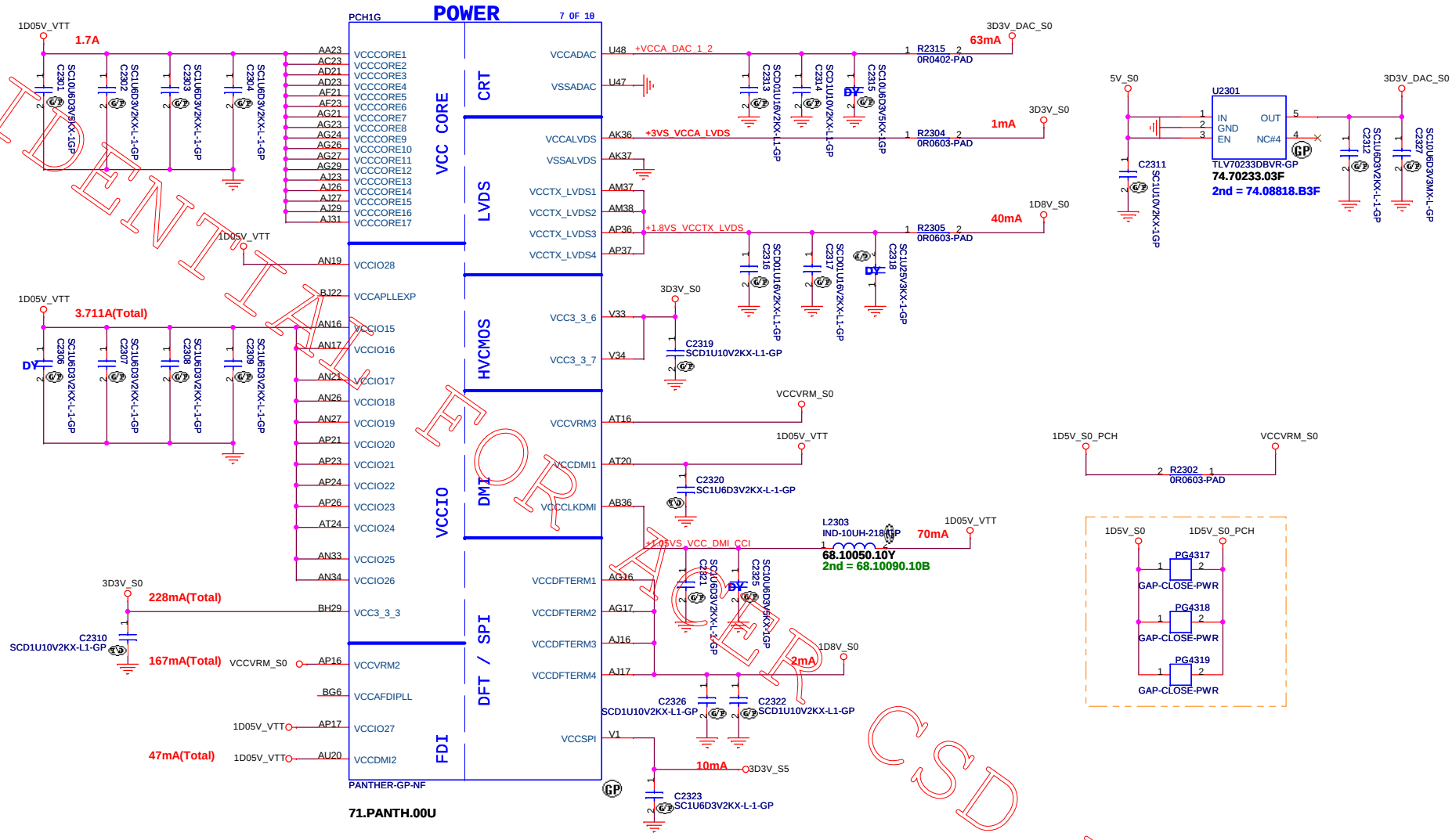
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 22 of 103

SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 23 of 103

SSID = PCH

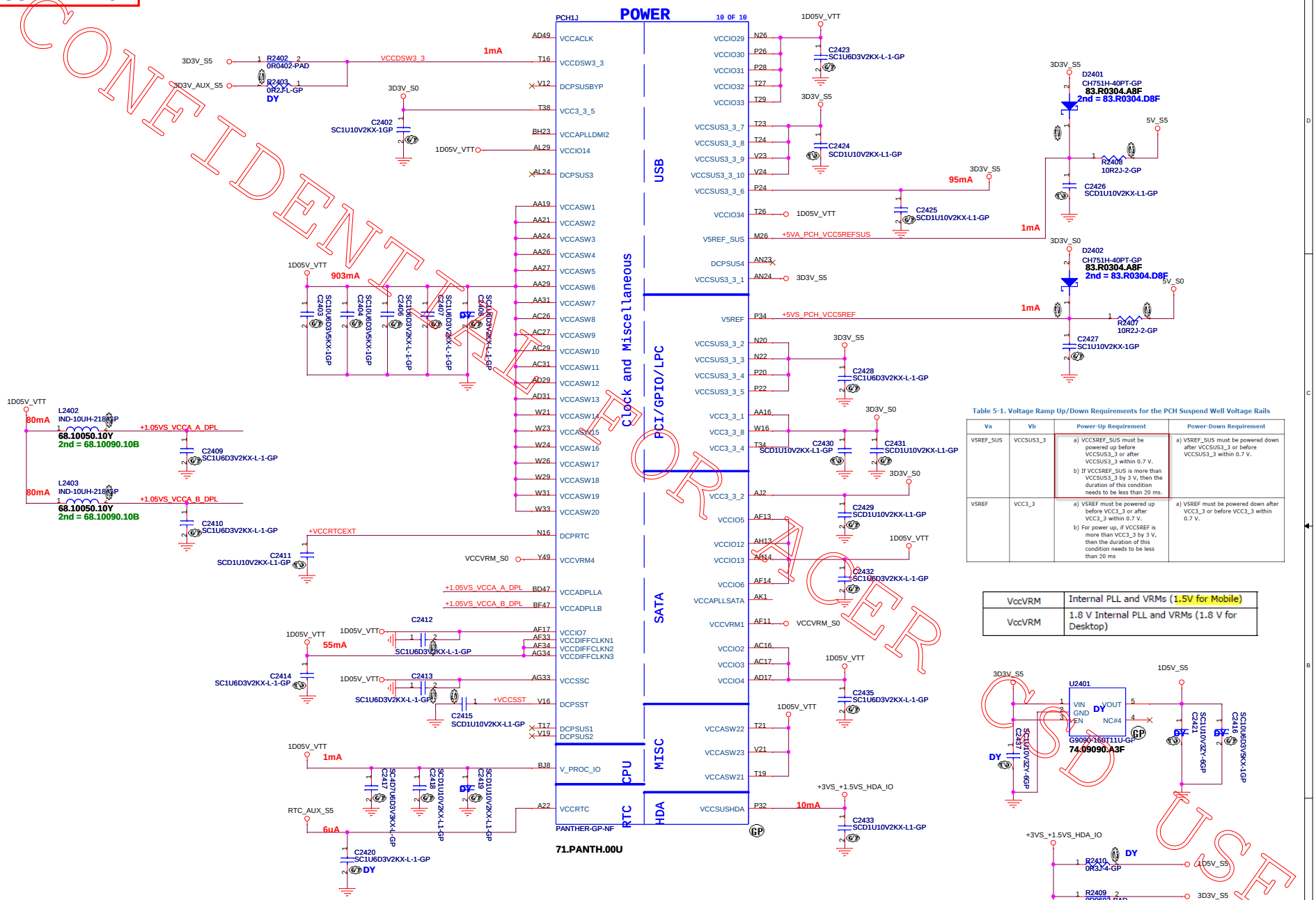


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

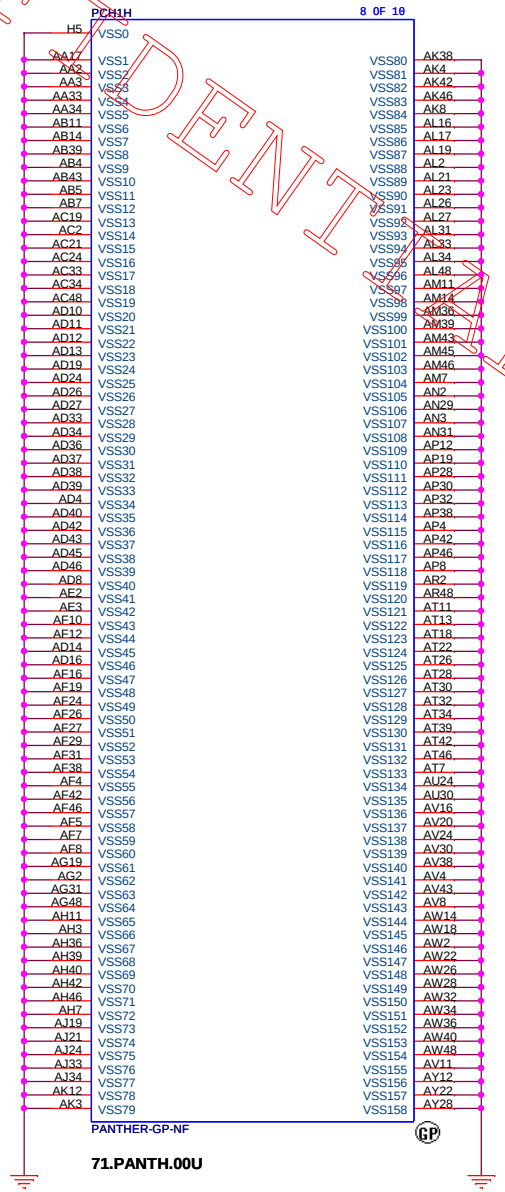
VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

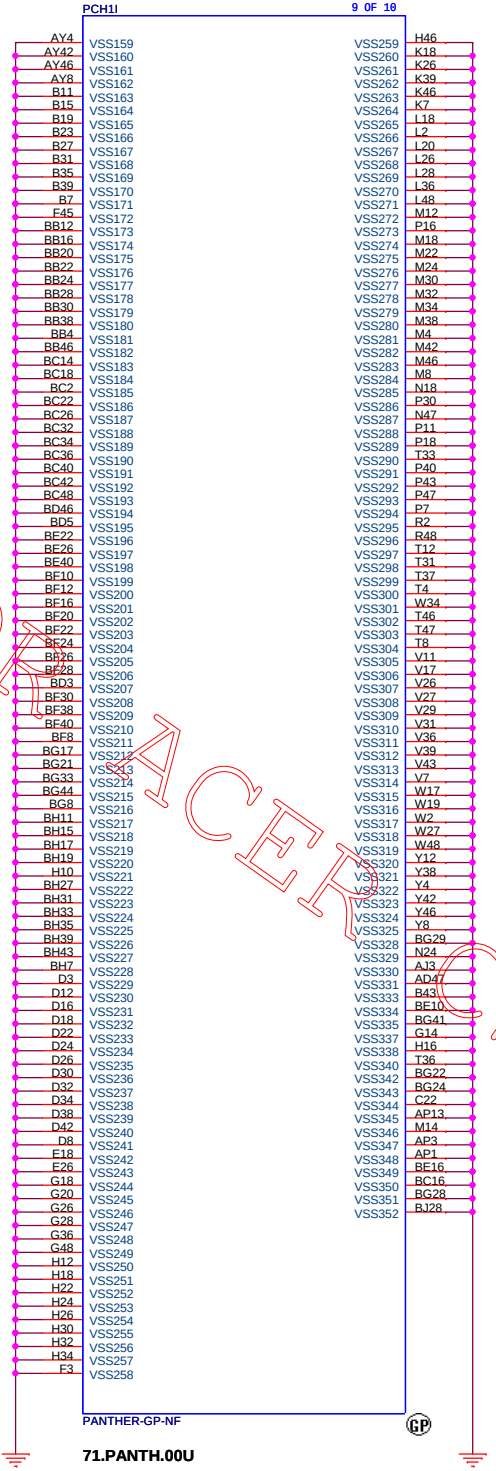
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size: Custom
Document Number: Petra Uma
Rev: -1
Date: Tuesday, July 10, 2012
Sheet 24 of 103

SSID = PCH





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 25 of 103

(Blanking)

<Core Design>

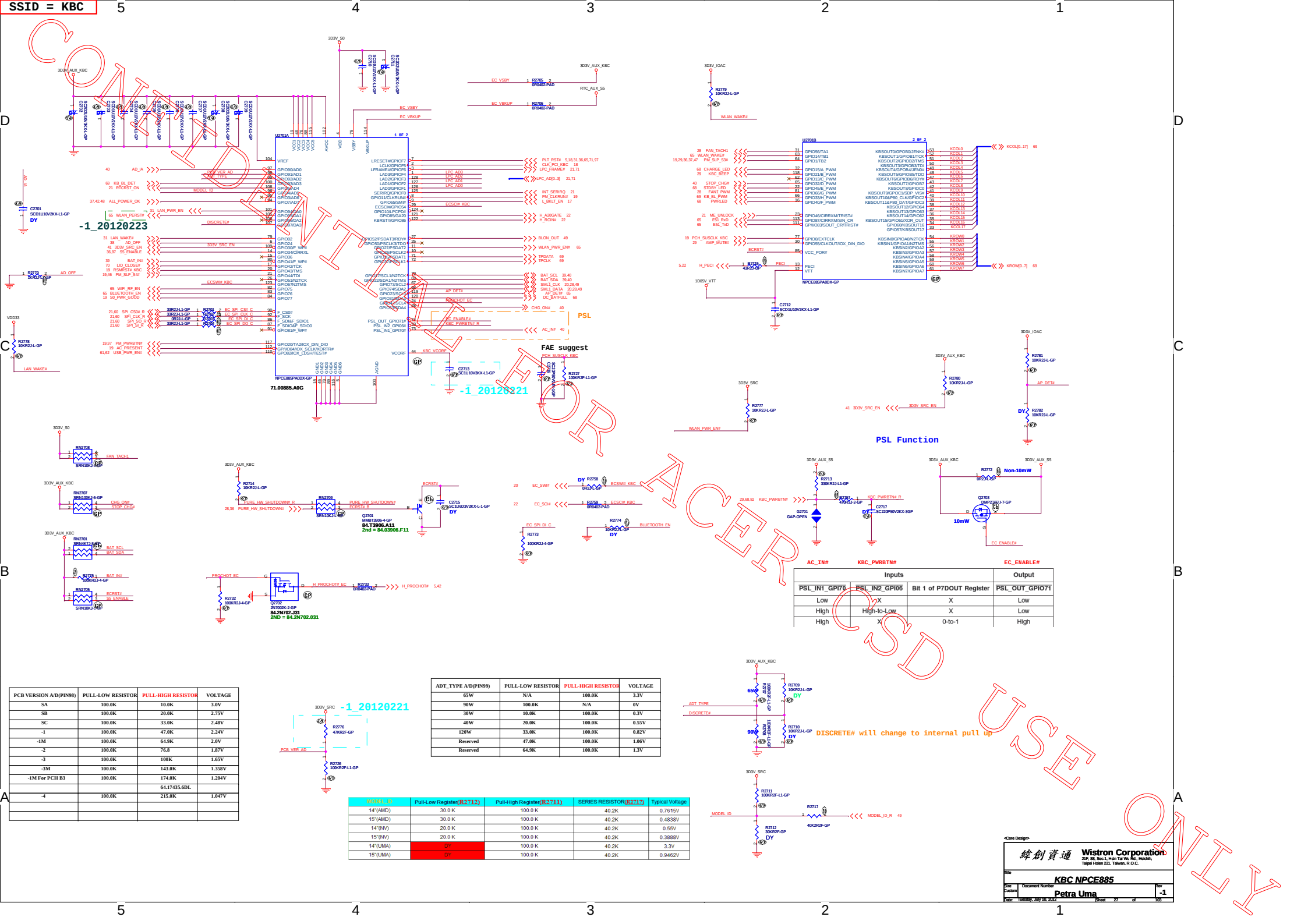
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Clock(colay)*

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 26 of 103

SSID = KBC



SSID = Thermal

Thermal sensor NCT 7718W

3D3V_S0

C2802
SCD1U10V2KX-L1-GP

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

Q2801
PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.T11

R2808
NTC-100K-8-GP
DY

P2800_DXP
C2806
SC470P50V3JN-2GP
DY
P2800_DXN
C2807
SC220P50V2KX-2GP

2.System Sensor, Put on palm rest

3D3V_S0
U2801
VDD
D+
D-
T_CRIT#
SCL
SDA
ALERT#
GND
NCT7718W-GP
THERM_SYS_SHDN#
NCT_CLK
NCT_DATA
ALERT#

1.H/W T8 Shutdown

RN2801
SRN2K2J-1-GP

Q2803
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

NCT_CLK
NCT_DATA
SML1_CLK 20,27,49
SML1_DATA 20,27,49

R2802
0R2J-L-GP
DY
R2803
0R2J-L-GP
DY

Layout 15 mil

5V_S0
D2802
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
C2809
SC4D7U10V3KX-GP
C2808
SCD1U10V2KX-L1-GP

ACES-CON4-29-GP
27 FAN1_PWM
R2806
0R0402-PAD
FAN1_PWM_R
FAN_TACH1_C
5V_S0
FAN1
20.F1639.004
2nd = 20.F1804.004
3rd = 20.F1352.004

27 FAN_TACH1
D2801
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
FAN_TACH1_C

ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree

3D3V_S0
R5
R2813
18K7R2D-GP
ALERT#

3D3V_S0
R7
R2809
2KR2F-3-GP

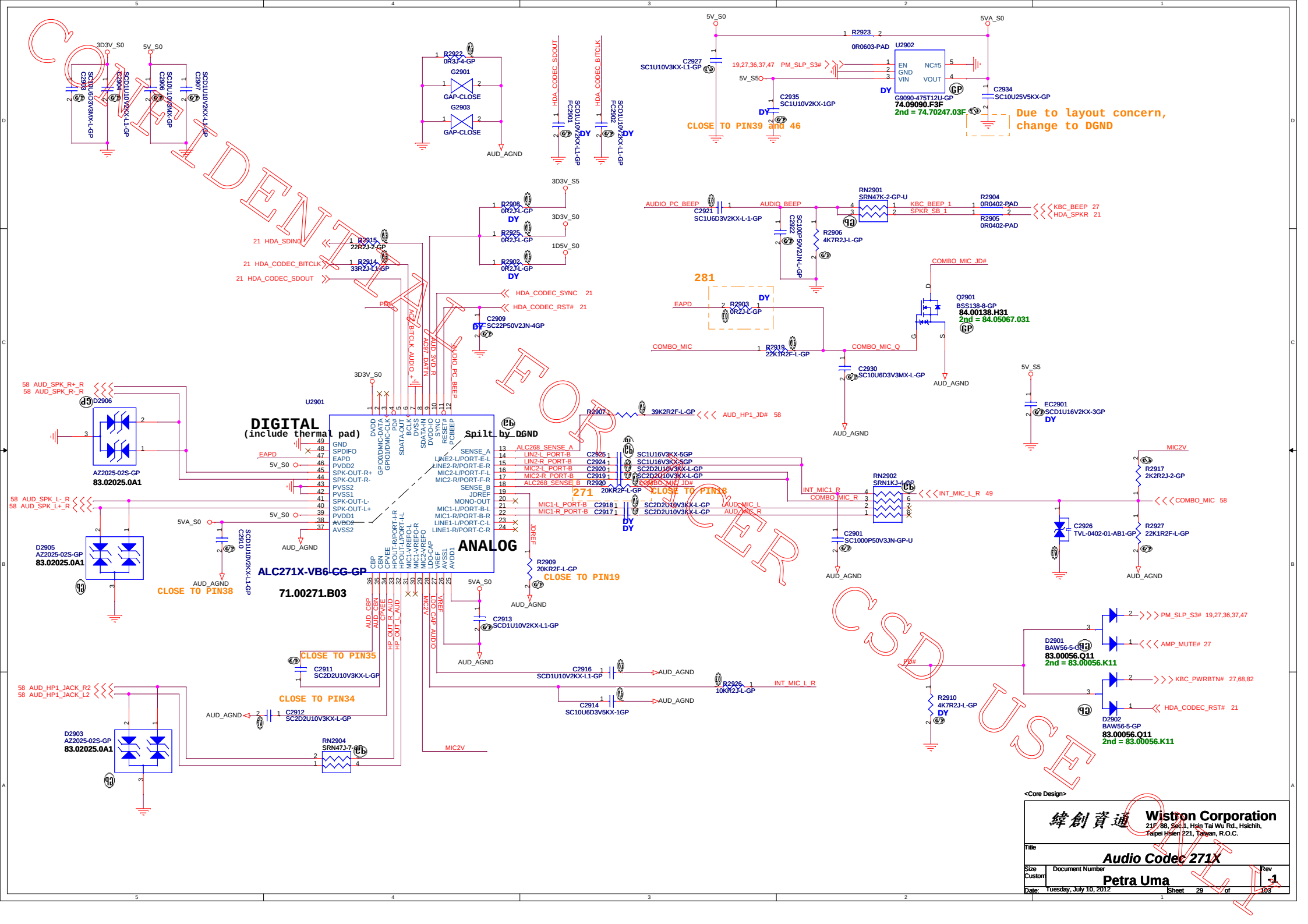
27,36 PURE_HW_SHUTDOWN#
R2812
10KR2J-L-GR
DY
C2810
SCD1U10V2KX-L1-GP
DY

Q2802
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
S
D
G
THERM_SYS_SHDN#
IMVP_PWRGD_R
DY
R2810
0R2J-L-GP
3D3V_S0
R2811
0R0402-PAD
IMVP_PWRGD 36,42

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal 7718/Fan Controllor P2793*
Size: Custom
Document Number: Petra Uma
Rev: -1
Date: Tuesday, July 10, 2012
Sheet 28 of 103


CONFIDENTIAL
FOR WISTRON USE ONLY
U2901
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB6-CG-GP
71.00271.B03
U2902
G9090-475T12U-GP
74.09090.F3F
2nd = 74.70247.03F
Due to layout concern, change to DGND
CLOSE TO PIN39 and 46
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
CLOSE TO PIN18
271
281
Q2901
BSS138-8-GP
84.00138.H31
2nd = 84.05067.031
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
D2902
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
D2903
AZ2025-02S-GP
83.02025.0A1
D2905
AZ2025-02S-GP
83.02025.0A1
D2906
AZ2025-02S-GP
83.02025.0A1
RN2901
SRN47K-2-GP-U
RN2902
SRN1KJ-4-GP
RN2904
SRN47J-7-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec 271X
Size
Custom
Document Number
Petra Uma
Rev
-1
Date: Tuesday, July 10, 2012
Sheet 29 of 103

(Blanking)

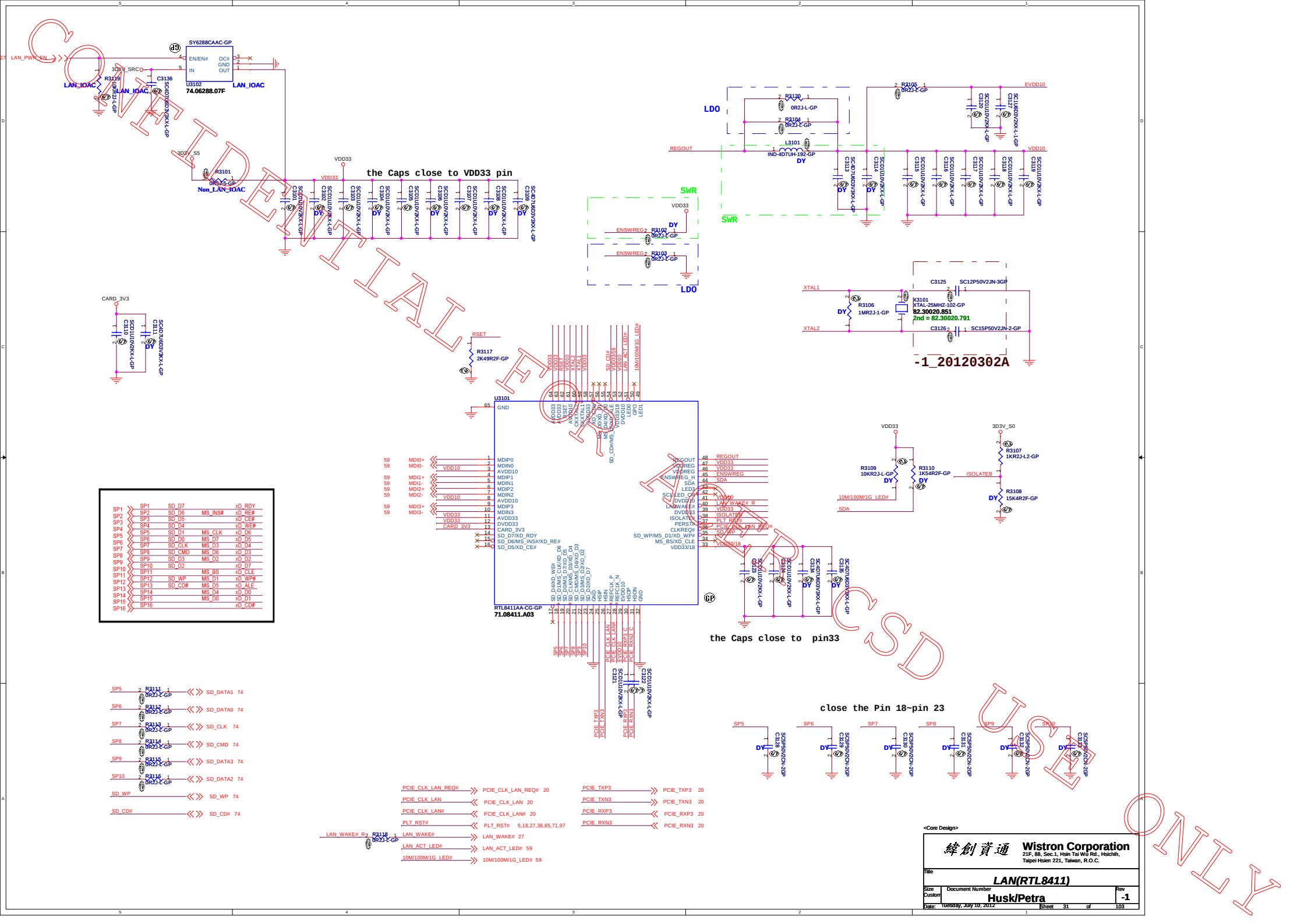
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio AMP**

Size: A4 | Document Number: **Petra Uma** | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 30 of 103


CONFIDENTIAL
SY6288CAAC-GP
U3102
74.06288.07F
LAN_IOAC
Non_LAN_IOAC
the Caps close to VDD33 pin
LDO
SWR
RTL8411AA-CG-GP
71.08411.A03
-1_20120302A
the Caps close to pin33
close the Pin 18~pin 23
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN(RTL8411)
Husk/Petra
Tuesday, July 10, 2012
Sheet 31 of 103
-1
ISOLATEB
LAN_WAKE#
PCIE_CLK_LAN_REQ#
PCIE_CLK_LAN
PCIE_CLK_LAN#
PLT_RST#
PCIE_TXP3
PCIE_TXN3
PCIE_RXP3
PCIE_RXN3
SD_DATA1
SD_DATA0
SD_CLK
SD_CMD
SD_DATA3
SD_DATA2
SD_WP
SD_CD#
CONFIDENTIAL
LAN CSD USE ONLY

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTS5159 (CARD READER)**

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 34 of 103

(Blanking)

<Core Design>

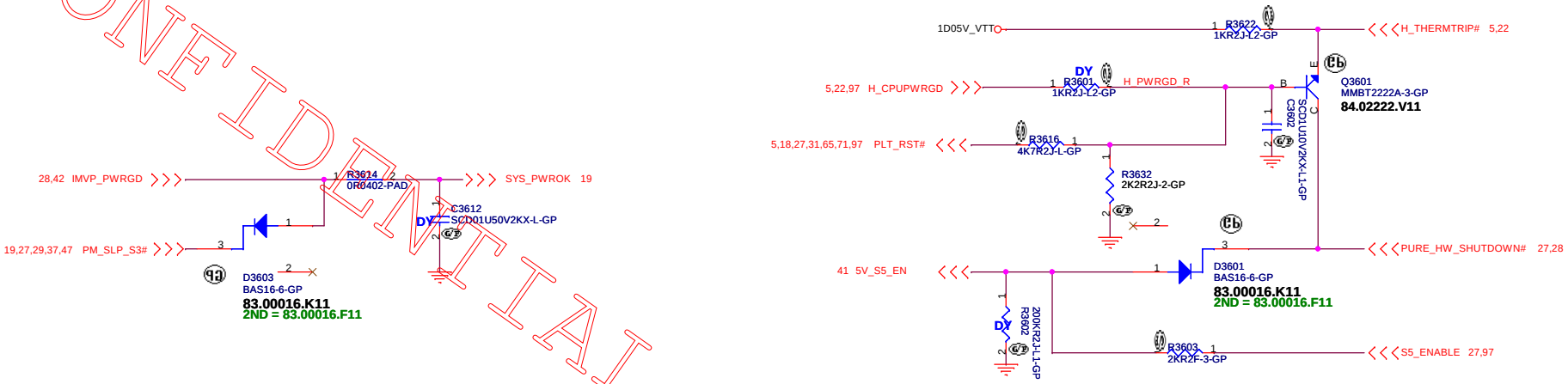
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Controller*

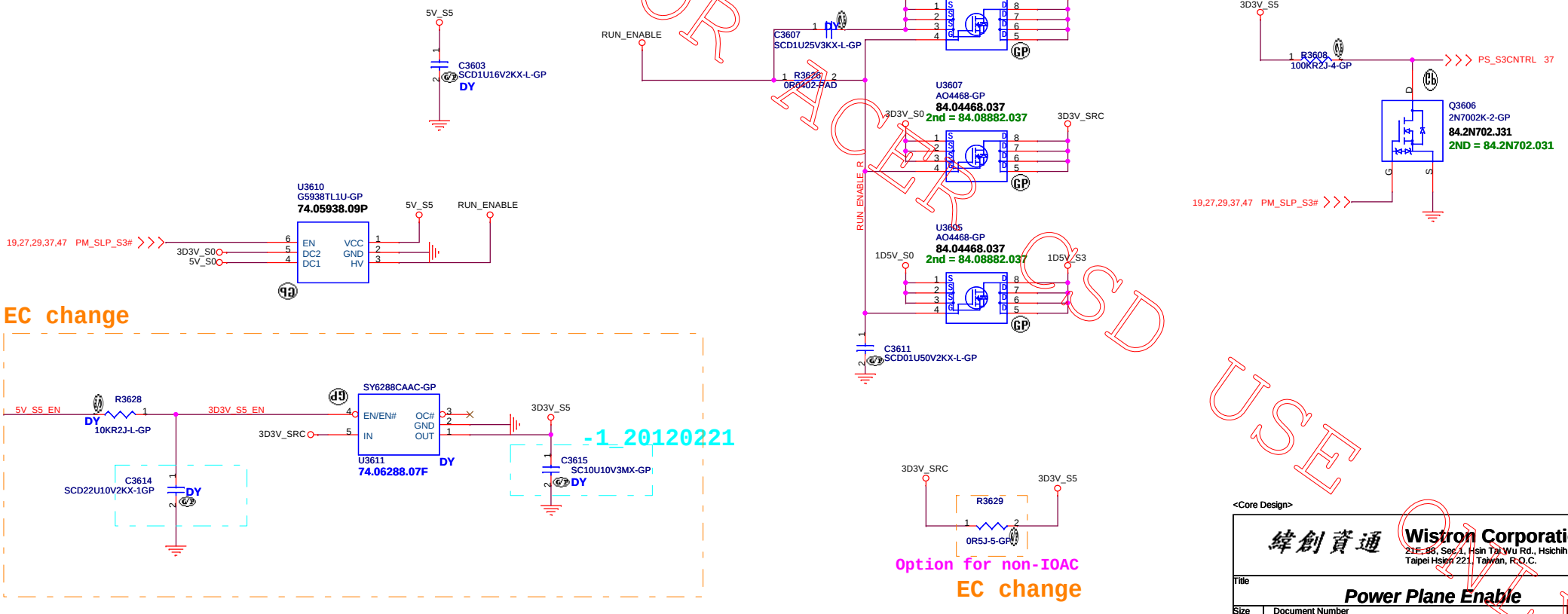
Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 35 of 103

Power Sequence



ANNIE Run Power



<Core Design>

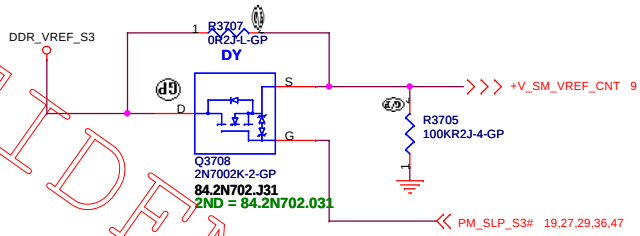
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

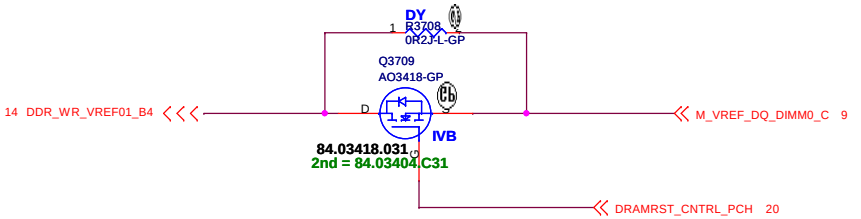
Title: Power Plane Enable

Size: A3 | Document Number: Petra Uma | Rev: -1

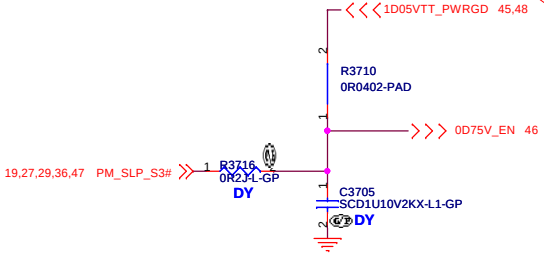
Date: Tuesday, July 10, 2012 | Sheet 36 of 103

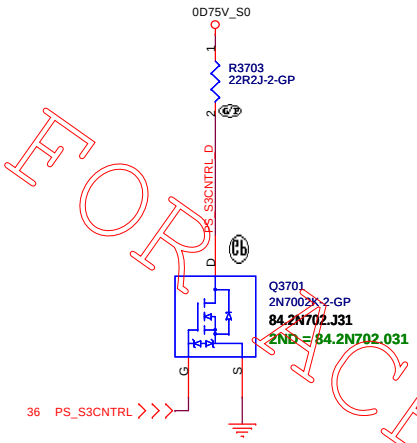
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

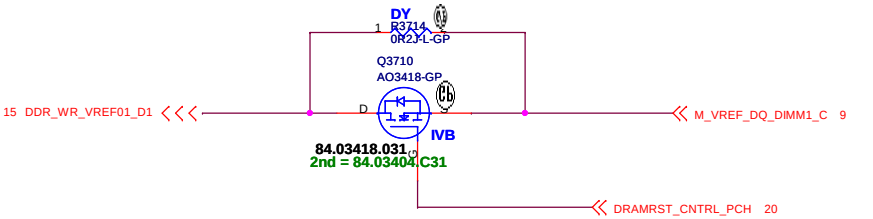




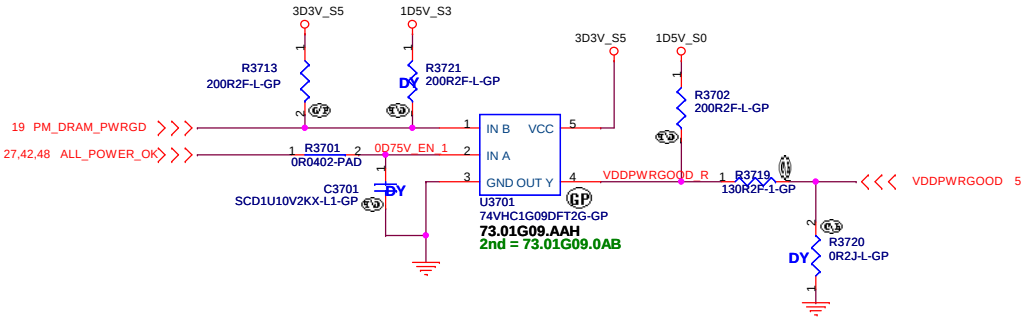
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



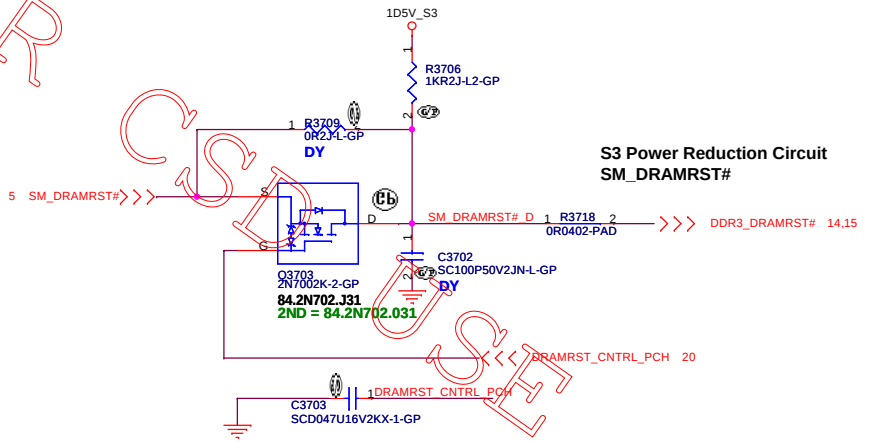




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

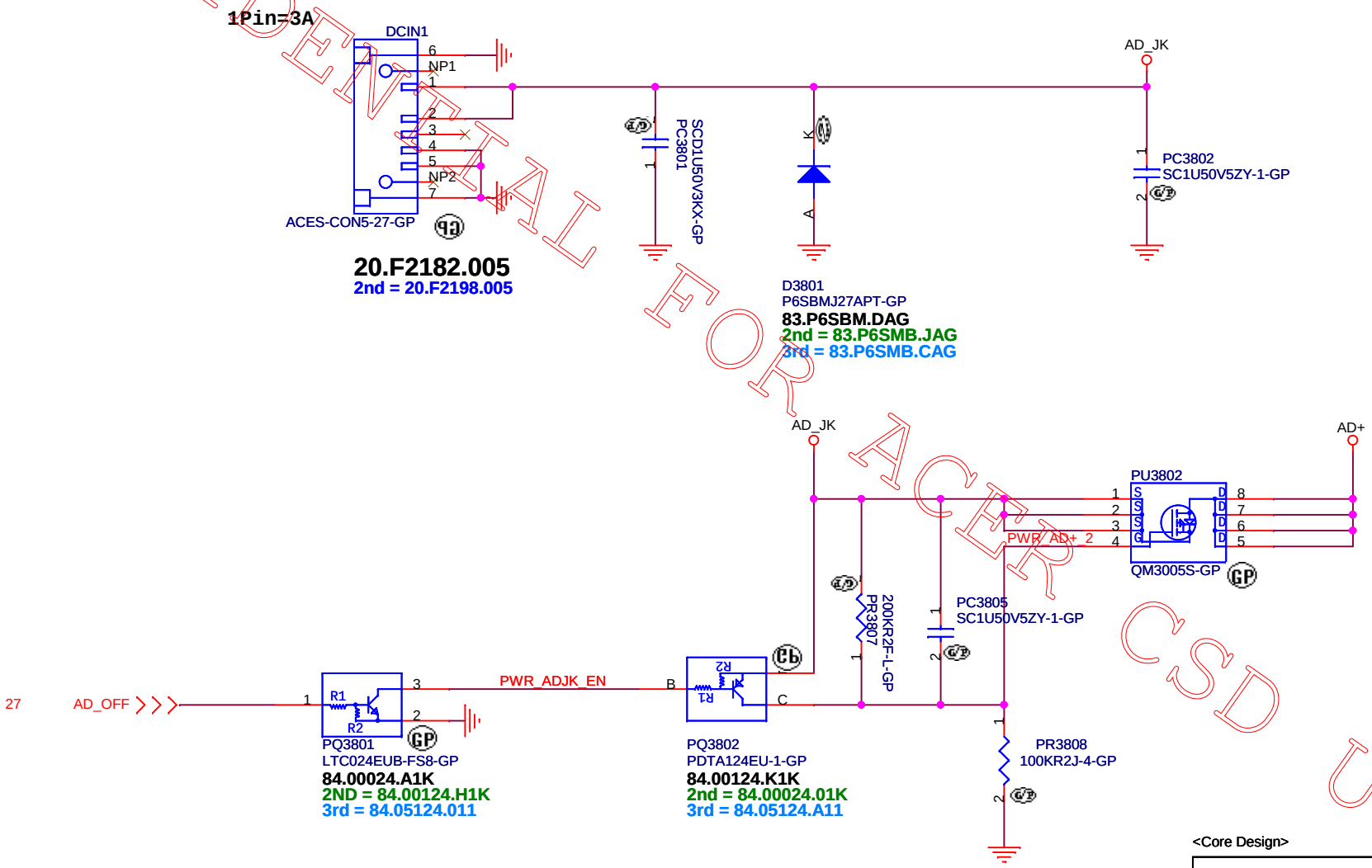
Title: **ADAPTER**

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 37 of 103

ANNIE solution

Adaptor in to generate DCBATOUT



<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
A4	**Petra Uma**	-1

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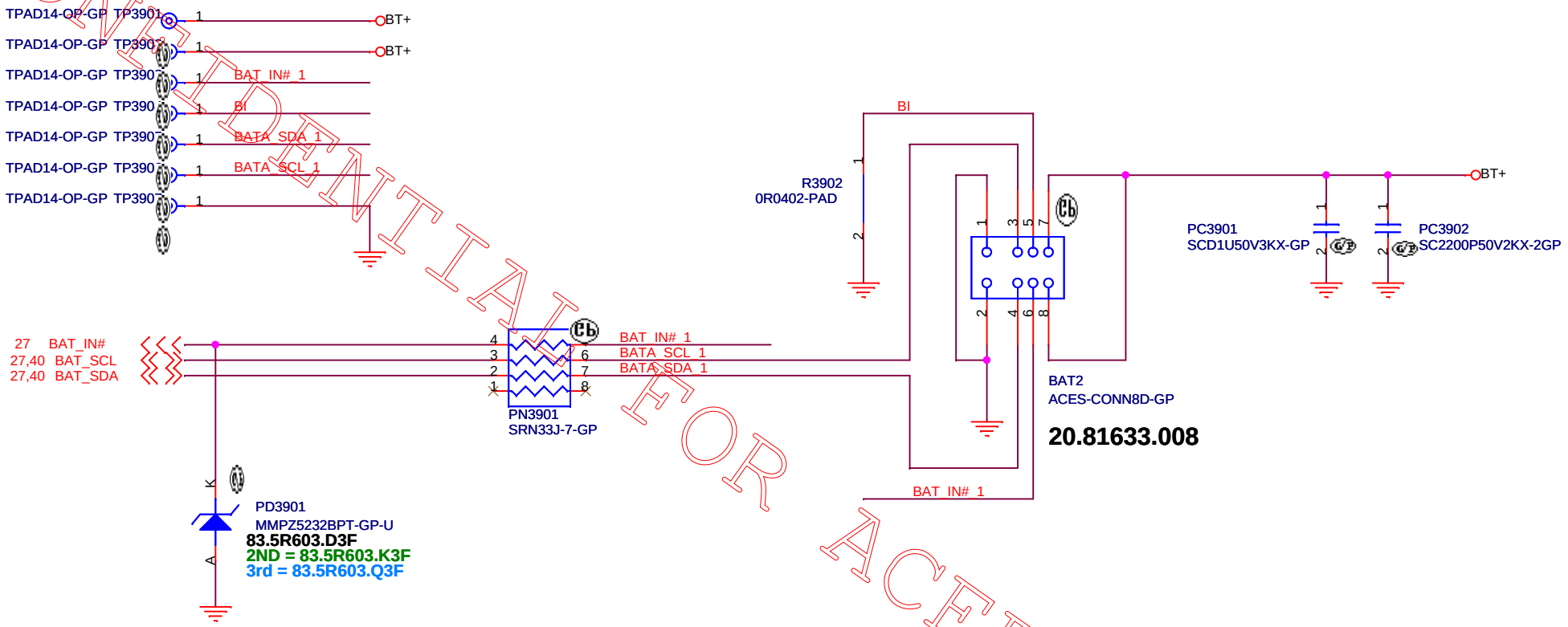
BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 39 of 103

SSID = Charger

A87(ANNIE/ASTRO)
PR4007 PR4001

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

Delete PC4008
Wayler , 2011-1208

Delete PR4016
PR4015 change to 10 ohm
Wayler , 2011-1208

EC change

PL4001 change to 7*7*3

MAG. 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Charger Current=1.4~3.6A

PU4003 change to 74.24727.073
Wayler , 2011-1208

PR4032 , PR4033 DY
Wayler , 12-06

<Core Design>

Wistron Corporation
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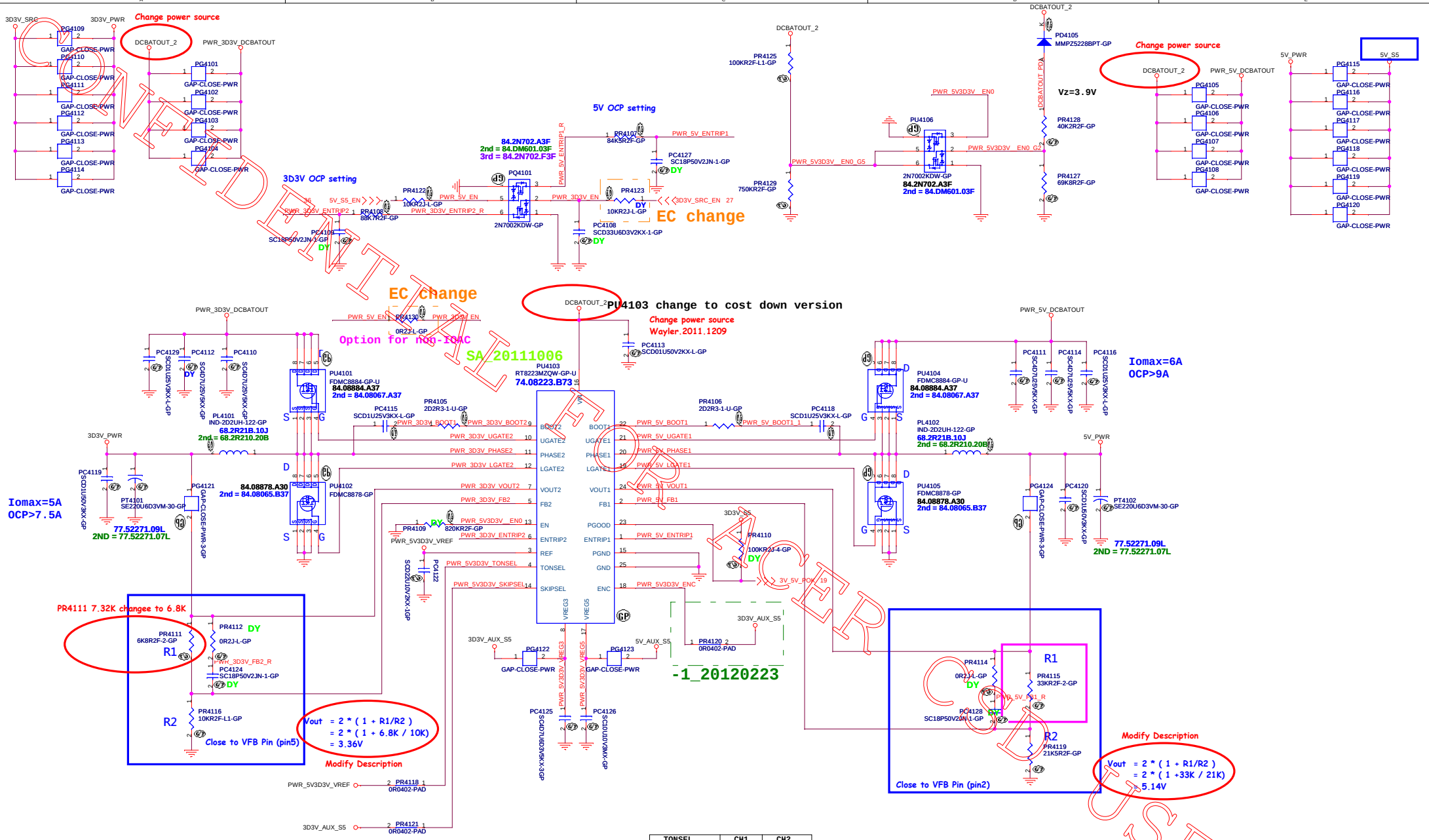
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 40 of 108



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(RT8223M)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 41 of 103

SSID = CPU.Regulator

PC4205 package change to 0402

Setting LoadLine

PC4210 package change to 0402

Setting IMax

PC4211 package change to 0402

PC4206 DY

Setting GFX LoadLine

Place near choke of Phase1

Setting OCP

PR4218 change to 453 ohm
Wayler 12.06

SA:change power plane

PR4240 DY
Wayler 12.06

PU4201 change to V1.7 (74.95836.B33)

NTC Place near high side MOSFET of Phase1

NTC place near high side MOSFET of Phase1

Close to VR

SA:change to be 0603

-1_20120223

<Core Design>

Wistron Corporation
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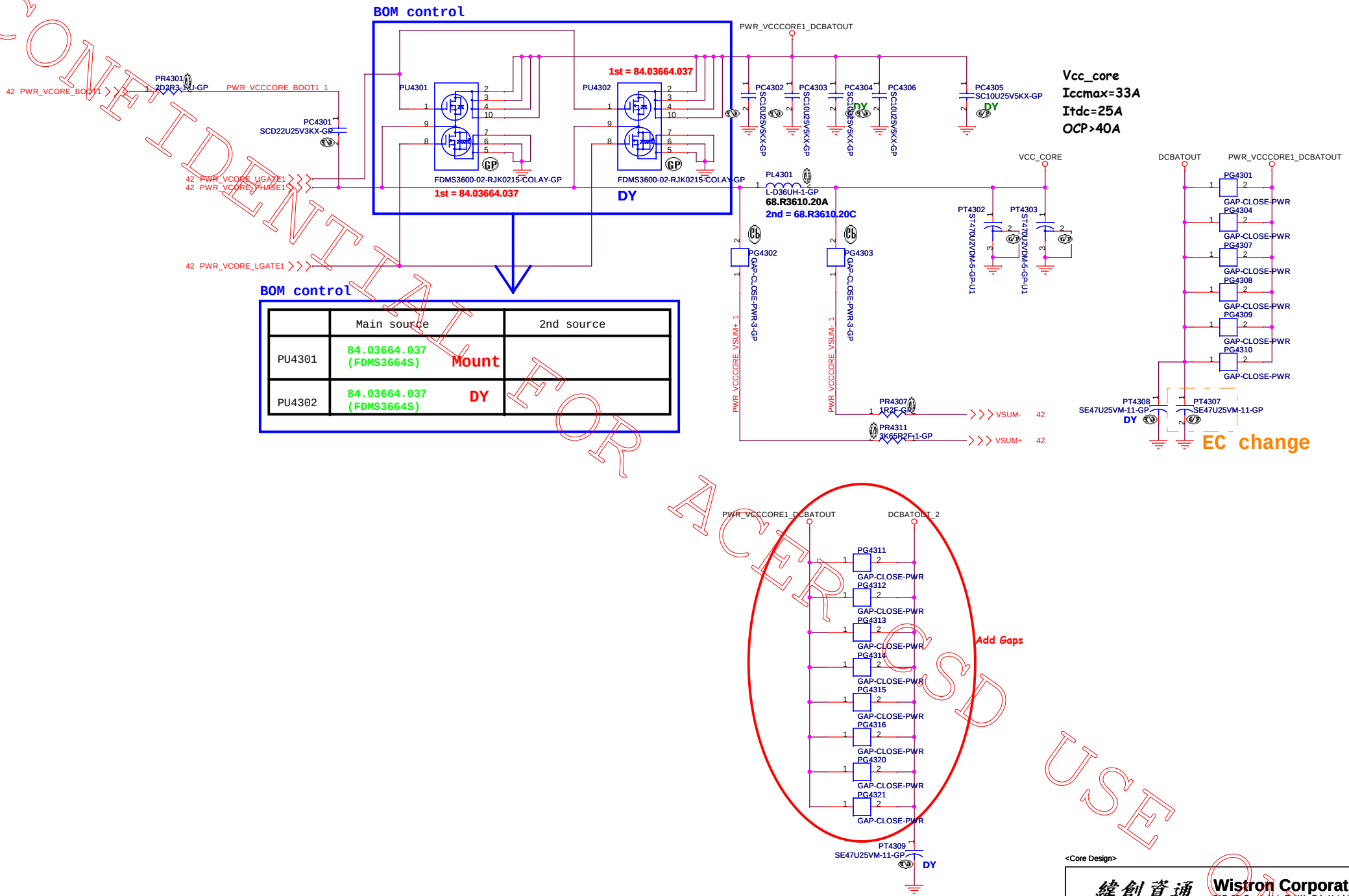
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(1/3)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 42 of 102



<Core Design>

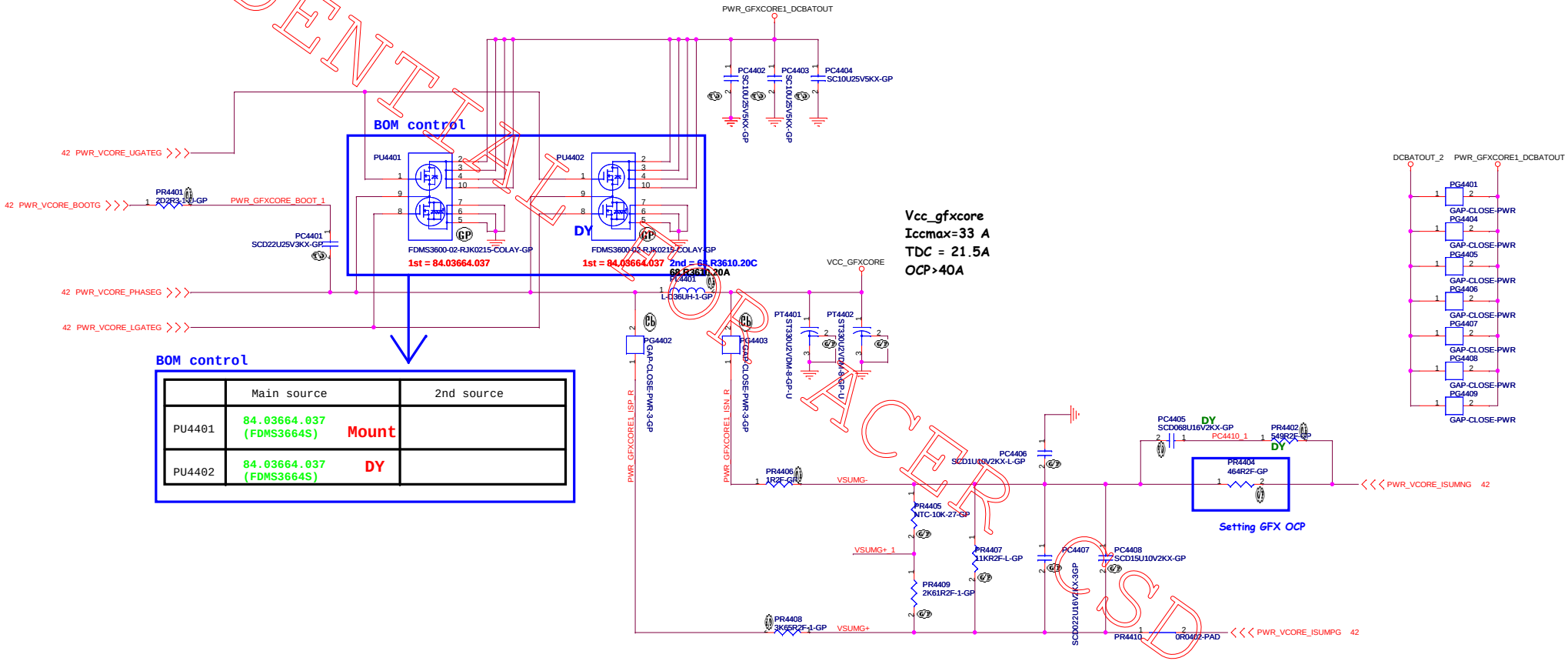
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number | Rev: -1

Petra Uma

Date: Tuesday, July 10, 2012 | Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(3/3)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 44 of 102

TPS51218D for 1D05V

DCBATOUT_2 PWR_DCBATOUT_1D05V
PG4501 PG4502 PG4503 PG4504 GAP-CLOSE-PWR

1D05V_VTT 1D05V_PWR 1D05V_VTT
PG4513 PG4514 PG4515 PG4516 PG4518 PG4520 GAP-CLOSE-PWR
PG4506 PG4507 PG4508 PG4509 PG4510 PG4511 PG4512 GAP-CLOSE-PWR

DCBATOUT PWR_DCBATOUT_1D05V
PG4521 PG4522 PG4523 GAP-CLOSE-PWR

PT4501 SE47U25VM-11-GP DY

PR4504 change to 54K9 , OCP > 27A
2012-0130 , Wayler.

Freq=360KHz

3D3V_S0 PR4516 10KR2J-L-GP
37,48 1D05VTT_PWRGD
46,47 RUNPWROK PR4512 0R0402-PAD
PR4504 54K9R2F-L-GP
PC4505 SC1KP50V2KX-1GP

PU4501
PGOOD TRIP EN VFB RF GND VBST DRVH SW V5IN DRVL
PWR_1D05V_IMAX PWR_1D05V_EN PWR_1D05V_VFB PWR_1D05V_CCM
PWR_1D05V_BOOT PWR_1D05V_UGATE PWR_1D05V_PHASE PWR_1D05V_LGATE
TPS51218DSCR-GP-U2
74.51218.073

PR4503 470KR2F-GP
PR4505 2D2R3-1-U-GP
PWR_1D05V_BOOT_R
PC4503 SCD1U25V3KX-L-GP
C4502 SC1U10V2KX-1GP
05V_S5

PWR_DCBATOUT_1D05V
PU4502 FDMS7698-GP
84.07698.037
2nd = 84.08065.037
PU4503 FDMS0308AS-GP
84.00308.B30
2nd = 84.08058.037
G D S

PC4504 PC4506 PC4507 PC4511
SC4D7U25V5KX-GP SC4D7U25V5KX-GP SCD01U25V2KX-3GP SCD1U25V3KXL-GP

Pana. 0.42uH 7*7*4
DCR=1.5mohm
PL4501 IND-D42UH-4-GP
SD:暫時先換7x7mm

Iomax = 20.645A
TDC = 14.45 A
OCP > 26.83A

PR4506 10R2F-L-GP
PR4507 10KR2F-L1-GP
PR4508 20KR2F-L-GP
PR4509 10R2F-L-GP
VTT_SENSE_L
VSS_SENSE_L
PWR_1D05V_VFB
SC18P50V2JN-1-GP
PC4508

1D05V_PWR
PC4509 SCD1U50V3KX-GP
PT4504 PT4503 SE330U2VDM-L-GP
79.33719.L01

-1_20120221

PR4510 0R2J-L-GP
PC4510 SC1000P50V3JN-GP-U
PR4511 0R2J-L-GP
VTT_SENSE_L → VCCIO_SENSE 8
VSS_SENSE_L → VSSIO_SENSE 8

Vout=0.704*(1+R1/R2)

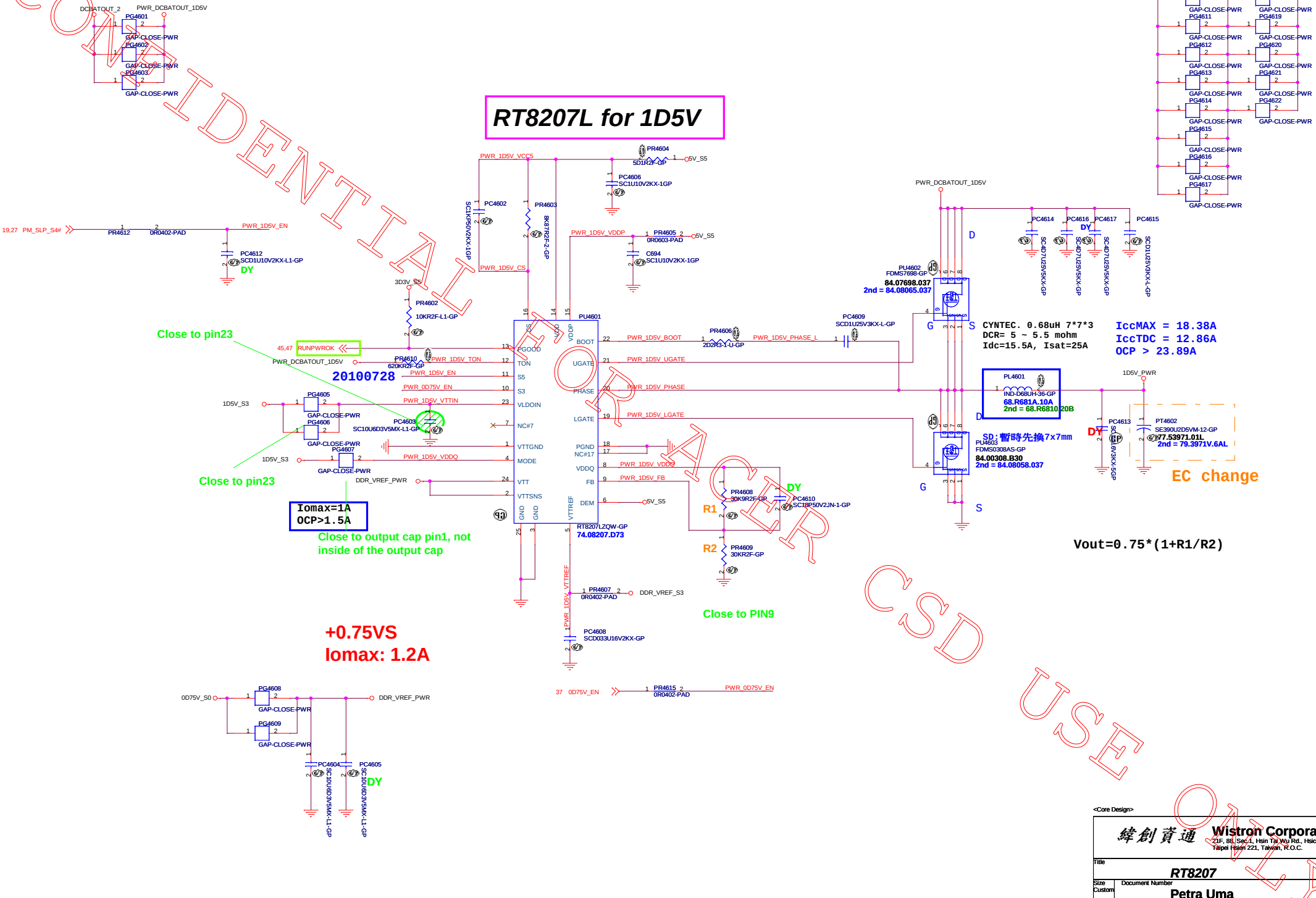
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)
Size: A3 | Document Number: Petra Uma | Rev: -1
Date: Tuesday, July 10, 2012 | Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

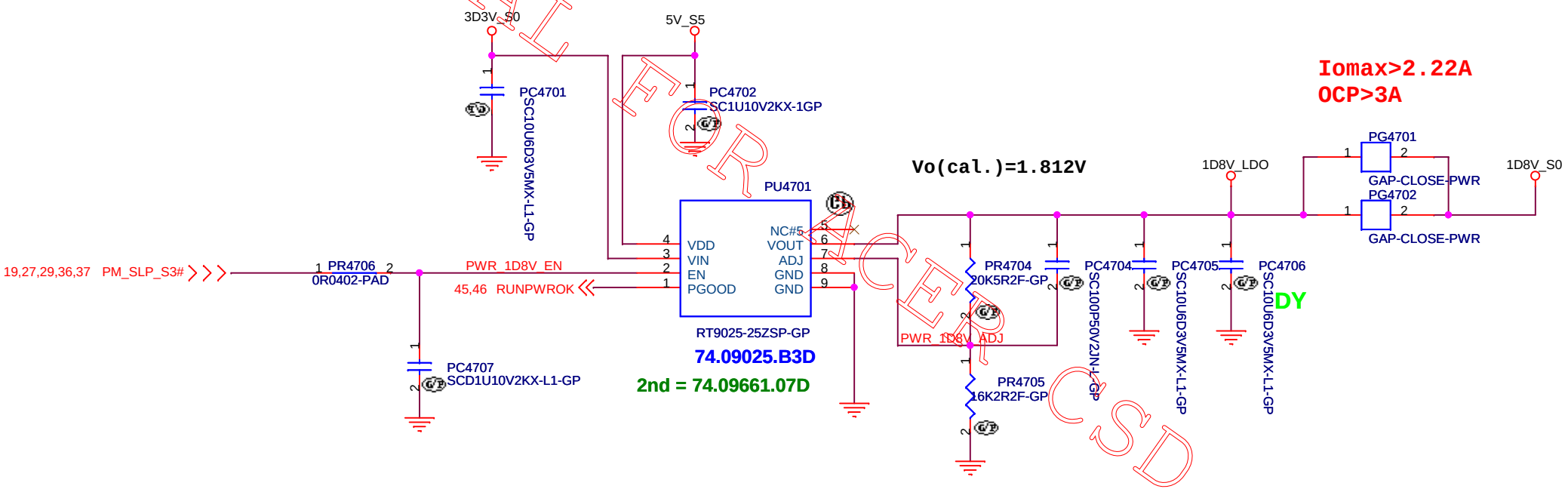
Title: RT8207

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO_1D8V(RT9025)***

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 47 of 103

LDO G978 for VCCSA

D0, D1 V_O Selection Table

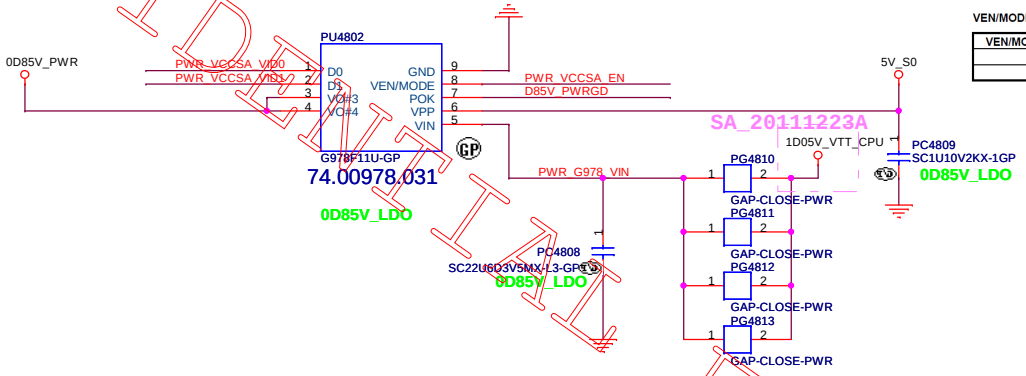
D0	D1	V_O, MODE=0	V_O, MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

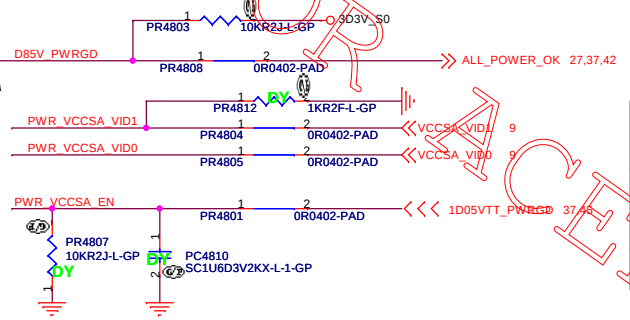
VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

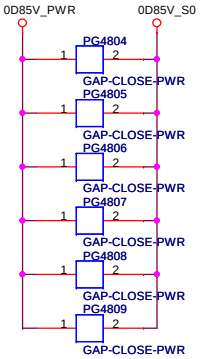
VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1



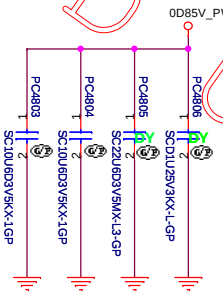
PWM SY8037 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



Design Current =4 A



<Core Design>

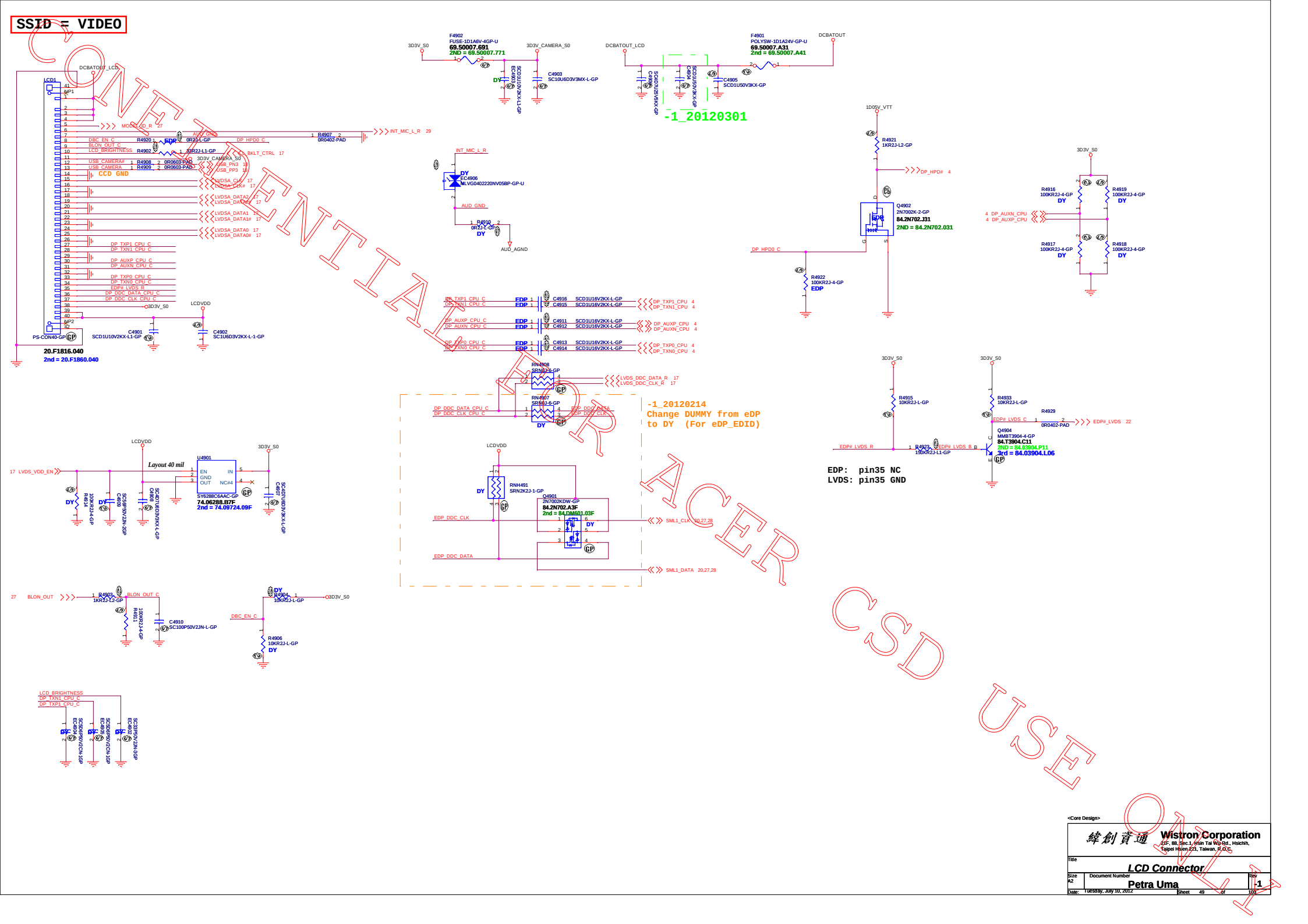
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA SY8037

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 48 of 103

SSID = VIDEO



<Core Design>

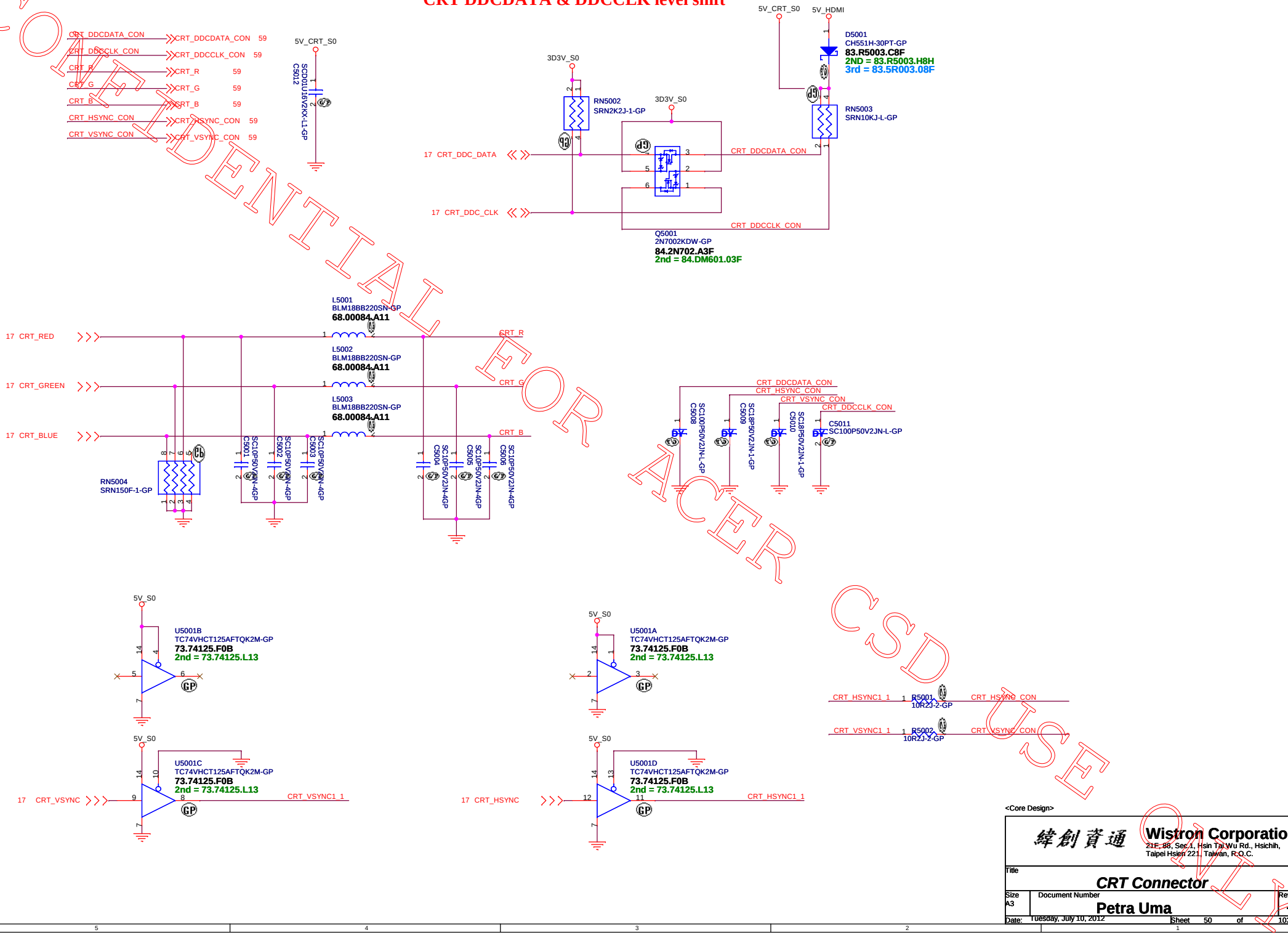
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: A2 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 49 of 103

CRT DDCDATA & DDCCLK level shift



<Core Design>

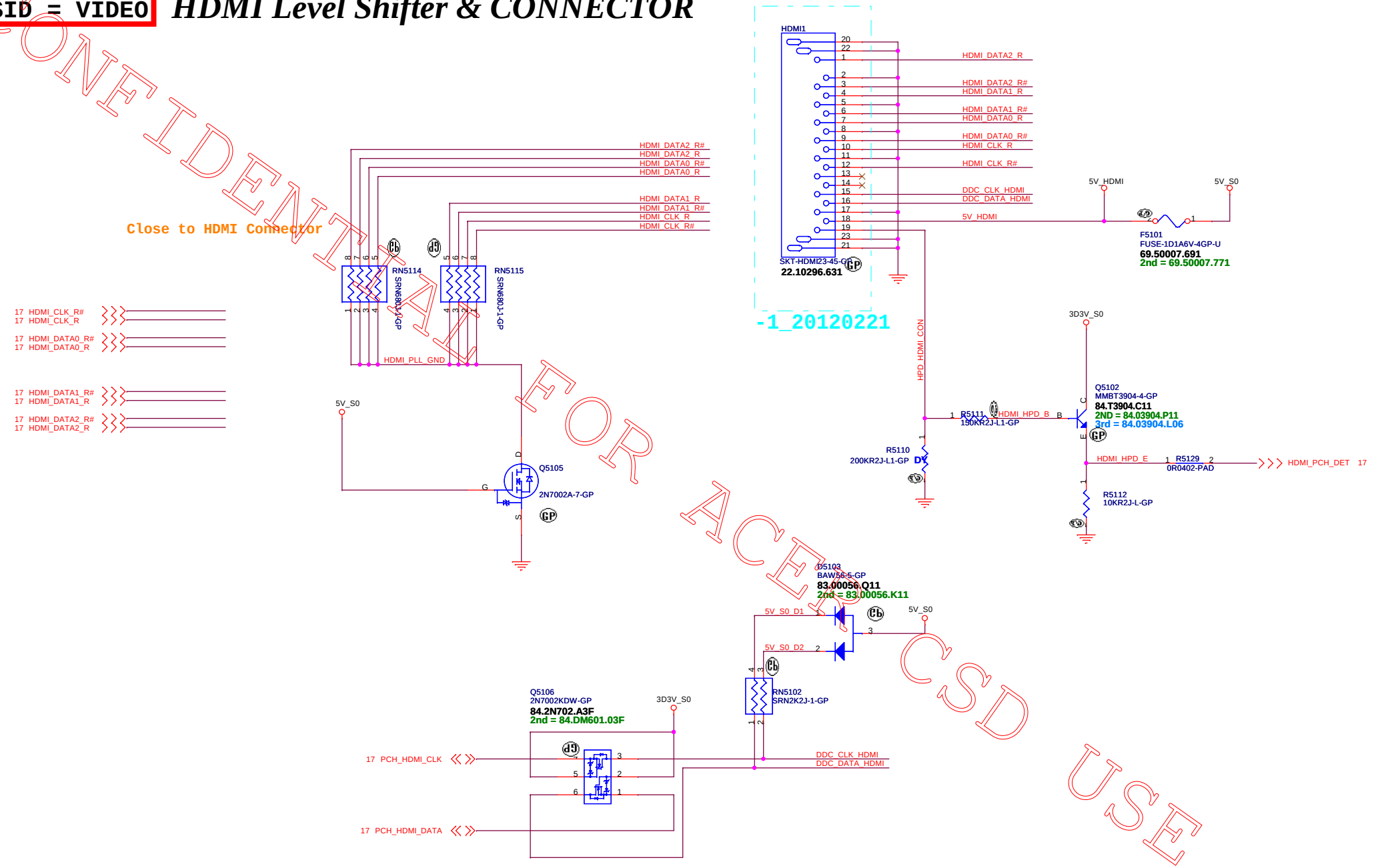
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CRT Connector**	
Size A3	Document Number **Petra Uma**	Rev -1
Date: Tuesday, July 10, 2012	Sheet 50 of 103	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector



<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 52 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 53 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	-1

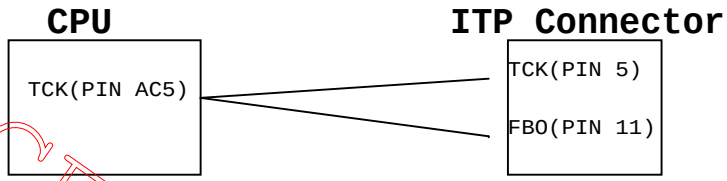
Date: Wednesday, February 22, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

(Blanking)



<Core Design>

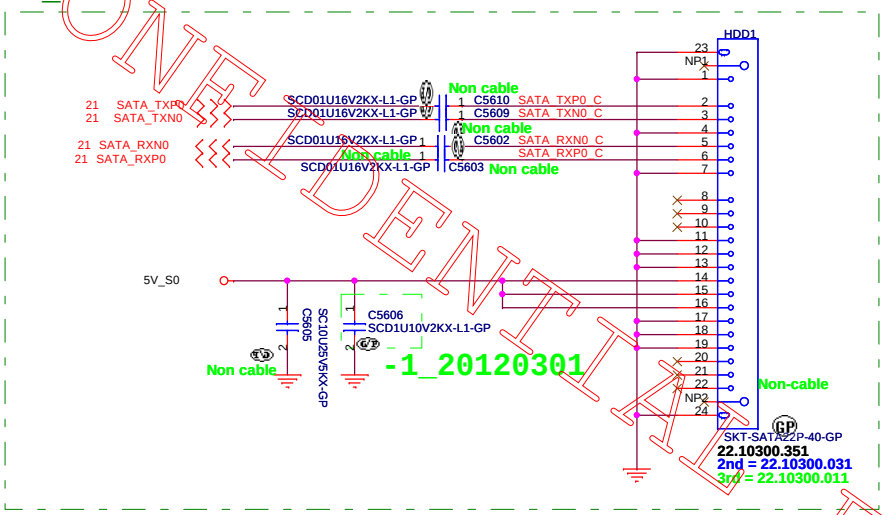
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

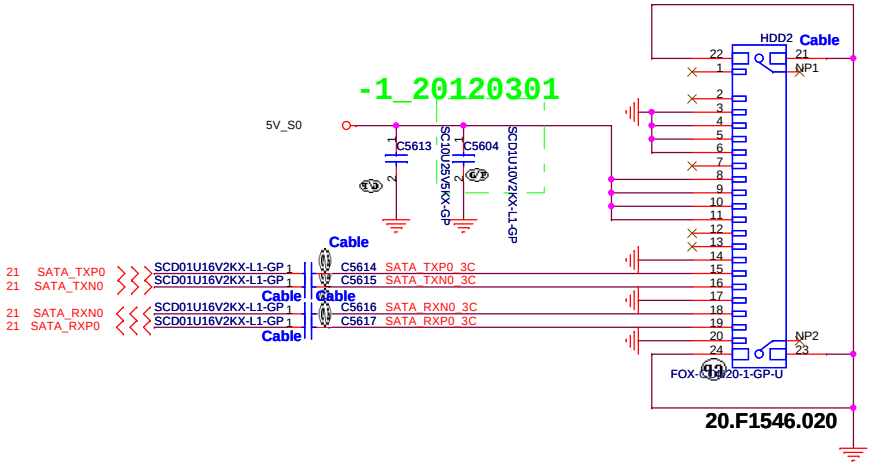
Title: ITP		
Size: A4	Document Number: Petra Uma	Rev: -1
Date: Wednesday, February 22, 2012	Sheet 55 of 103	

SSID = SATA

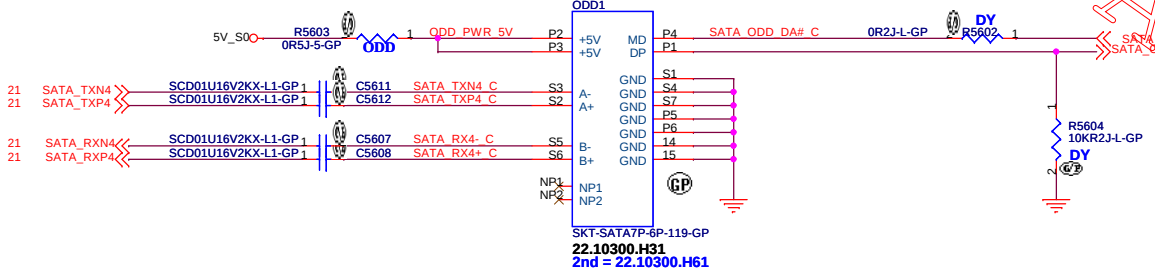
-1_20120223

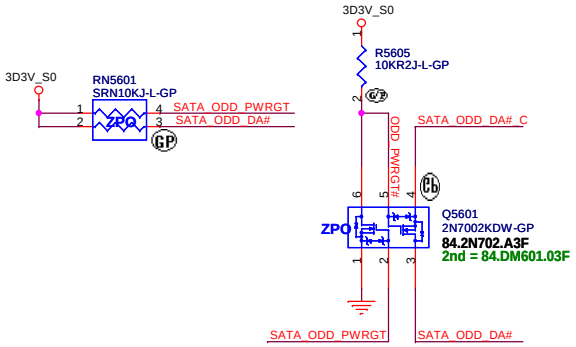
SATA HDD Connector



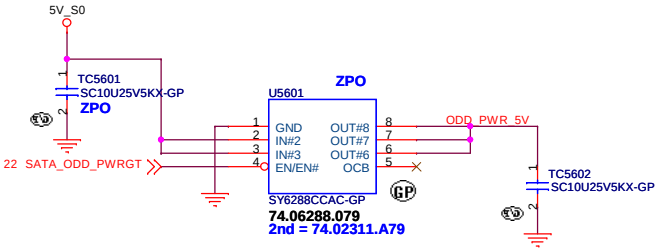


ODD Connector





SATA Zero Power ODD



High Active 2A

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: HDD/ODD

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 56 of 103

ESATA Power

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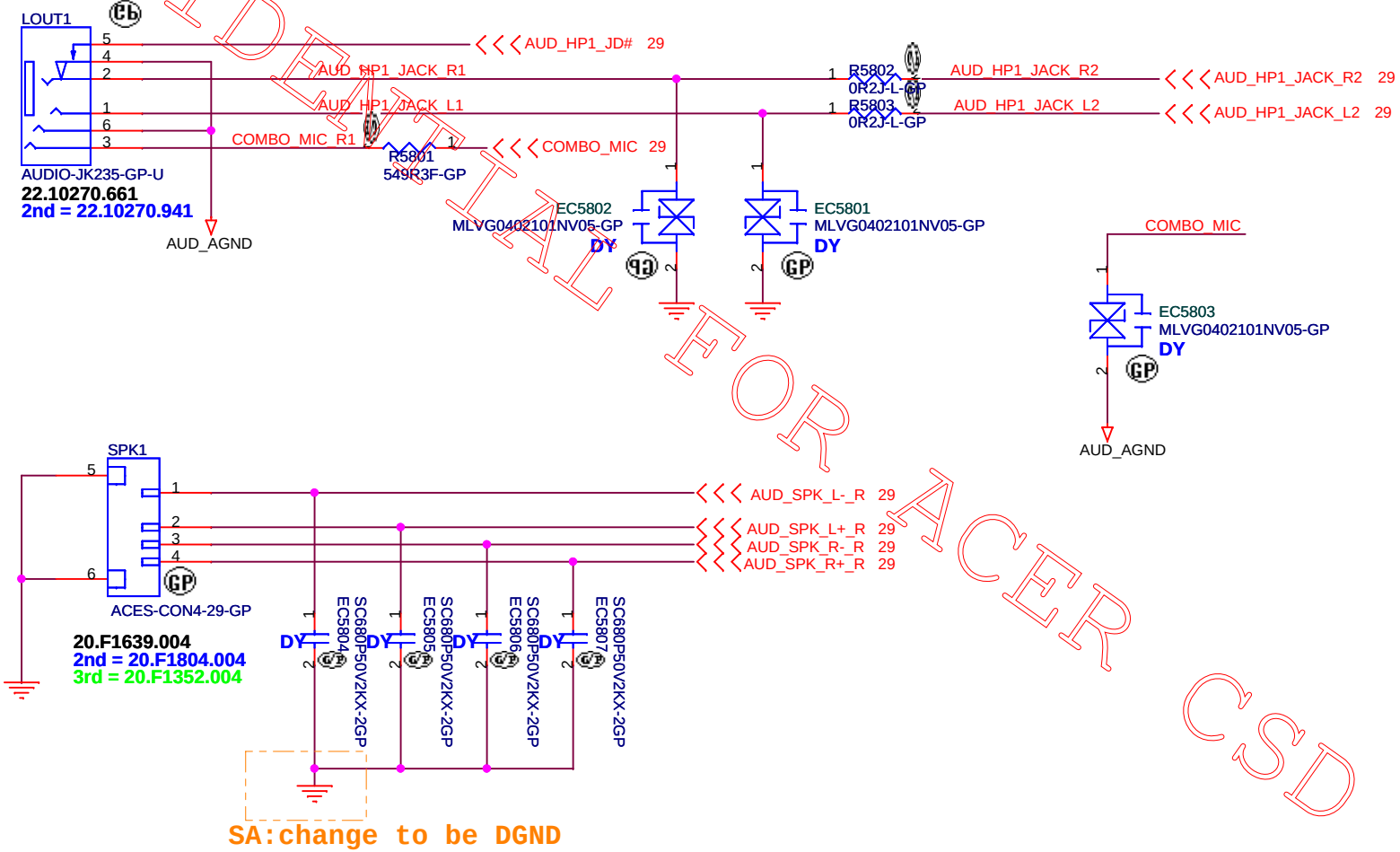
Title: E-SATA/USB CHARGER

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 57 of 103

SSID = AUDIO



<Core Design>

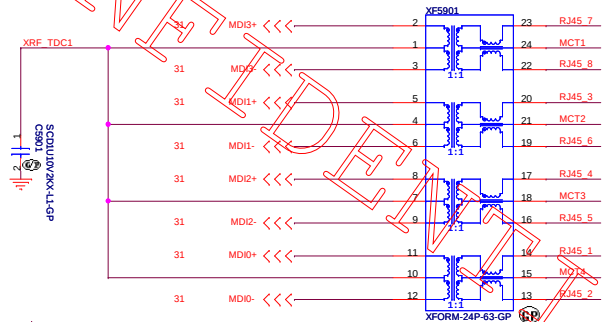
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

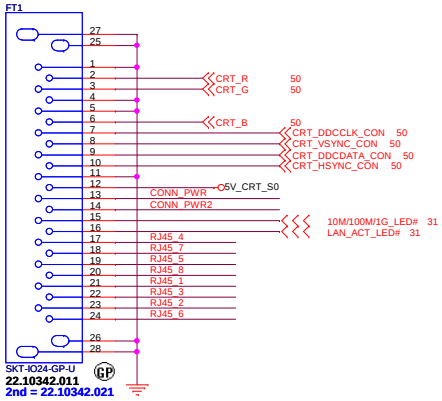
Title: ***Audio Jack***

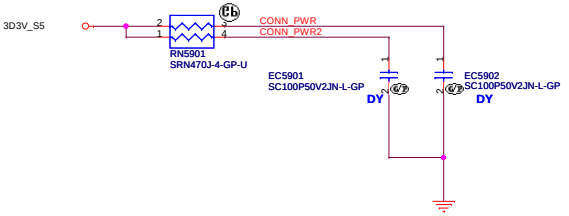
Size	Document Number	Rev
A4	Petra Uma	-1

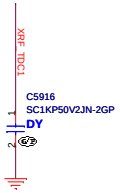
Date: Tuesday, July 10, 2012 Sheet 58 of 103

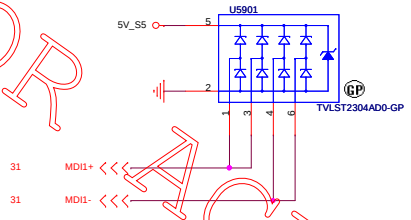
SSID = LAN

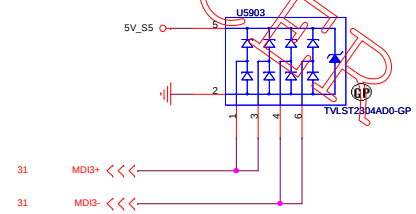


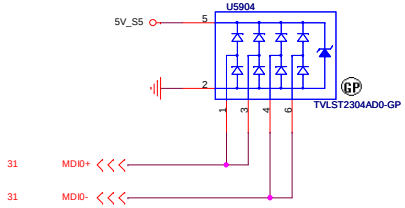


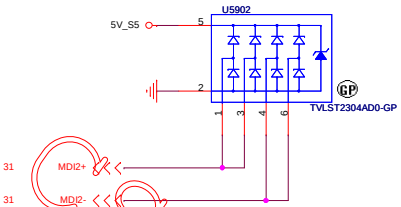


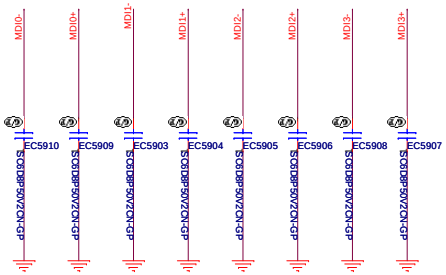


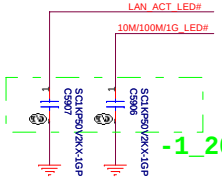




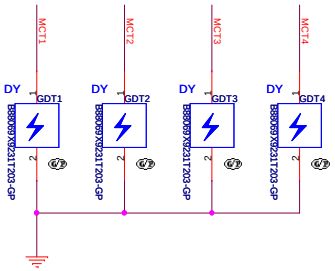


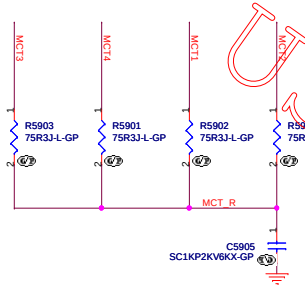






-1_20120301





<Core Design>
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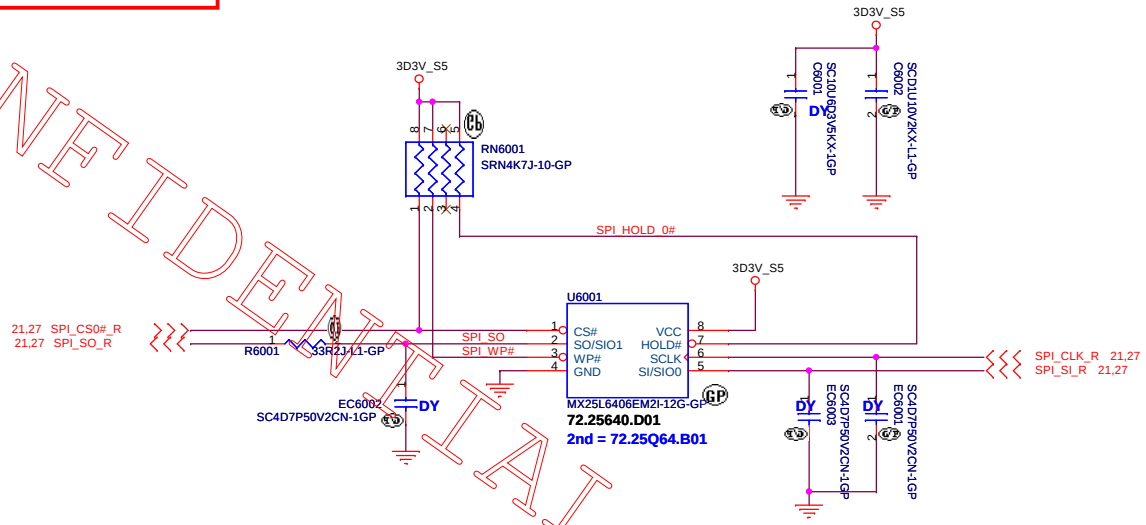
Title: LAN CONNECTOR

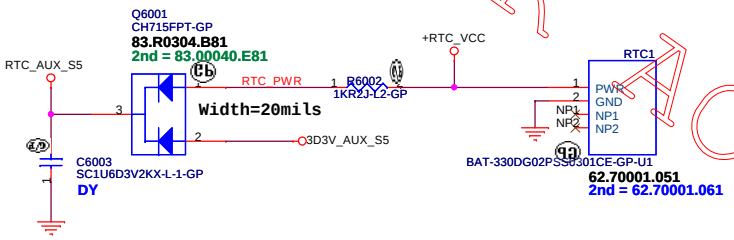
Size	Document Number	Rev
Custom	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



<Core Design>

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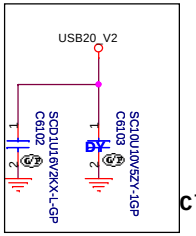
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash/RTC***

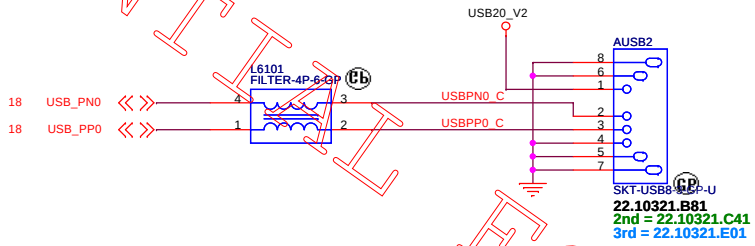
Size: Custom | Document Number: **Petra Uma** | Rev: **-1**

Date: Tuesday, July 10, 2012 | Sheet 60 of 103

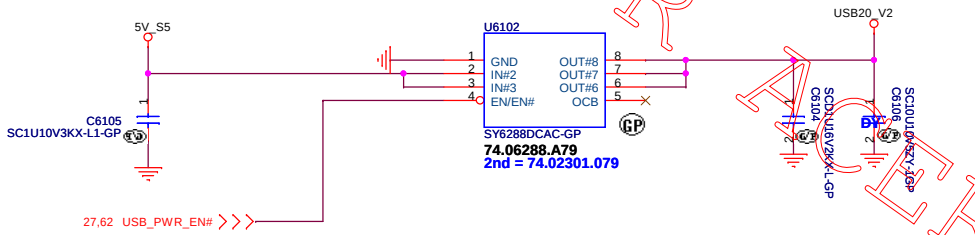
SSID = USB

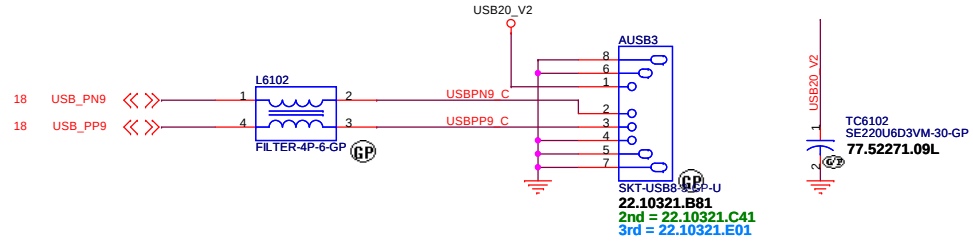


Close to AUSB2



Low Active 2A





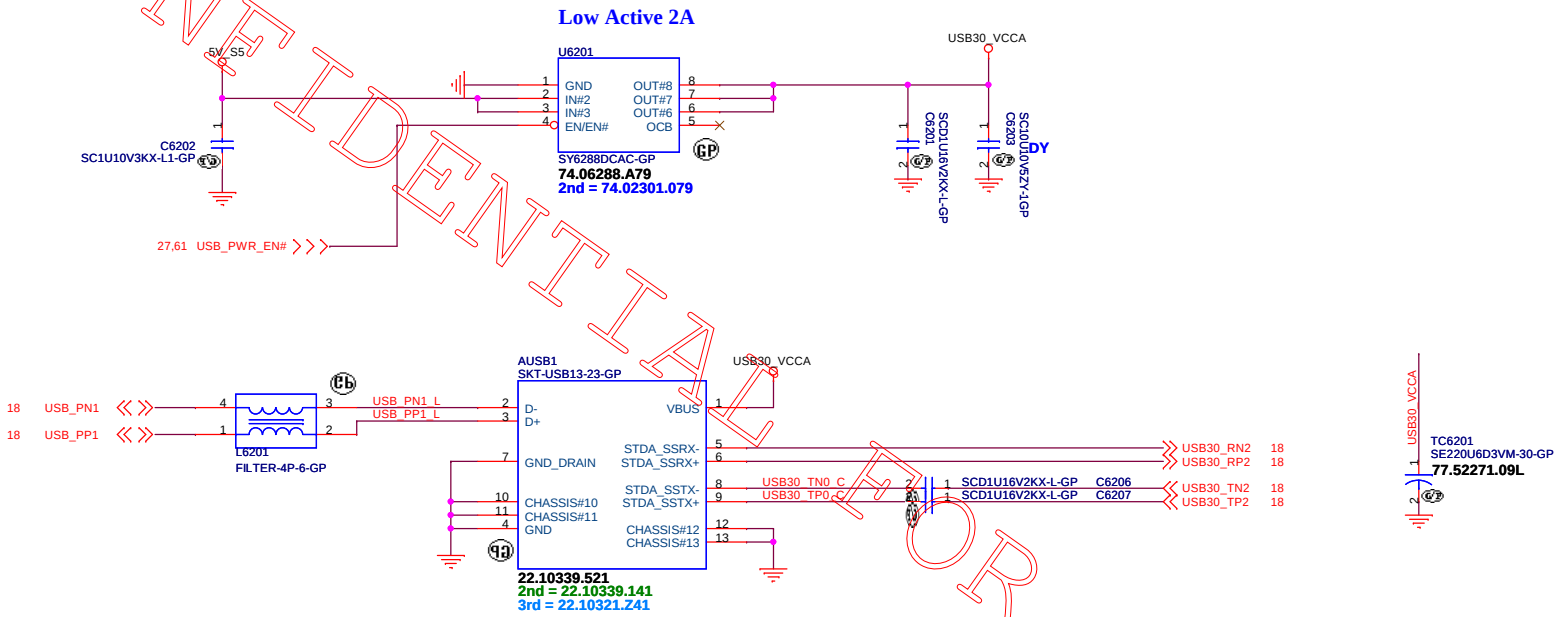
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

緯創資通 Wistron Corporation
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Title: USB 3.0 Port

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 62 of 103

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Bluetooth*

Size: A4 | Document Number: Petra Uma | Rev: -1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

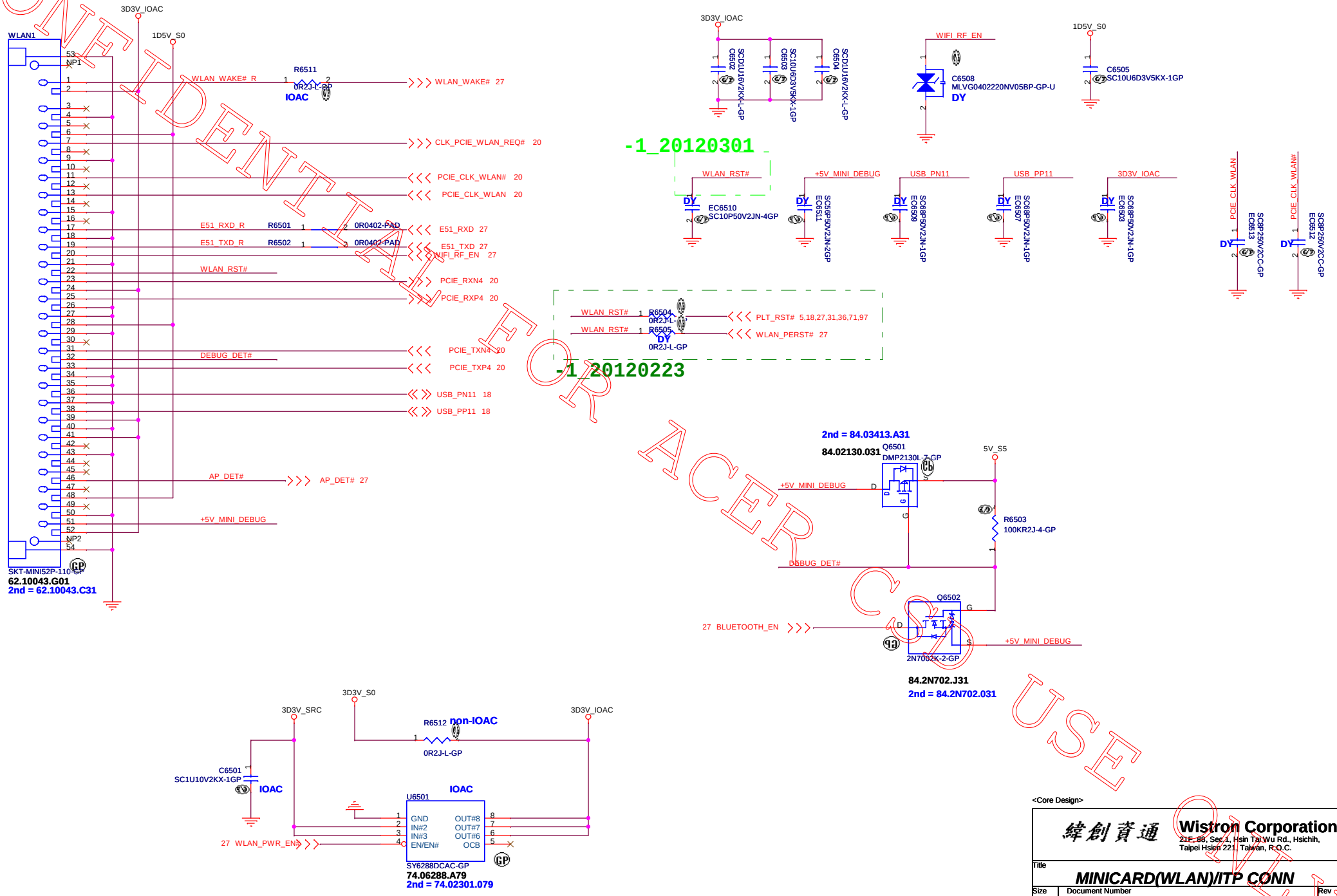
Title: ***RESERVED***

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 66 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

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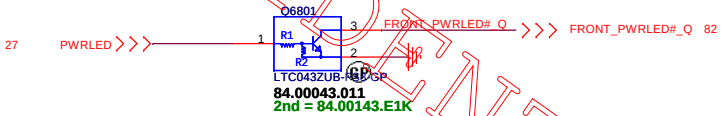
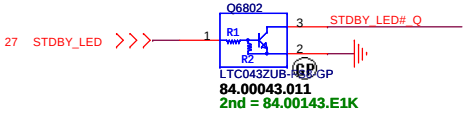
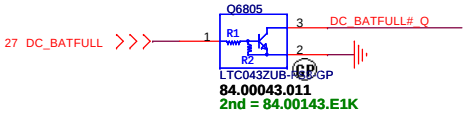
Power button LED



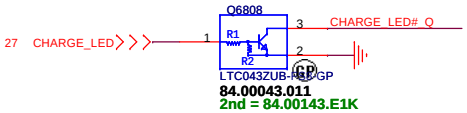
Power STDBY_LED

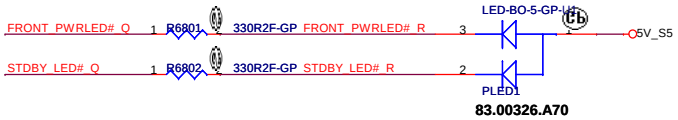


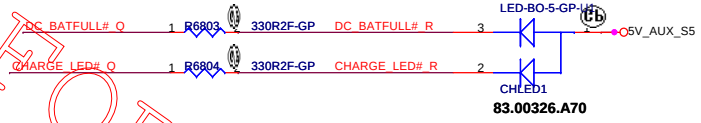
Battery LED2(DC_BATFULL)

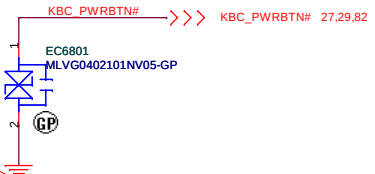


Battery LED1(CHARGE)









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: LED Bard/Power Button

Size	Document Number	Rev
Custom	Petra Uma	-1

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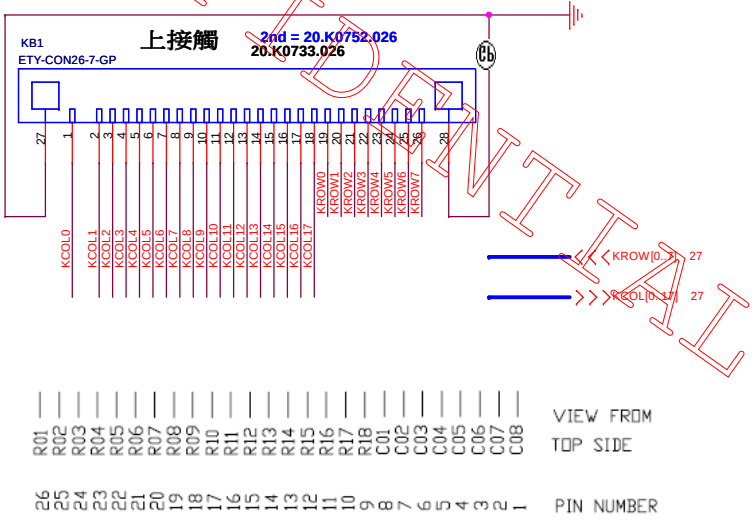
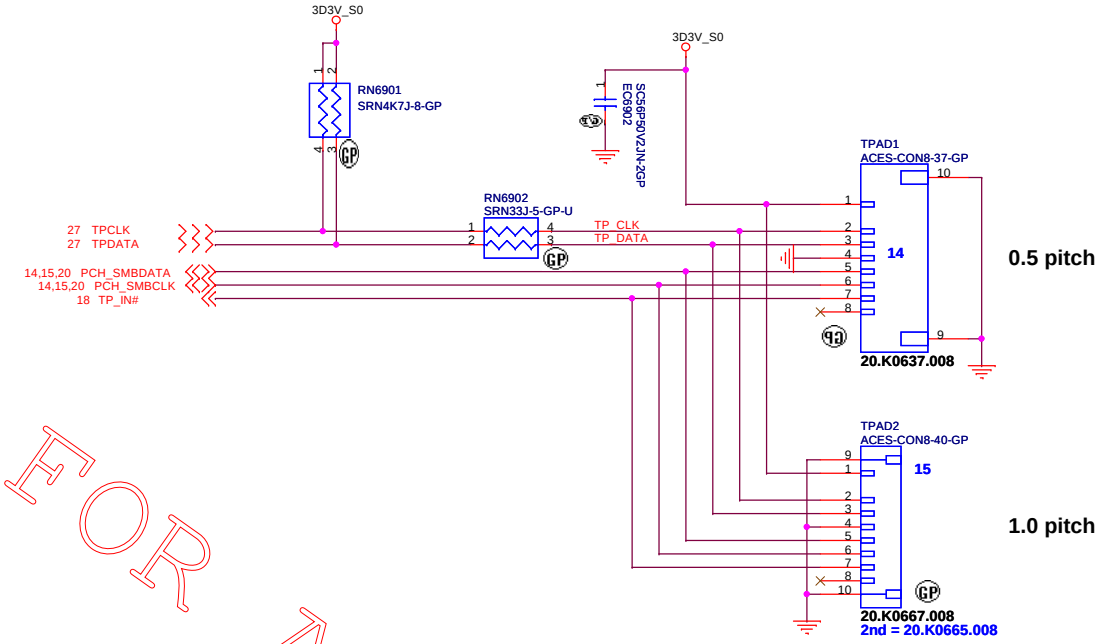
SSID = KBC

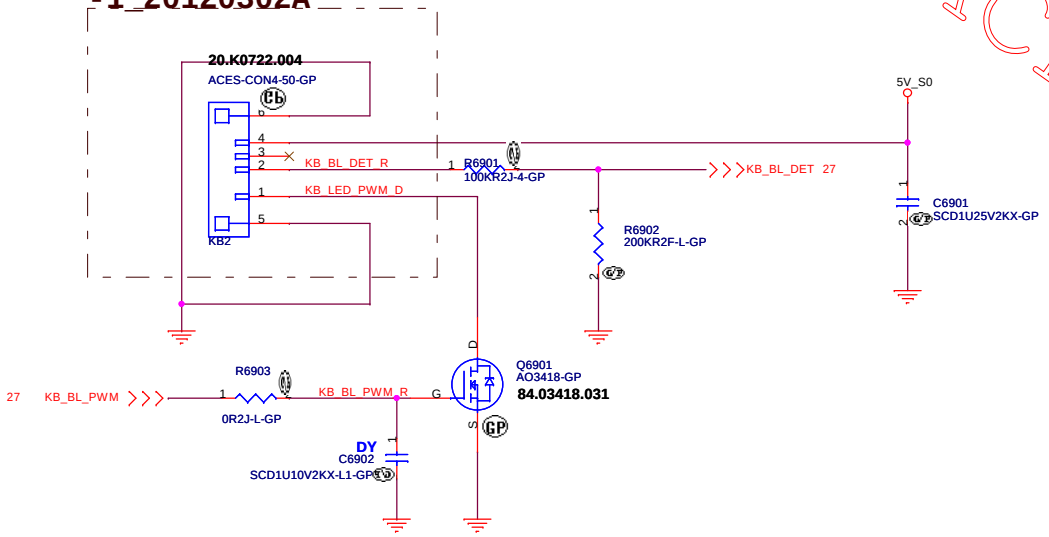
Internal KeyBoard Connector



TOUCH PAD



-1_20120302A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Petra Uma | Rev: -1

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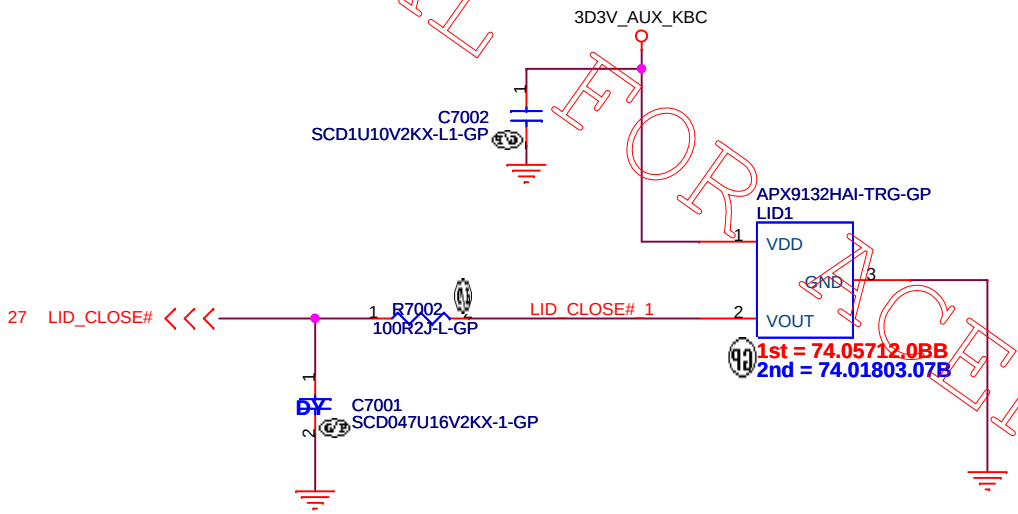

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Petra Uma**	-1

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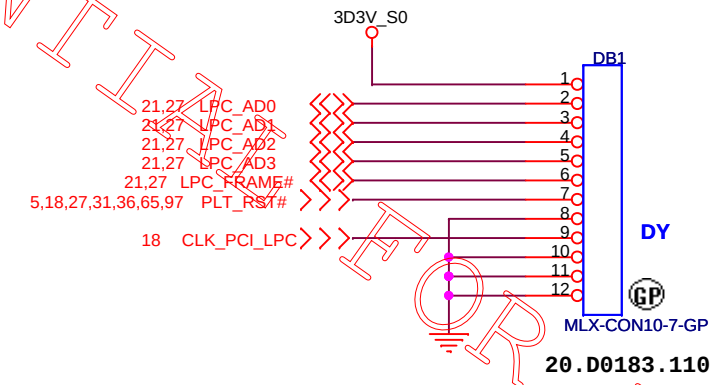

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Petra Uma**	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 72 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

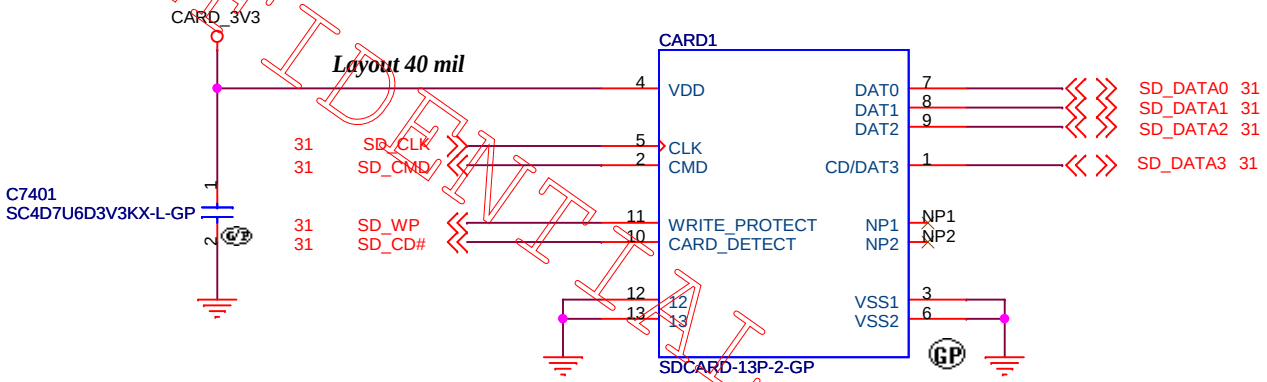
Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	-1

Date: Wednesday, February 22, 2012 Sheet 73 of 103

SD/MMC Card Reader

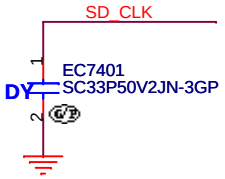
SSID = SDIO



62.10051.C41

2nd = 62.10051.D71

BCM57765/BCM57785 Pin Number	*Signal Name*	*SD/MMC Interface*	*MS-Pro Interface*	*xD Interface*
21	CR_CLK/RY_BY#	CR_CLK	MS_CLK	RY_BY#
26	CR_CMD/CLE	CR_CMD	MS_BS	CLE
25	CR_DATA0	CR_DATA0	MS_DATA0	XD_DATA0
24	CR_DATA1	CR_DATA1	MS_DATA1	XD_DATA1
23	CR_DATA2	CR_DATA2	MS_DATA2	XD_DATA2
22	CR_DATA3	CR_DATA3	MS_DATA3	XD_DATA3
52	CR_DATA4	CR_DATA4	MS_DATA4	XD_DATA4
53	CR_DATA5	CR_DATA5	MS_DATA5	XD_DATA5
54	CR_DATA6	CR_DATA6	MS_DATA6	XD_DATA6
55	CR_DATA7	CR_DATA7	MS_DATA7	XD_DATA7
60	ALE	–	–	ALE
1	SD_DETECT/WE#	CR_DETECT	–	WE#
9	RE#	–	–	RE#
59	CE#/MS_INS#	–	MS_INS#	CE#
57	CR_WP#/XD_WP#	SD_WP#	–	WP#
68	XD_DETECT	–	–	XD_DETECT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size: A4 | Document Number: **Petra Uma** | Rev: **-1**

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *New Card*

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 75 of 103

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	**Petra Uma**	-1

Date: Wednesday, February 22, 2012 Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

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Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

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Title: G- Sensor

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 79 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

緯創資通 Wistron Corporation
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Title: ***Reserved***

Size	Document Number	Rev
A4	Petra Uma	-1

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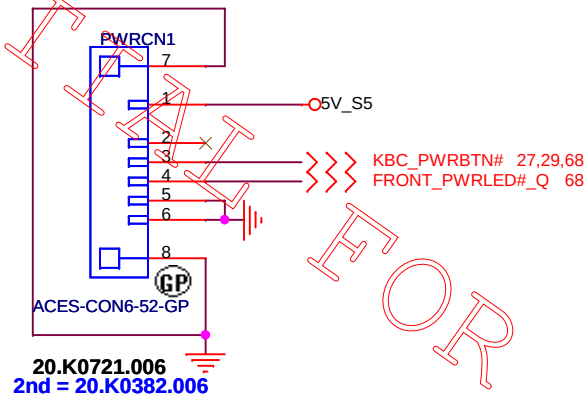

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208F_+VGA_CORE

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A4	Petra Uma	-1

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LVDS Channel A

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Panel BL brightness/Power En/BL En

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size: A4 | Document Number: Petra Uma | Rev: -1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CRT_Switch

Size: A4 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 95 of 103

SSID = SDIO

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<Core Design>

緯創資通 Wistron Corporation
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Title: TOUCH PANEL

Size	Document Number	Rev
A4	Petra Uma	-1

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H1 HOLE355X355R111-S1-GP
H2 HOLE355X355R111-S1-GP
H3 HOLE355X355R111-S1-GP
H4 HOLE355X355R111-S1-GP
H6 HOLE335R115-GP
H5 HOLE355X355R111-S1-GP
H10 HOLE335R115-GP
H11 HOLE335R115-GP
H12 HOLE335R115-GP

CPU
HS3 STF237R128H41-GP 34.4TU18.001 2nd = 34.4TU18.101
HS2 STF237R128H41-GP 34.4TU18.001 2nd = 34.4TU18.101
HS1 STF237R128H41-GP 34.4TU18.001 2nd = 34.4TU18.101

EC change

Check test point

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
19,27 PM_PWRBTN#	AFTP10
5,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
5,18,27,31,36,65,71 PLT_RST#	AFTP13

Test Point放在Dimm Door打開可量測處

1D05V_VTT
EC9705 SCD1U10V2KX-L1-GP
EC9706 SCD1U10V2KX-L1-GP

AD_JK
EC9716 SCD1U50V3KX-GP

DCBATOUT
EC9715 SCD1U50V3KX-GP
EC9714 SCD1U50V3KX-GP
EC9701 SCD1U50V3KX-GP

DCBATOUT_2
EC9702 SCD1U50V3KX-GP
EC9707 SCD1U50V3KX-GP
EC9723 SCD1U50V3KX-GP
EC9722 SCD1U50V3KX-GP
EC9721 SCD1U50V3KX-GP

PWR_VCCCORE1_DCBATOUT
EC9704 SCD1U50V3KX-GP

3D3V_S0
EC9708 SCD1U10V2KX-L1-GP

EC9728 MLVG0402101NV05-GP
EC9729 MLVG0402101NV05-GP
AUD_AGND

1D5V_S3
EC9711 SCD1U10V2KX-L1-GP
EC9712 SCD1U10V2KX-L1-GP
EC9713 SCD1U10V2KX-L1-GP

5V_S0
EC9717 SCD1U10V2KX-L1-GP
EC9718 SCD1U10V2KX-L1-GP
EC9719 SCD1U10V2KX-L1-GP
EC9720 SCD1U10V2KX-L1-GP

5V_S5
EC9725 SCD1U10V2KX-L1-GP

-1_20120301

-1_20120301

BT+
EC9730 SCD1U50V3KX-GP
EC9731 SCD1U50V3KX-GP

DCBATOUT
EC9732 SCD1U50V3KX-GP

LCDVDD
EC9726 SCD1U10V2KX-L1-GP

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Petra Uma
Rev: -1
Date: Tuesday, July 10, 2012
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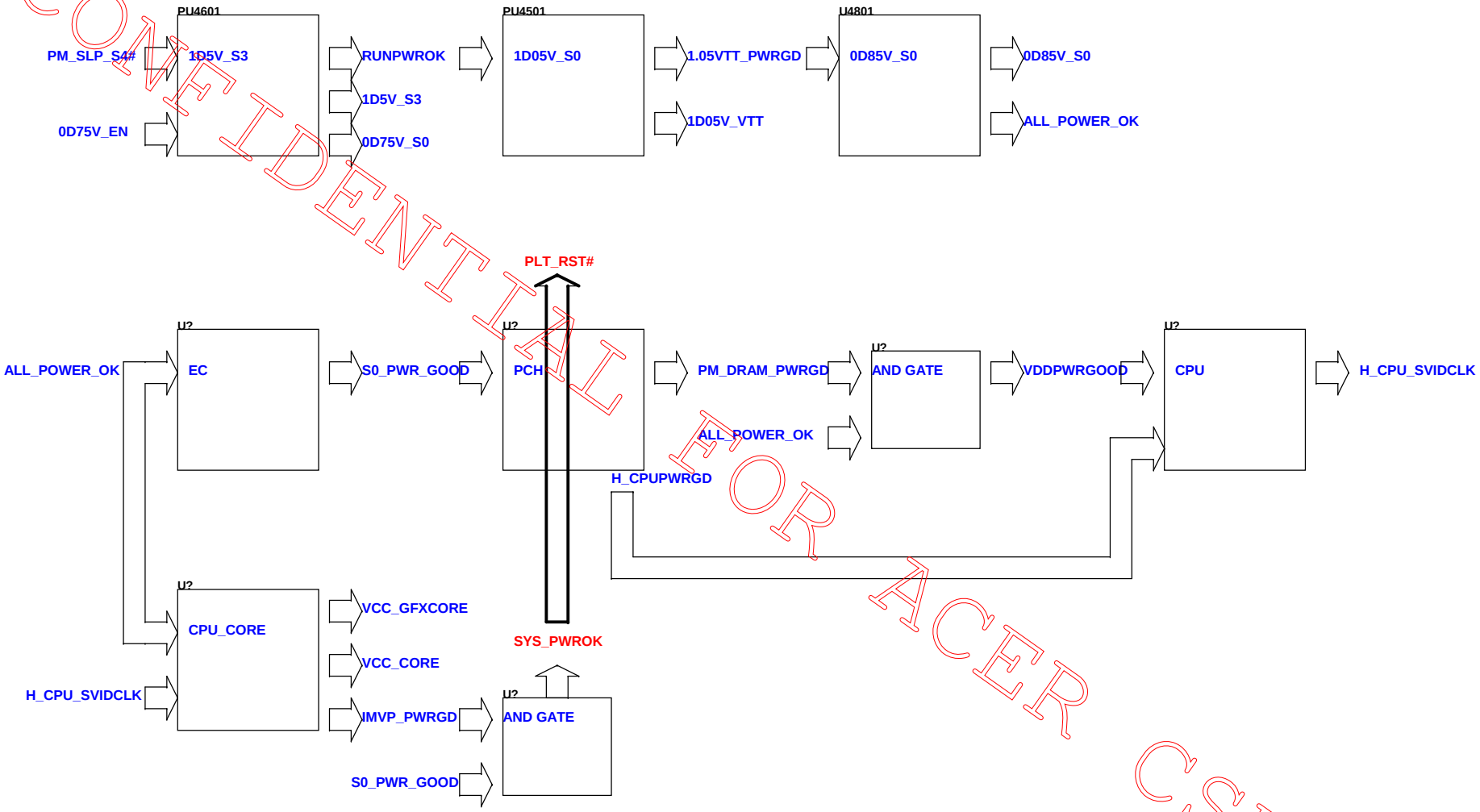
Power Sequence



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Change History

Size: A3 | Document Number: Petra Uma | Rev: -1

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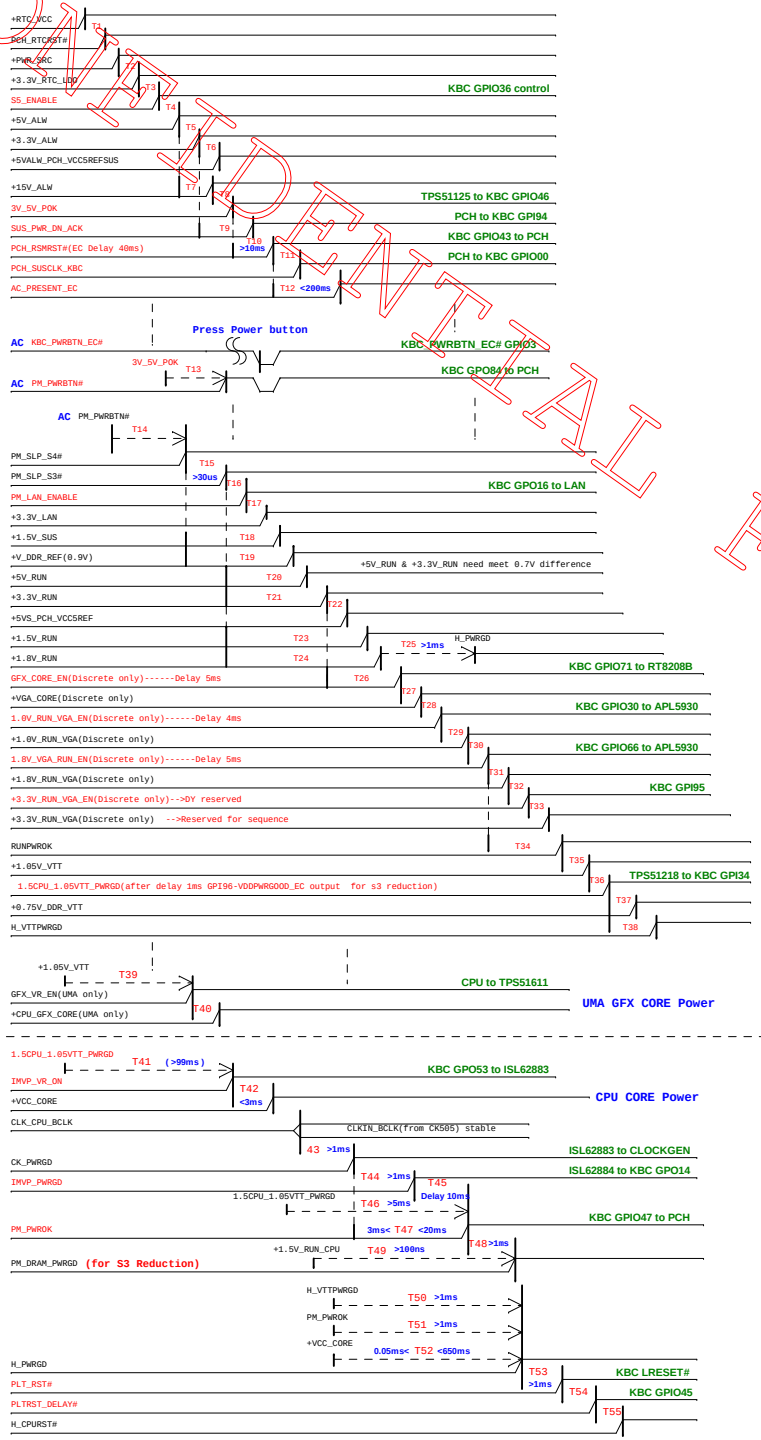
Intel-Power Up Sequence

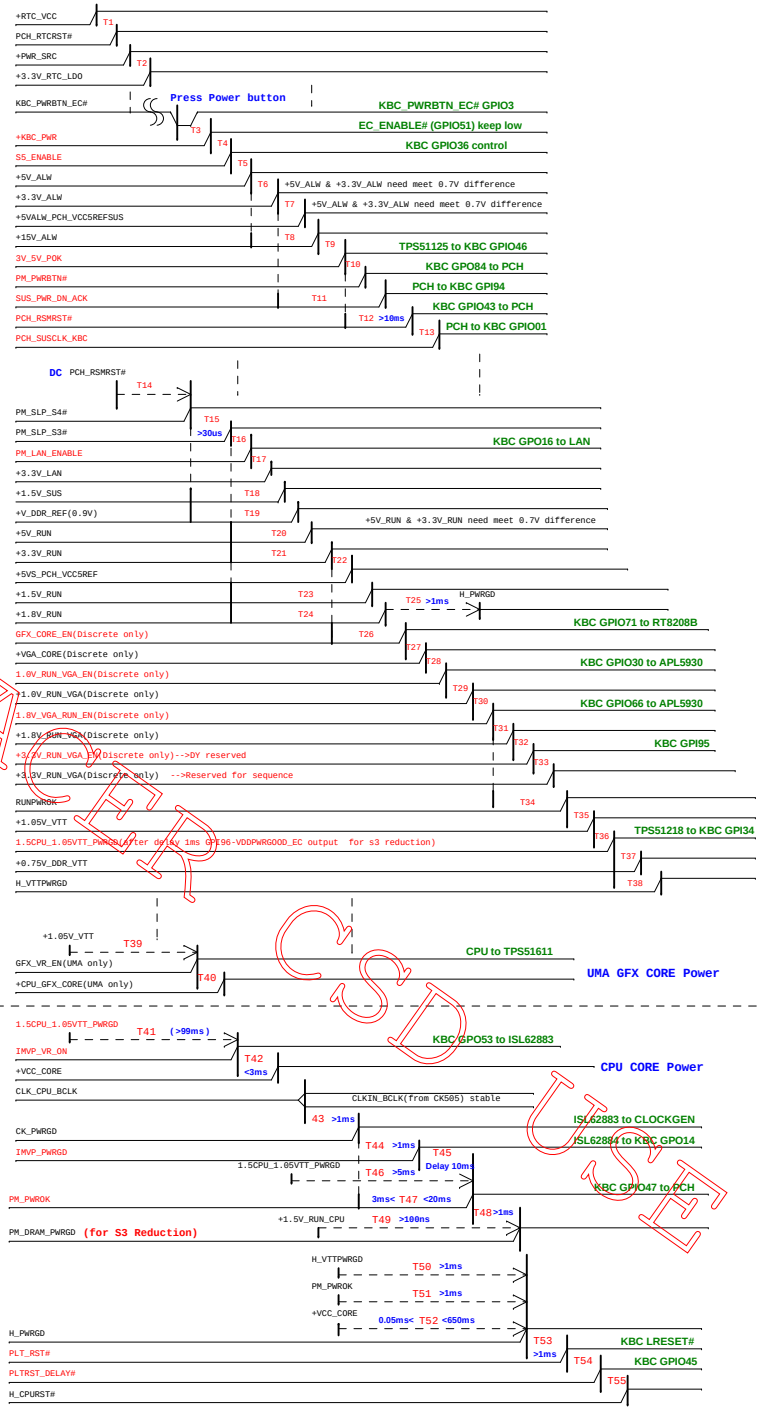
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>
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Title: Power Sequence

Size	Document Number	Rev
A1	Petra Uma	-1

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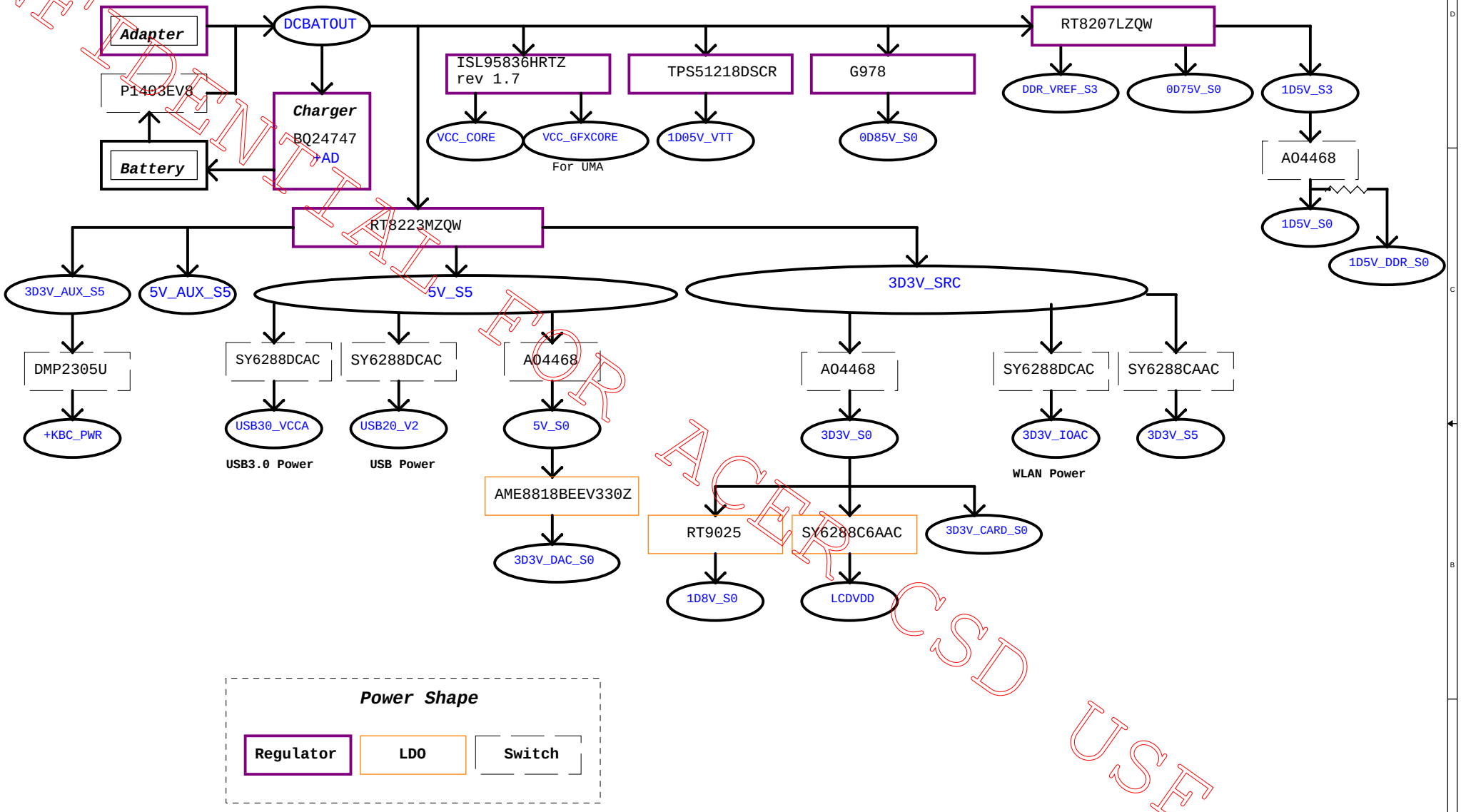

<Core Design>

緯創資通 Wistron Corporation
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Title: Power Block Diagram

Size	Document Number	Rev
A3	Petra Uma	-1

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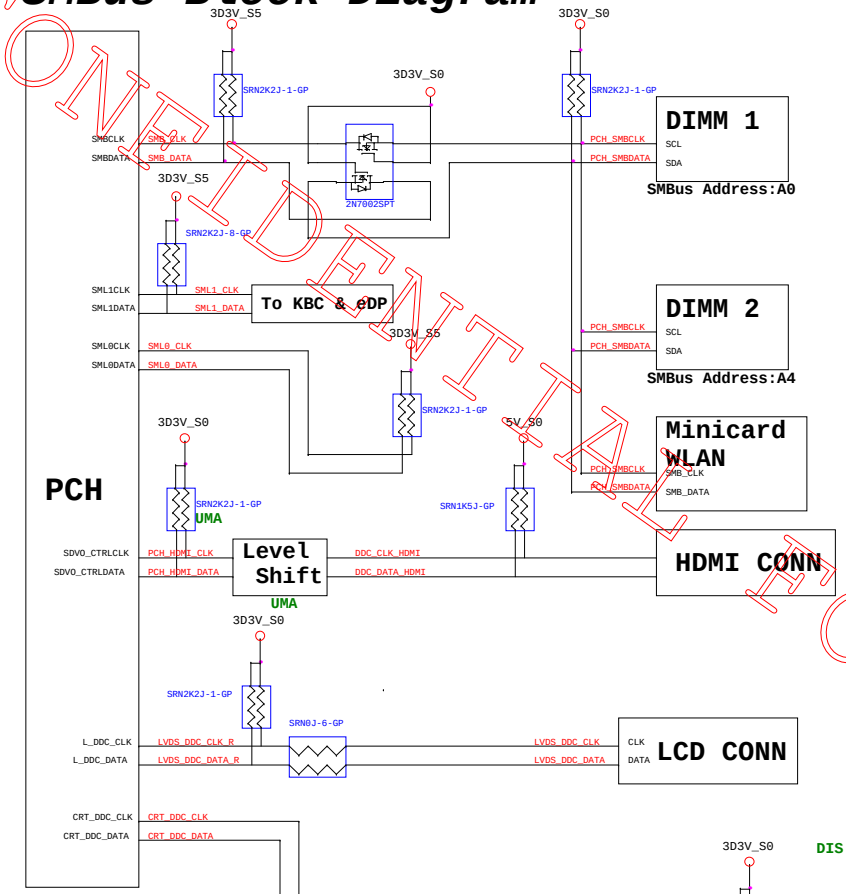
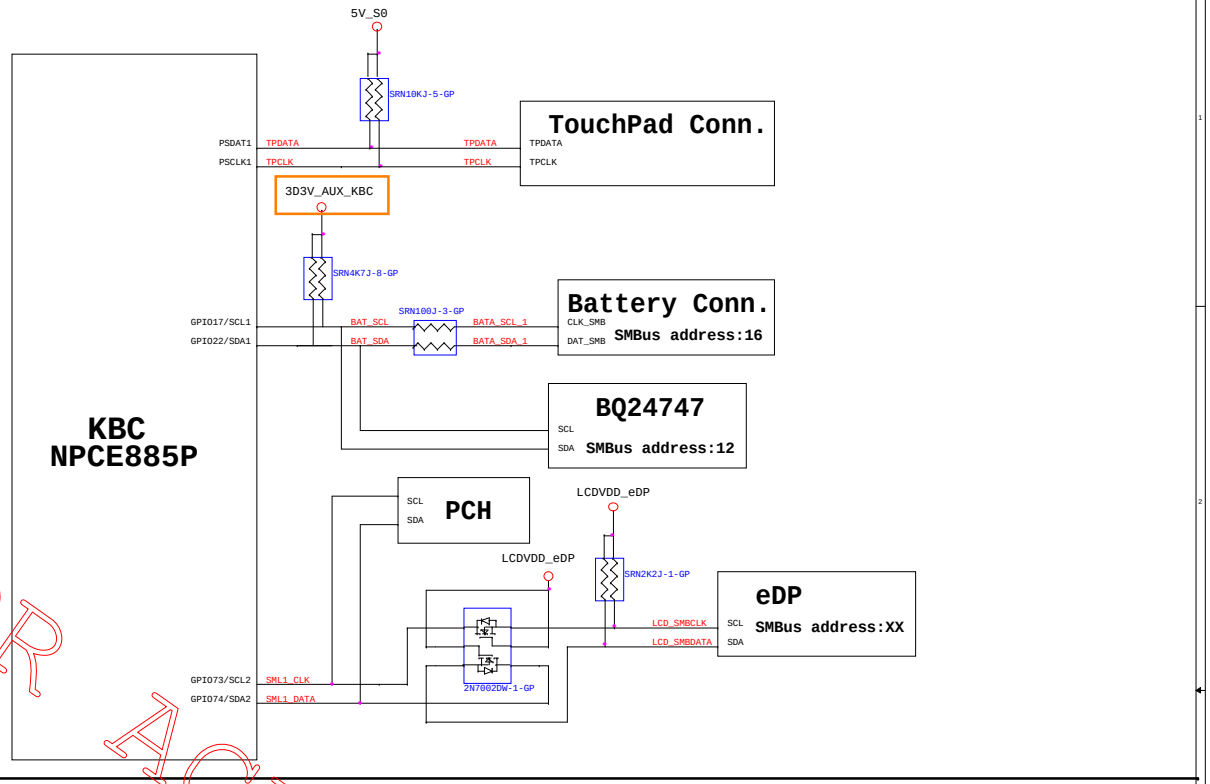
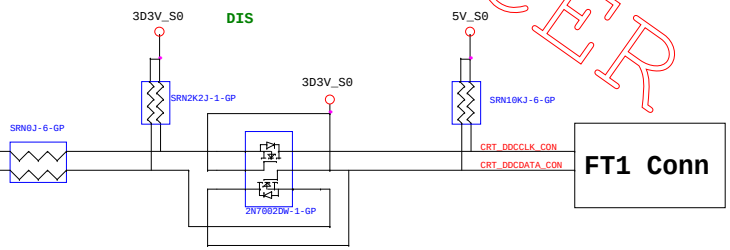
PCH SMBus Block Diagram



KBC SMBus Block Diagram





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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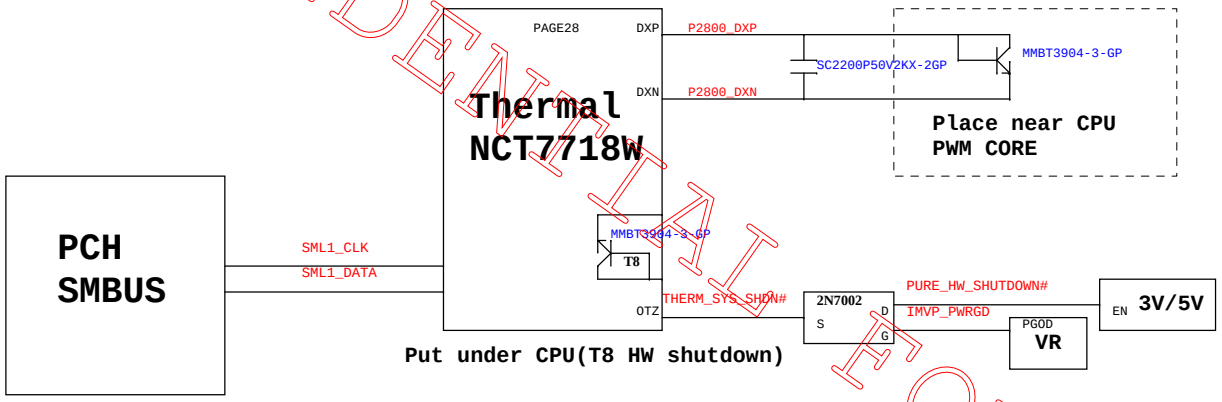
Title: SMBUS Block Diagram

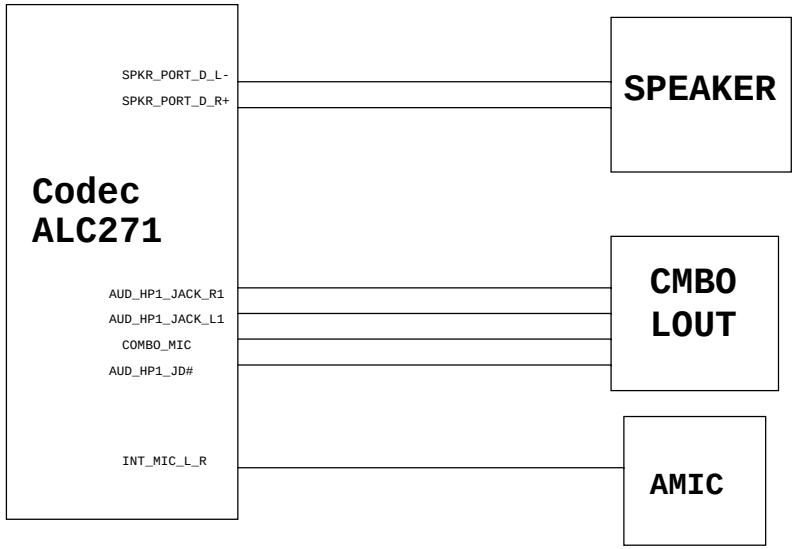
Size	Document Number	Rev
A2	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram



<Core Design>

緯創資通 Wistron Corporation
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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 102 of 103

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<Core Design>

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Title: ***USB charger***

Size	Document Number	Rev
A4	Petra Uma	-1

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