Husk/Petra
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

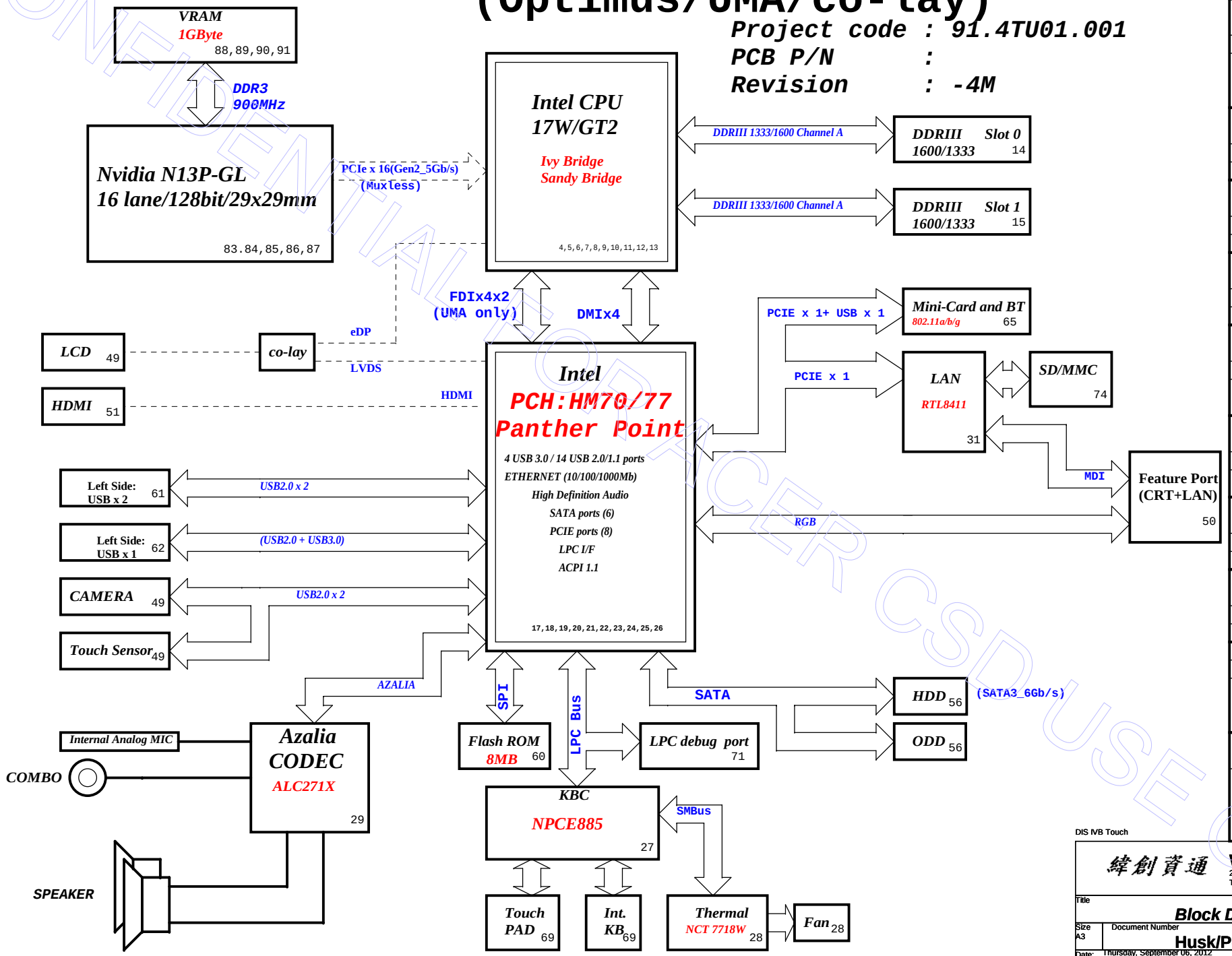
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page
Size: A3 | Document Number: Husk/Petra | Rev: -4M
Date: Thursday, September 06, 2012 | Sheet 1 of 103

Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -4M



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Husk/Petra | Rev: -4M
Date: Thursday, September 06, 2012 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

DIS IVB Touch

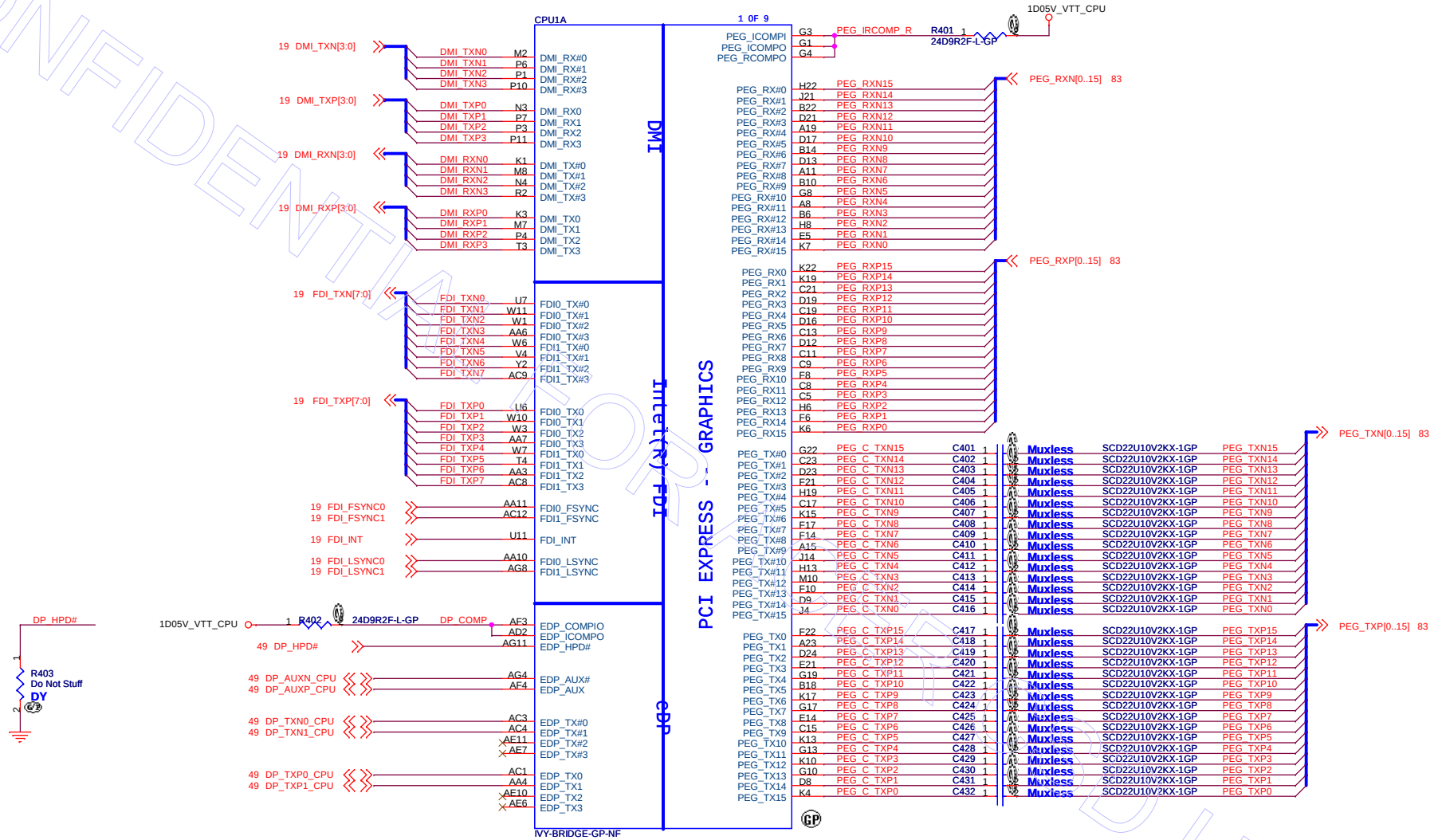
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 3 of 103

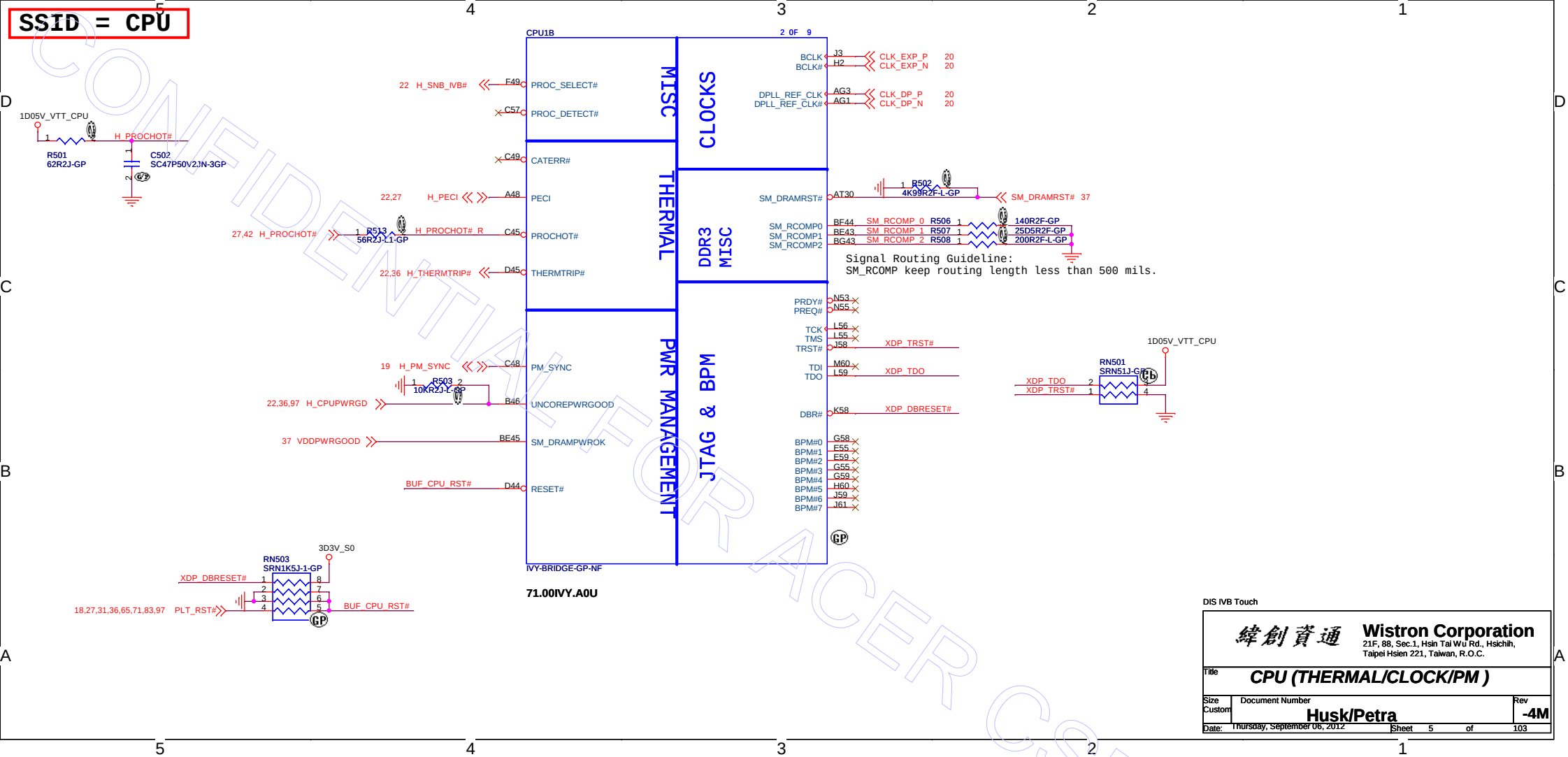
SSID = CPU



DIS IVB Touch

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (PCIE/DMI/FDI)
Size A3	Husk/Petra
Rev	-4M
Date: Thursday, September 06, 2012	Sheet 4 of 103

SSID = CPU



DIS IVB Touch

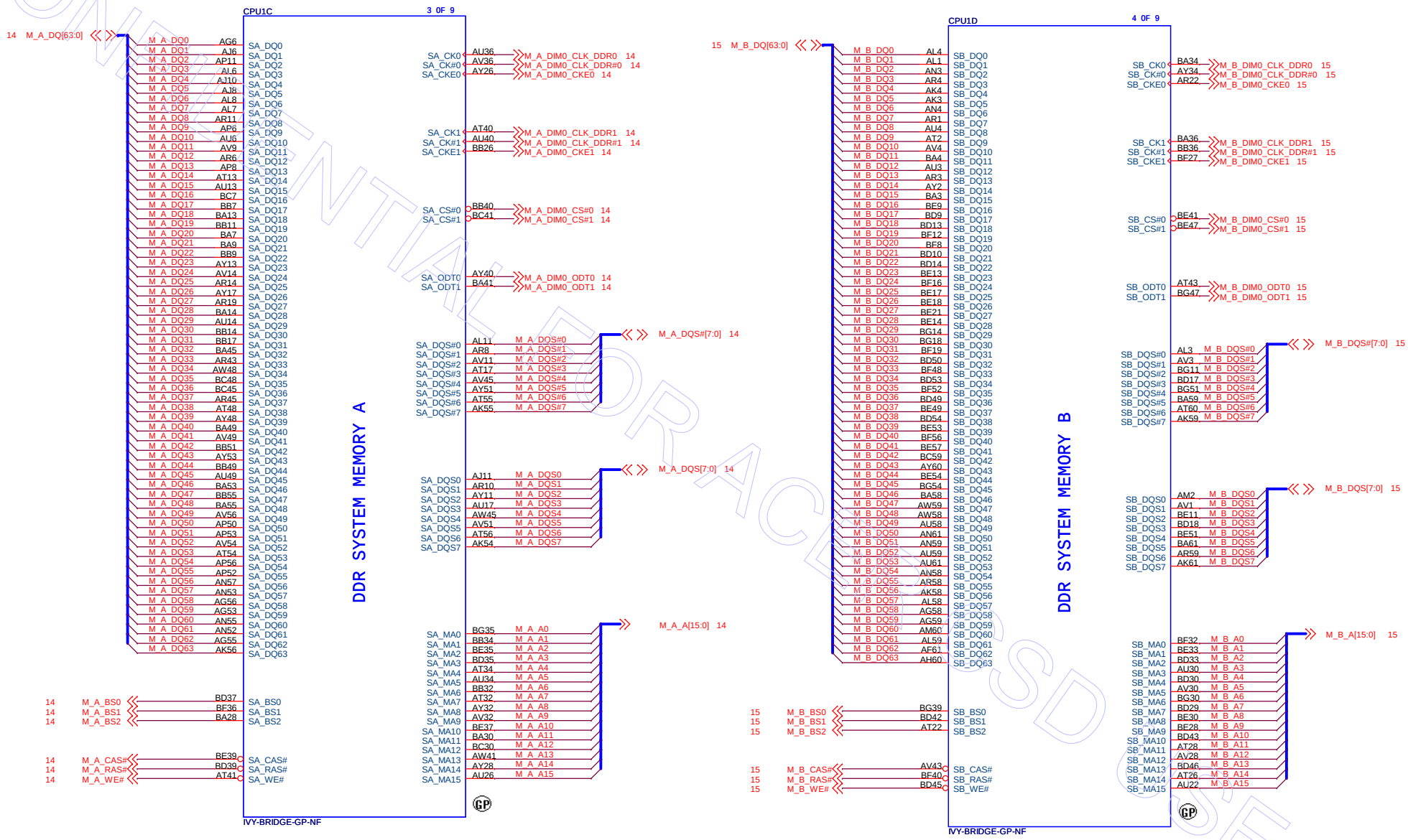
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 5 of 103

SSID = CPU



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 6 of 103

SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG2
R702
1KR2J-L2-GP
Muxless

Enabl EDP function	
CFG4	1:Disable 0:Enable

CFG4
R703
1KR2J-L2-GP
EDP

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5
R704
Do Not Stuff
DY

CFG6
R705
Do Not Stuff
DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7
R706
Do Not Stuff
DY

Do Not Stuff TP701 1 CFG0_TP
Do Not Stuff TP702 1 CFG1_TP
CFG2
Do Not Stuff TP703 1 CFG3_TP
CFG4
CFG5
CFG6
CFG7

CPU1E
5 OF 9

B50	CFG0		BCLK_ITP	N59	
C51	CFG1		BCLK_ITP#	N58	
B54	CFG2				
D53	CFG3				
A51	CFG4		RSVD30	N42	
C53	CFG5		RSVD31	L42	
C55	CFG6		RSVD32	L45	
H49	CFG7		RSVD33	L47	
A55	CFG8				
H51	CFG9				
K49	CFG10		RSVD34	M13	
K53	CFG11		RSVD35	M14	
F53	CFG12		RSVD36	U14	
G53	CFG13		RSVD37	W14	
L51	CFG14		RSVD38	P13	
F51	CFG15				
D52	CFG16				
L53	CFG17		RSVD39	AT49	
			RSVD40	K24	
H43	VCC_VAL_SENSE				
K43	VSS_VAL_SENSE		RSVD41	AH2	
			RSVD42	AG13	
H45	VAXG_VAL_SENSE		RSVD43	AM14	
K45	VSSAXG_VAL_SENSE		RSVD44	AM15	
			RSVD45	N50	
F48	VCC_DIE_SENSE				
G48	RSVD47				
H48	RSVD6				
K48	RSVD7				
			DC_TEST_A4	A4	
			DC_TEST_C4	C4	
BA19	RSVD8		DC_TEST_D3	D3	
AV19	RSVD9		DC_TEST_D1	D1	
AT21	RSVD10		DC_TEST_A58	A58	
BB21	RSVD11		DC_TEST_A59	A59	
BB19	RSVD12		DC_TEST_C59	C59	
AY21	RSVD13		DC_TEST_A61	A61	
BA22	RSVD14		DC_TEST_C61	C61	
AY22	RSVD15		DC_TEST_D61	D61	
AU19	RSVD16		DC_TEST_BD61	BD61	
AU21	RSVD17		DC_TEST_BE61	BE61	
BD21	RSVD18		DC_TEST_BE59	BE59	
BD22	RSVD19		DC_TEST_BG61	BG61	
BD25	RSVD20		DC_TEST_BG59	BG59	
BD26	RSVD21		DC_TEST_BG58	BG58	
BG22	RSVD22		DC_TEST_BG4	BG4	
BE22	RSVD23		DC_TEST_BG3	BG3	
BG26	RSVD24		DC_TEST_BE3	BE3	
BE26	RSVD25		DC_TEST_BG1	BG1	
BF23	RSVD26		DC_TEST_BE1	BE1	
BE24	RSVD27		DC_TEST_BD1	BD1	

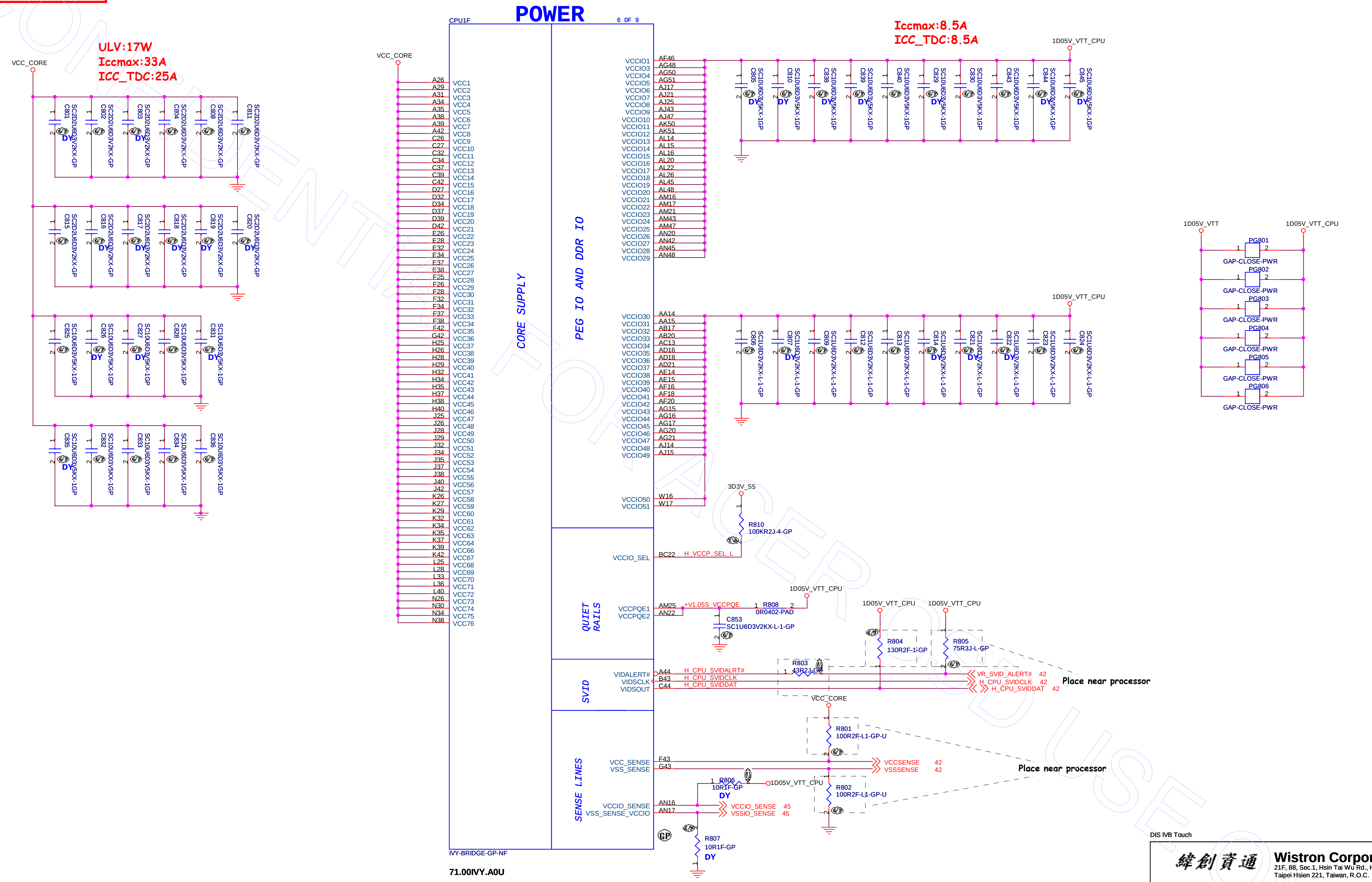
RESERVED
GP
IVY-BRIDGE-GP-NF
71.00IVY.A0U

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)
Size: A3
Document Number: Husk/Petra
Rev: -4M
Date: Thursday, September 06, 2012
Sheet 7 of 103

SSID = CPU



DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU (VCC_CORE)**
Size: Custom; Document Number: **Husk/Petra**	Rev: **-4M**
Date: Monday, September 17, 2012	Sheet 8 of 103

SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

CPU1G 7 OF 9

VCC_GFXCORE

SC10U6D3V5KX-1GP C902 C903 C904 C905 C908 C919 C920 C921 (DY)

SC1U6D3V2KX-1-GP C907 C909 C914 C916 (DY)

VAXG1 AA46
VAXG2 AB47
VAXG3 AB50
VAXG4 AB51
VAXG5 AB52
VAXG6 AB53
VAXG7 AB55
VAXG8 AB56
VAXG9 AB58
VAXG10 AB59
VAXG11 AC61
VAXG12 AD47
VAXG13 AD48
VAXG14 AD50
VAXG15 AD51
VAXG16 AD52
VAXG17 AD53
VAXG18 AD55
VAXG19 AD56
VAXG20 AD58
VAXG21 AD59
VAXG22 AE46
VAXG23 N45
VAXG24 P47
VAXG25 P48
VAXG26 P50
VAXG27 P51
VAXG28 P52
VAXG29 P53
VAXG30 P55
VAXG31 P56
VAXG32 P61
VAXG33 T49
VAXG34 T58
VAXG35 T59
VAXG36 T61
VAXG37 U46
VAXG38 V47
VAXG39 V48
VAXG40 V50
VAXG41 V51
VAXG42 V52
VAXG43 V53
VAXG44 V55
VAXG45 V56
VAXG46 V58
VAXG47 V59
VAXG48 W50
VAXG49 W51
VAXG50 W52
VAXG51 W53
VAXG52 W55
VAXG53 W56
VAXG54 W61
VAXG55 Y48
VAXG56 Y61

GRAPHICS

VREF

SM_VREF AY43 → +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ BE7
SB_DIMM_VREFDQ BG7

M_VREF_DQ_DIMM0_C → M_VREF_DQ_DIMM0_C 37
M_VREF_DQ_DIMM1_C → M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 SRN1KJ-7-GP DY

DDR3 - 1.5V RAILS

VDDQ1 AJ28
VDDQ2 AJ33
VDDQ3 AJ36
VDDQ4 AJ40
VDDQ5 AL30
VDDQ6 AL34
VDDQ7 AL38
VDDQ8 AL42
VDDQ9 AM33
VDDQ10 AM36
VDDQ11 AM40
VDDQ12 AN30
VDDQ13 AN34
VDDQ14 AN38
VDDQ15 AR26
VDDQ16 AR28
VDDQ17 AR30
VDDQ18 AR32
VDDQ19 AR34
VDDQ20 AR36
VDDQ21 AR40
VDDQ22 AV41
VDDQ23 AW26
VDDQ24 BA40
VDDQ25 BB28
VDDQ26 BG33

Iccmax:5A

1D5V_S0

SC10U6D3V5KX-1GP C910 C911 C912 C913 C918 C925 (DY)

SC1U6D3V2KX-1-GP C924 C917 C926 (DY)

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VCCD_Q AM28 AN26

1D5V_S0

R909 0R0402-PAD

C923 SC1U6D3V2KX-L-1-GP

QUIET RAILS

VCC_GFXCORE

R906 100R2F-L1-GP-U

R907 100R2F-L1-GP-U

R906,R907 close to CPU

VCC_AXG_SENSE
VSS_AXG_SENSE

42 VCC_AXG_SENSE F45
42 VSS_AXG_SENSE G45

VAXG_SENSE
VSSAXG_SENSE

SENSE LINES

1D8V_S0

ICC_MAX:1.2A

C922 SC1U10V2KX-1GP

VCCPLL1 BB3
VCCPLL2 BC1
VCCPLL3 BC4

1.8V RAIL

0D85V_S0

ICC_MAX:6A

C915 SC10U6D3V5KX-1GP

VCCSA1 L17
VCCSA2 L21
VCCSA3 N16
VCCSA4 N20
VCCSA5 N22
VCCSA6 P17
VCCSA7 P20
VCCSA8 R16
VCCSA9 R18
VCCSA10 R21
VCCSA11 U15
VCCSA12 V16
VCCSA13 V17
VCCSA14 V18
VCCSA15 V21
VCCSA16 W20

SA RAIL

VDDQ_SENSE BC43 TP_VDDQ_SENSE
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS

TP901 TPAD14-OP-GP
TP902 TPAD14-OP-GP

SENSE LINES

0D85V_S0

R902 100R2F-L1-GP-U

R902 need be close to pin U10.

VCCSA_SENSE U10 VCCSA_SENSE

VCCSA_VID0 D48 VCCSA_VID0
VCCSA_VID1 D49 VCCSA_VID1

VCCSA VID lines

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

1D05V_VTT_CPU 1D05V_VTT_CPU

R908 10KR2J-L-GP DY
R912 10KR2J-L-GP DY
R913 10KR2J-L-GP
R914 10KR2J-L-GP

VCCSA_VID0 VCCSA_VID1 → VCCSA_VID0 48, VCCSA_VID1 48

IVY-BRIDGE-GP-NF

71.00IVY.A0U

DIS IVB Touch

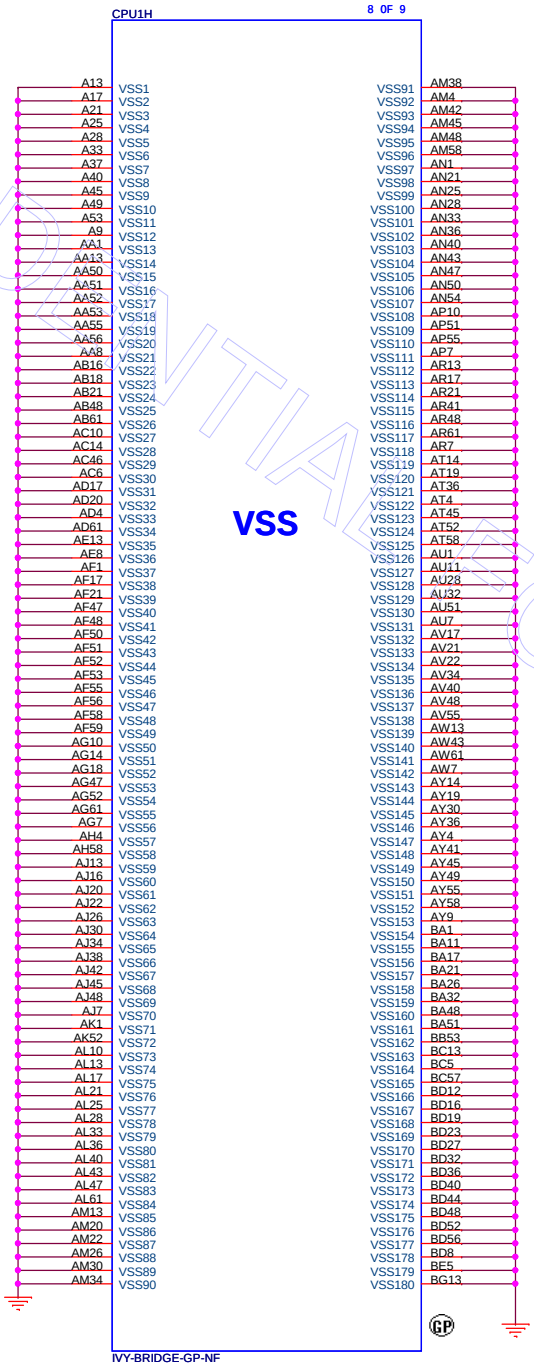
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

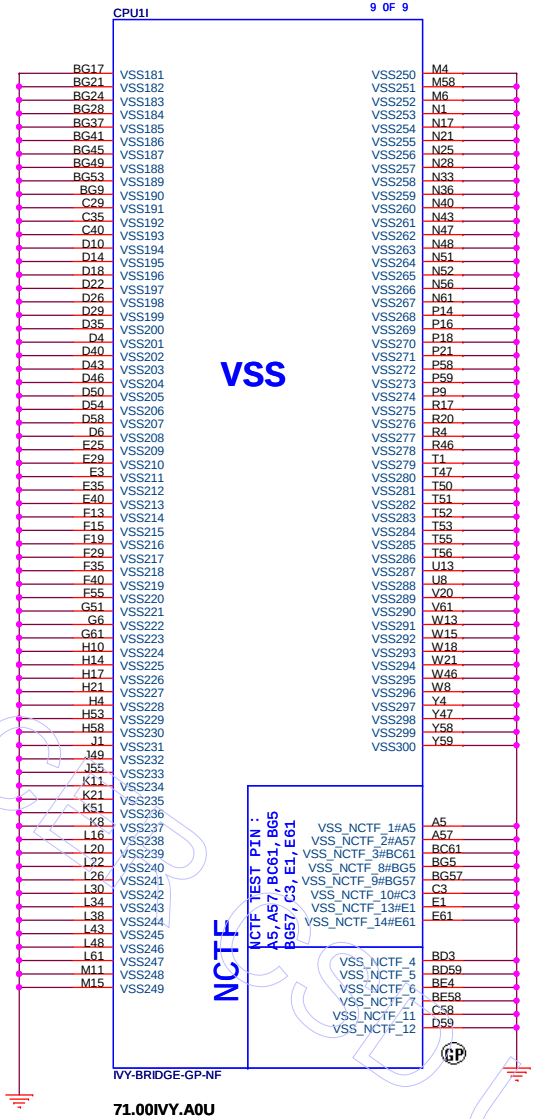
Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 9 of 103

SSID = CPU



71.00IVY.A0U



71.00IVY.A0U

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 10 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 11 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 12 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

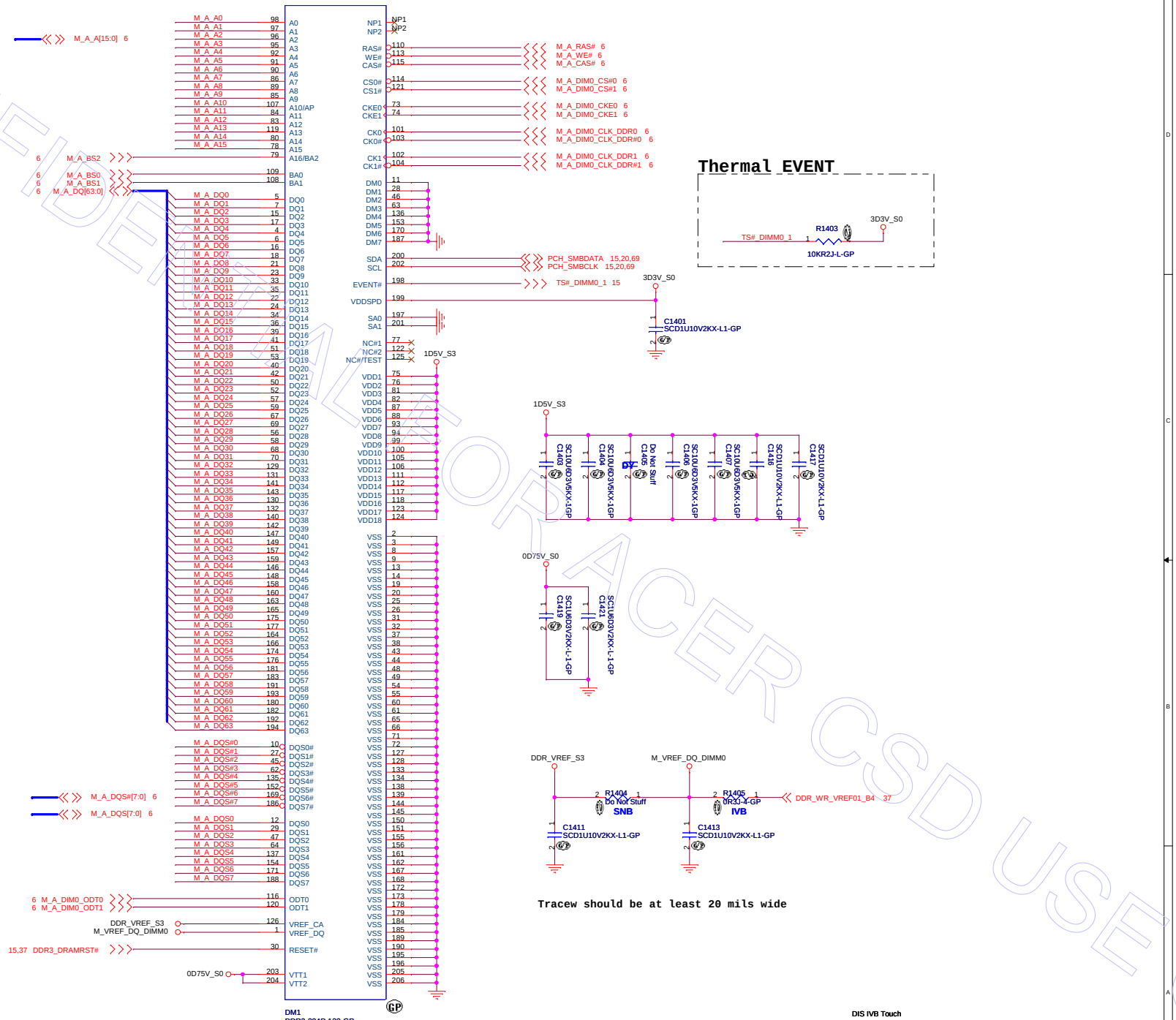
Title

Reserved

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 13 of 103

SSID = MEMORY



Thermal EVENT

Tracew should be at least 20 mils wide

DIS IVB Touch

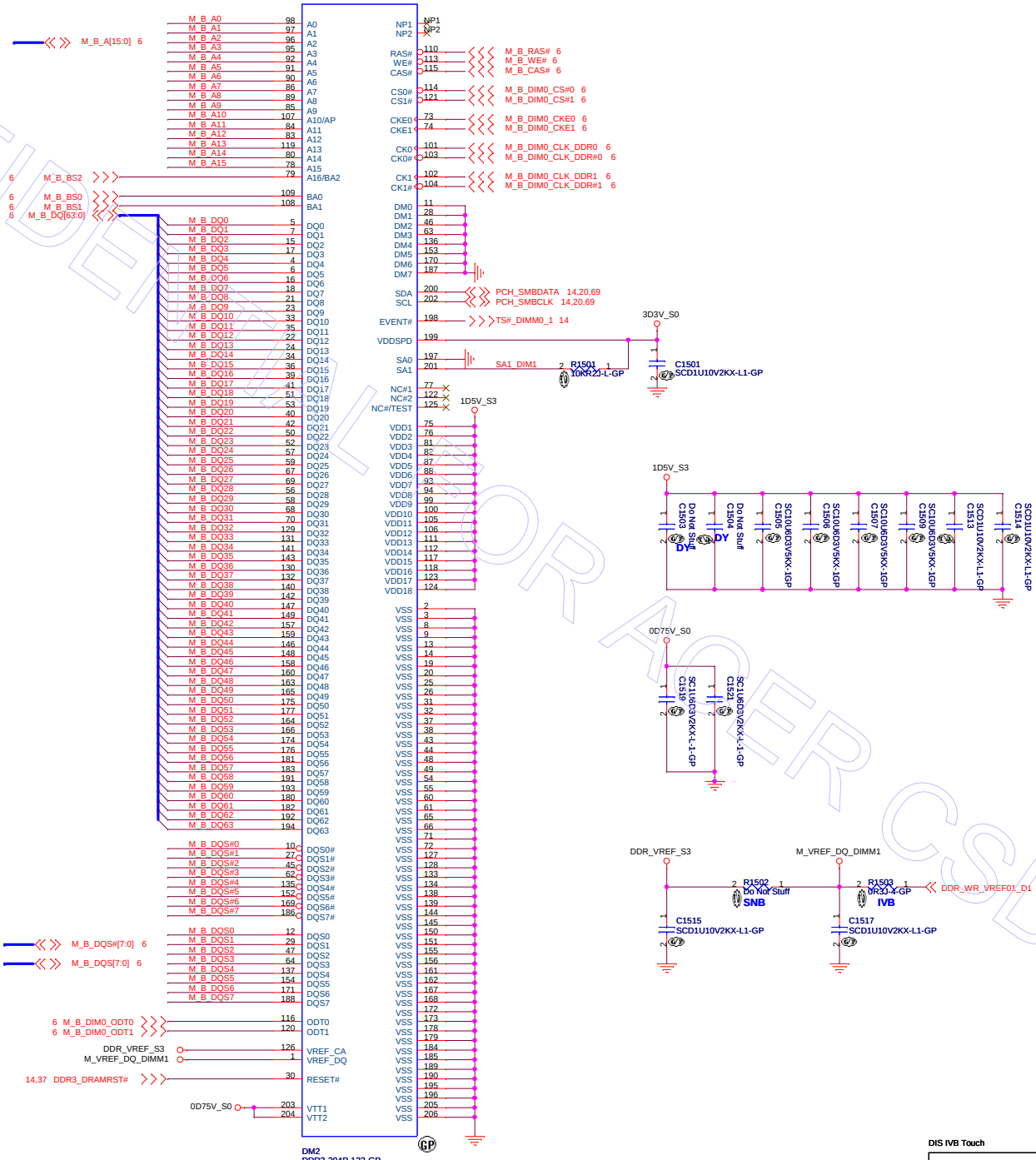
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 14 of 103

SSID = MEMORY



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 15 of 102

(Blanking)

DIS IVB Touch

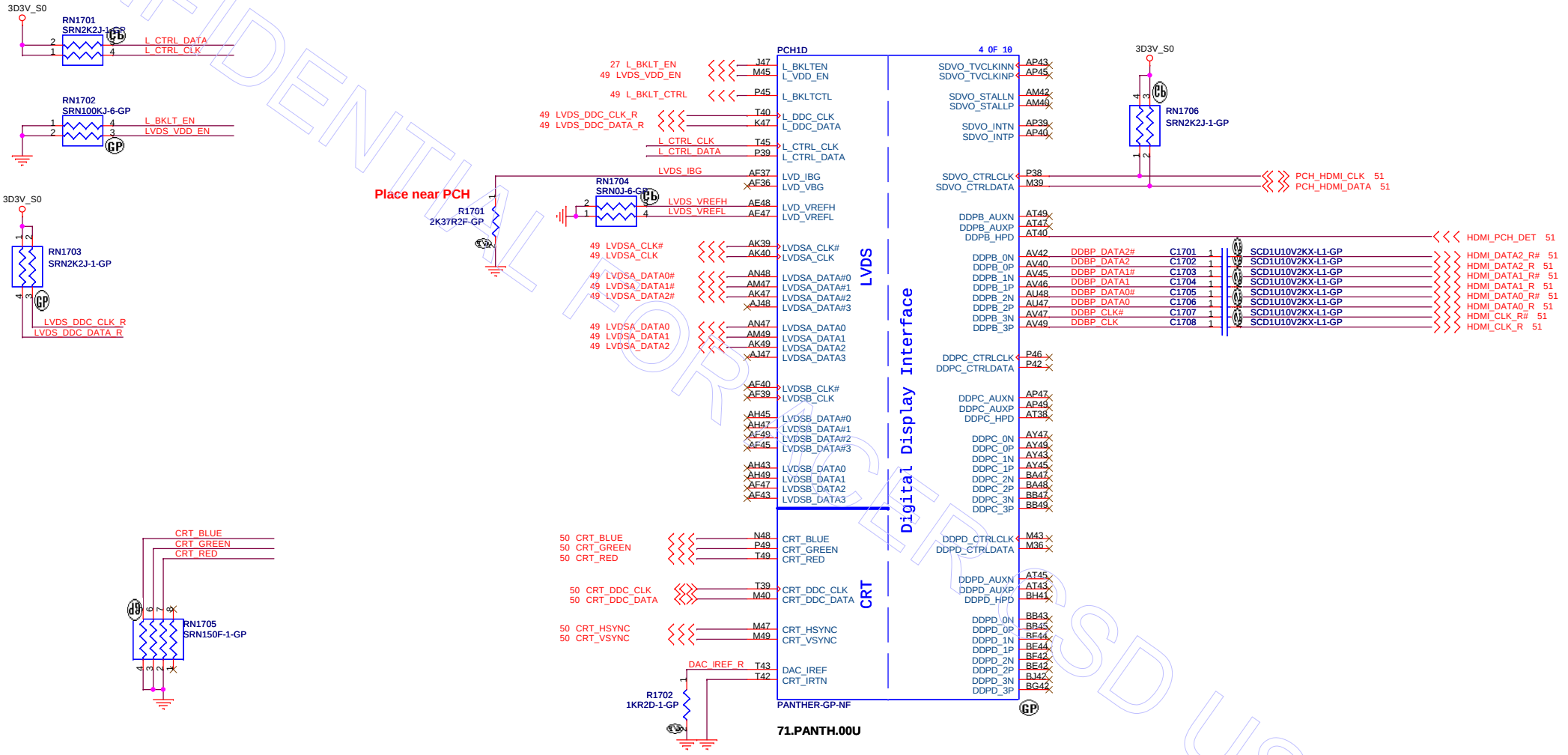
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	Husk/Petra	-4M

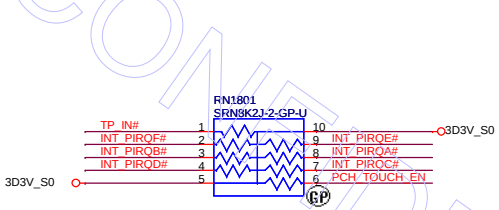
Date: Thursday, September 06, 2012 Sheet 16 of 103

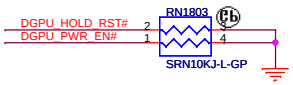


DIS IVB Touch

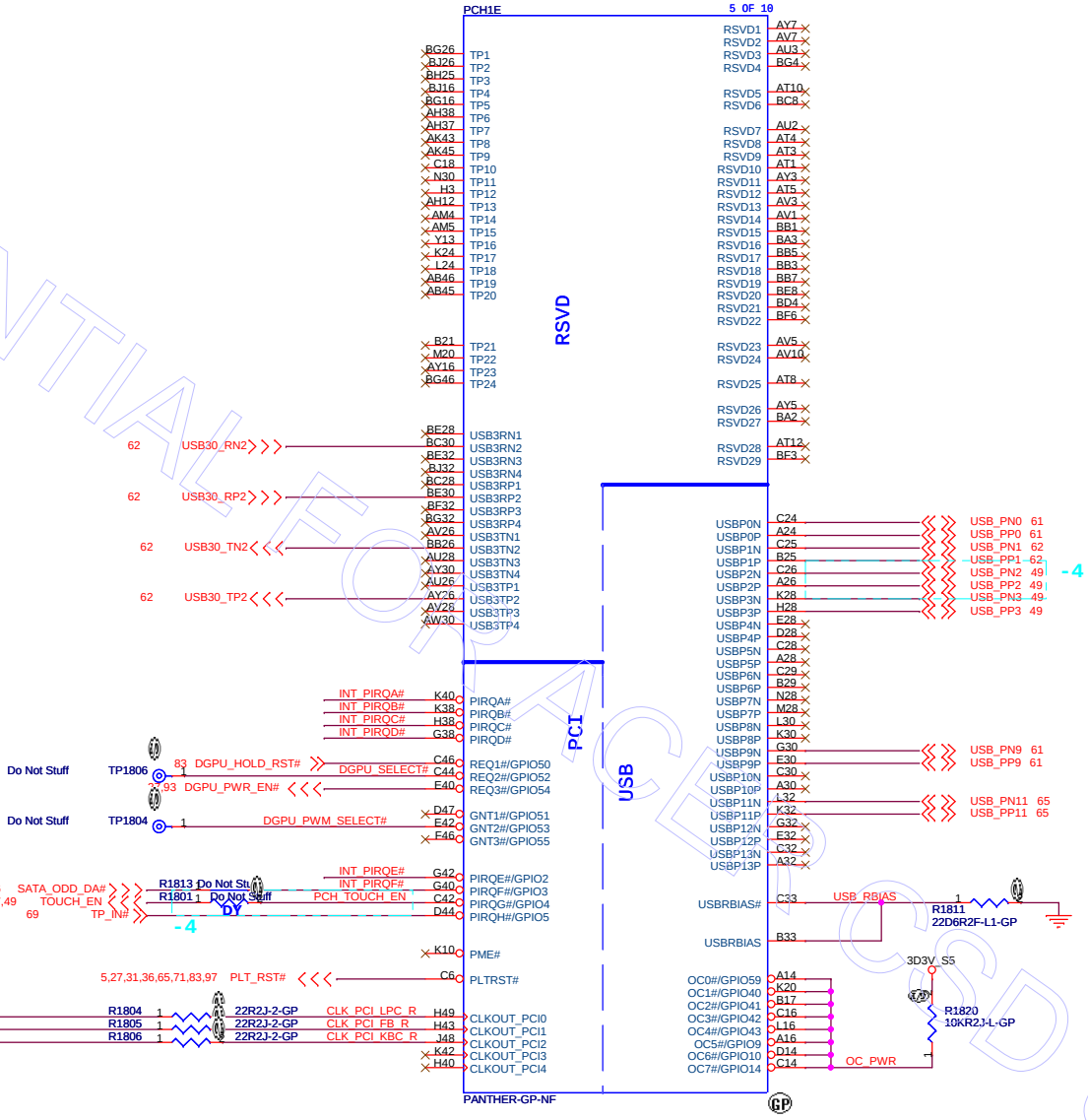
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH (LVDS/CRT/DDI)		
Size: A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 17 of 103	

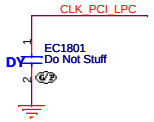
SSID = PCH





BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)





USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	Touch panel
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size	Document Number	Rev
Custom	Husk/Petra	-4M
Date: Thursday, September 06, 2012	Sheet 18 of 103	

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI_RXN[3:0]
4 DMI_RXP[3:0]
4 DMI_TXN[3:0]
4 DMI_TXP[3:0]

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

PCH1C 3 OF 10

DMI_RXN0 BC24 DMI0RXN
DMI_RXN1 BE20 DMI1RXN
DMI_RXN2 BG18 DMI2RXN
DMI_RXN3 BG20 DMI3RXN
DMI_RXP0 BE24 DMI0RXP
DMI_RXP1 BC20 DMI1RXP
DMI_RXP2 BJ18 DMI2RXP
DMI_RXP3 BJ20 DMI3RXP
DMI_TXN0 AW24 DMI0TXN
DMI_TXN1 AW20 DMI1TXN
DMI_TXN2 BB18 DMI2TXN
DMI_TXN3 AV18 DMI3TXN
DMI_TXP0 AY24 DMI0TXP
DMI_TXP1 AY20 DMI1TXP
DMI_TXP2 AY18 DMI2TXP
DMI_TXP3 AU18 DMI3TXP

DMI

FDI_RXN0 BJ14 FDI_TXN0
FDI_RXN1 AY14 FDI_TXN1
FDI_RXN2 BE14 FDI_TXN2
FDI_RXN3 BH13 FDI_TXN3
FDI_RXN4 BC12 FDI_TXN4
FDI_RXN5 BJ12 FDI_TXN5
FDI_RXN6 BG10 FDI_TXN6
FDI_RXN7 BG9 FDI_TXN7
FDI_RXP0 BG14 FDI_TXP0
FDI_RXP1 BB14 FDI_TXP1
FDI_RXP2 BF14 FDI_TXP2
FDI_RXP3 BG13 FDI_TXP3
FDI_RXP4 BE12 FDI_TXP4
FDI_RXP5 BG12 FDI_TXP5
FDI_RXP6 BJ10 FDI_TXP6
FDI_RXP7 BH9 FDI_TXP7
FDI_INT AW16 FDI_INT
FDI_FSYNC0 AV12 FDI_FSYNC0
FDI_FSYNC1 BC10 FDI_FSYNC1
FDI_LSYNC0 AV14 FDI_LSYNC0
FDI_LSYNC1 BB10 FDI_LSYNC1

FDI

1D05V_VTT
R1901 1 49D9R2F-GP DMI_COMP_R BJ24 DMI_ZCOMP
R1902 1 750R2F-GP RBIAS_CPY BG25 DMI_IRCOMP
BH21 DMI2RBIAS

DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH_DPWROK
R1910 Do Not Stuff
R1911 Do Not Stuff DY
PM_RSMRST# RTC_AUX_S5

SUS_PWR_ACK# C12 SUSACK#
SYS_RESET# K3 SYS_RESET#
SYS_PWROK P12 SYS_PWROK
PWROK L22 PWROK
APWROK L10
DRAMPWROK B13 37 PM_DRAM_PWRGD
RSMRST# C21 PM_RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30 K16 SUS_PWR_ACK_R
PWRBTN# E20 27,97 PM_PWRBTN#
ACPRESENT/GPIO31 H20 27 AC_PRESENT
BATLOW#/GPIO72 E10 BATLOW#
RI# A10 PM_RI#

WAKE# B9 PCIE_WAKE#
CLKRUN#/GPIO32 N3 PM_CLKRUN# 27
SUS_STAT#/GPIO61 G8
SUSCLK/GPIO62 N14 PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 D10
SLP_S4# H4 PM_SLP_S4# 27,46
SLP_S3# F4 PM_SLP_S3# 27,29,36,37,47
SLP_A# G10
SLP_SUS# G16 SLLP_SUS# TP 1 TP1904 Do Not Stuff
PMSYNCH AP14 H_PM_SYNC 5
SLP_LAN#/GPIO29 K14

System Power Management

PANTHER-GP-NF
71.PANTH.00U

DY R1926 Do Not Stuff SYS_PWROK
R1904 100KR2J-4-GP PWROK
3D3V_S0 R1905 10KR2J-L-GP
27 S0_PWR_GOOD 2 R1924 Do Not Stuff 1 PWROK

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 1 330KR2J-L1-GP
DSWODVREN R1918 1 DY Do Not Stuff

3D3V_S0
PM_CLKRUN# 1 R1919 8K2R2J-3-GP

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

3D3V_S5
RN1901 SRN10KJ-6-GP
8 1 BATLOW#
7 2 PM_RI#
6 3 AC_PRESENT
5 4 SUS_PWR_ACK_R
R1921 10KR2J-L-GP PCIE_WAKE#
R1922 10KR2J-L-GP SUS_PWR_ACK#
R1908 100KR2J-4-GP PM_RSMRST#

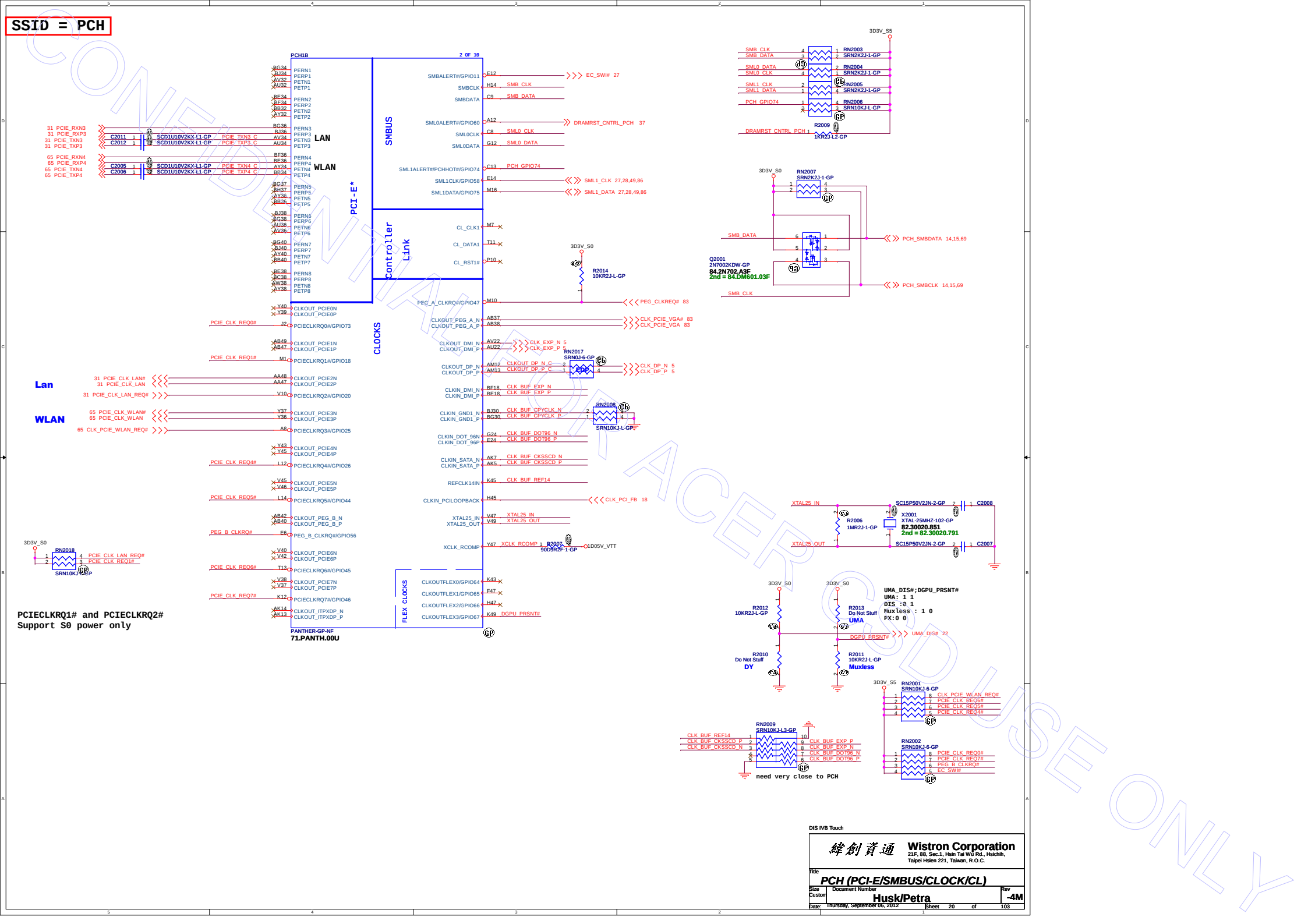
3D3V_AUX_S5
R1909 100KR2J-4-GP
R1916 10KR2J-L-GP
3V_5V_POK_# 1
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.F3F
PM_RSMRST# 1 R1912 1KR2J-L2-GP 2 RSMRST#_KBC 27
3V_5V_POK 41

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3
Document Number: Husk/Petra
Rev: -4M
Date: Thursday, September 06, 2012
Sheet 19 of 103

SSID = PCH



DIS IVB Touch

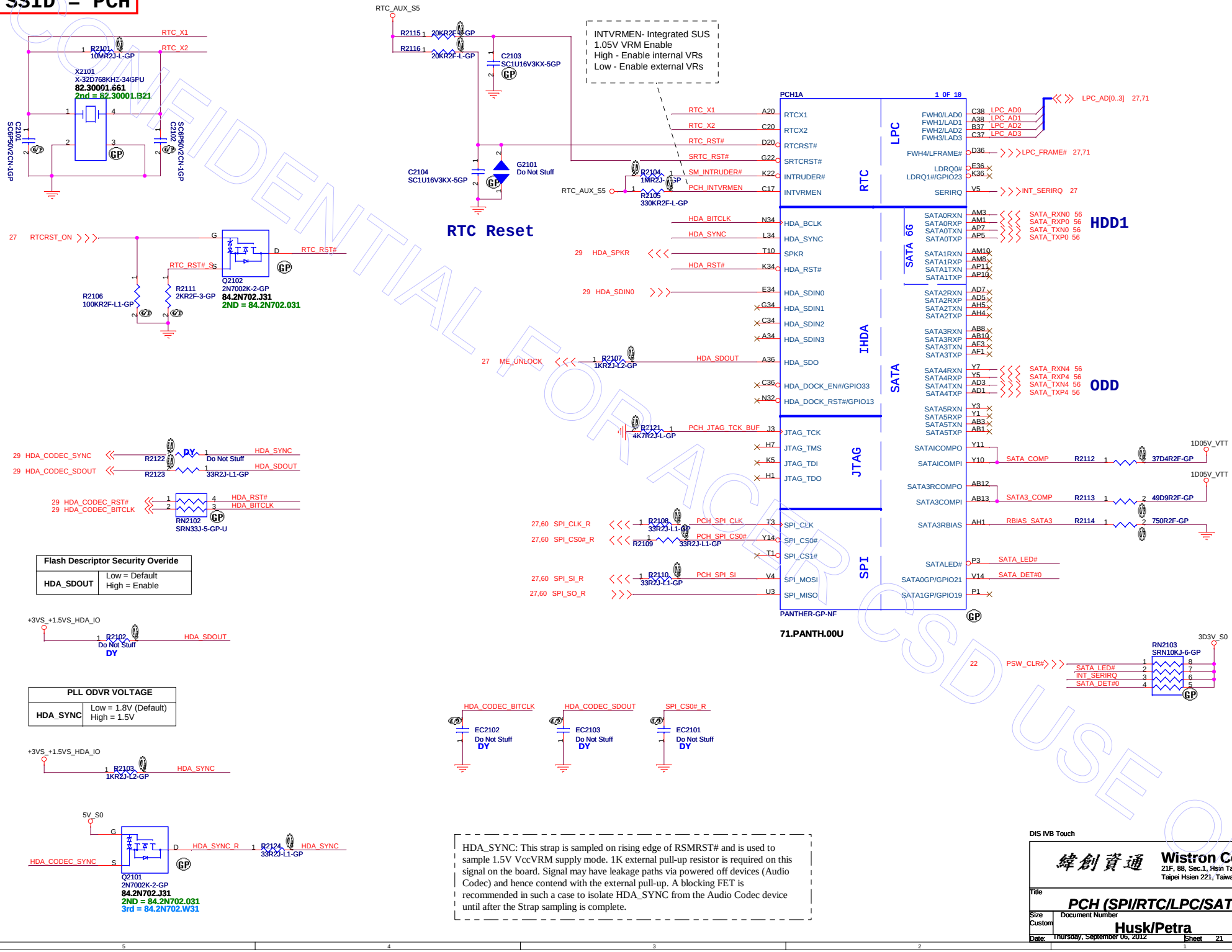
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 20 of 103

SSID = PCH



DIS IVB Touch

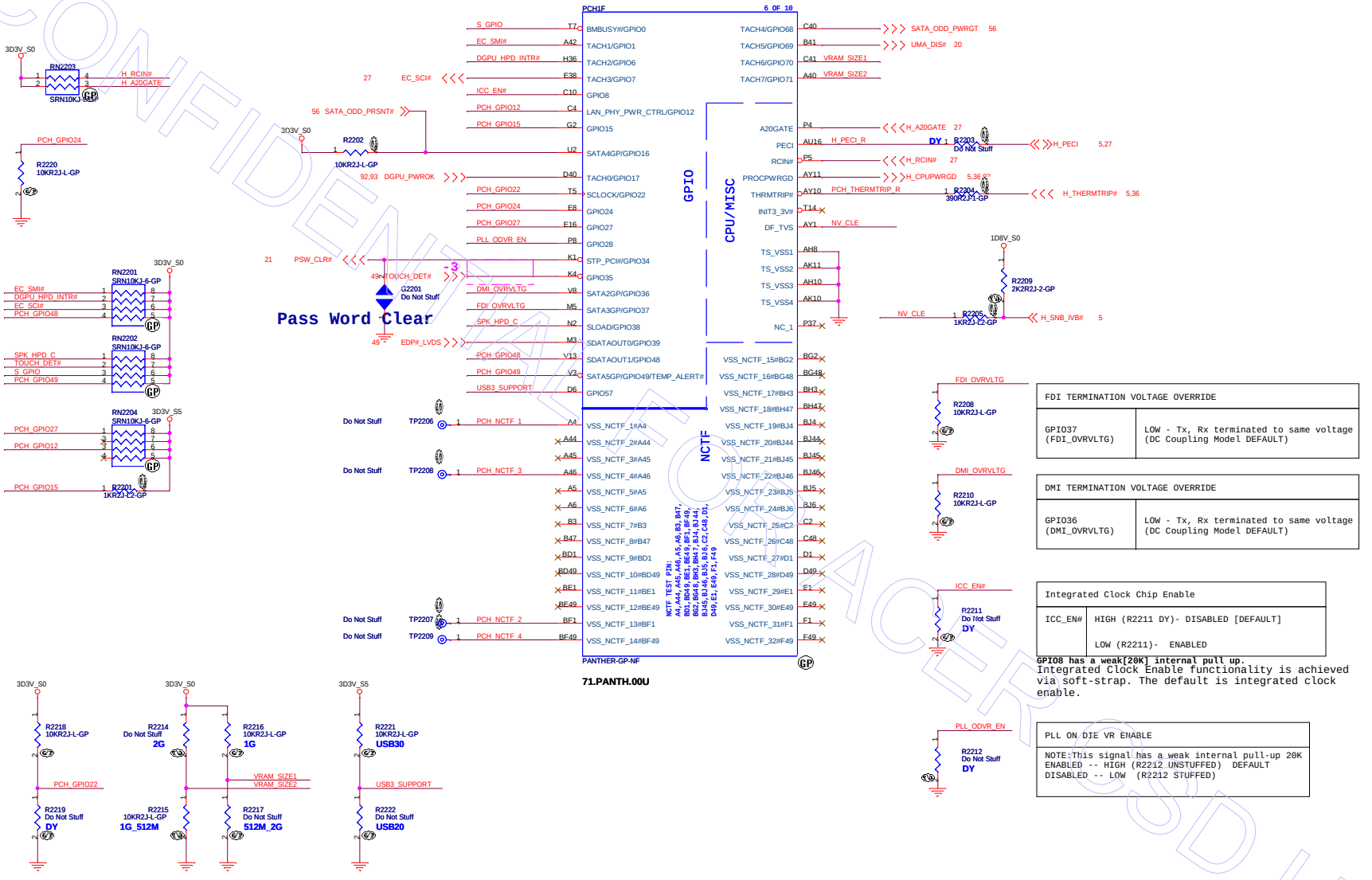
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

DIS IVB Touch

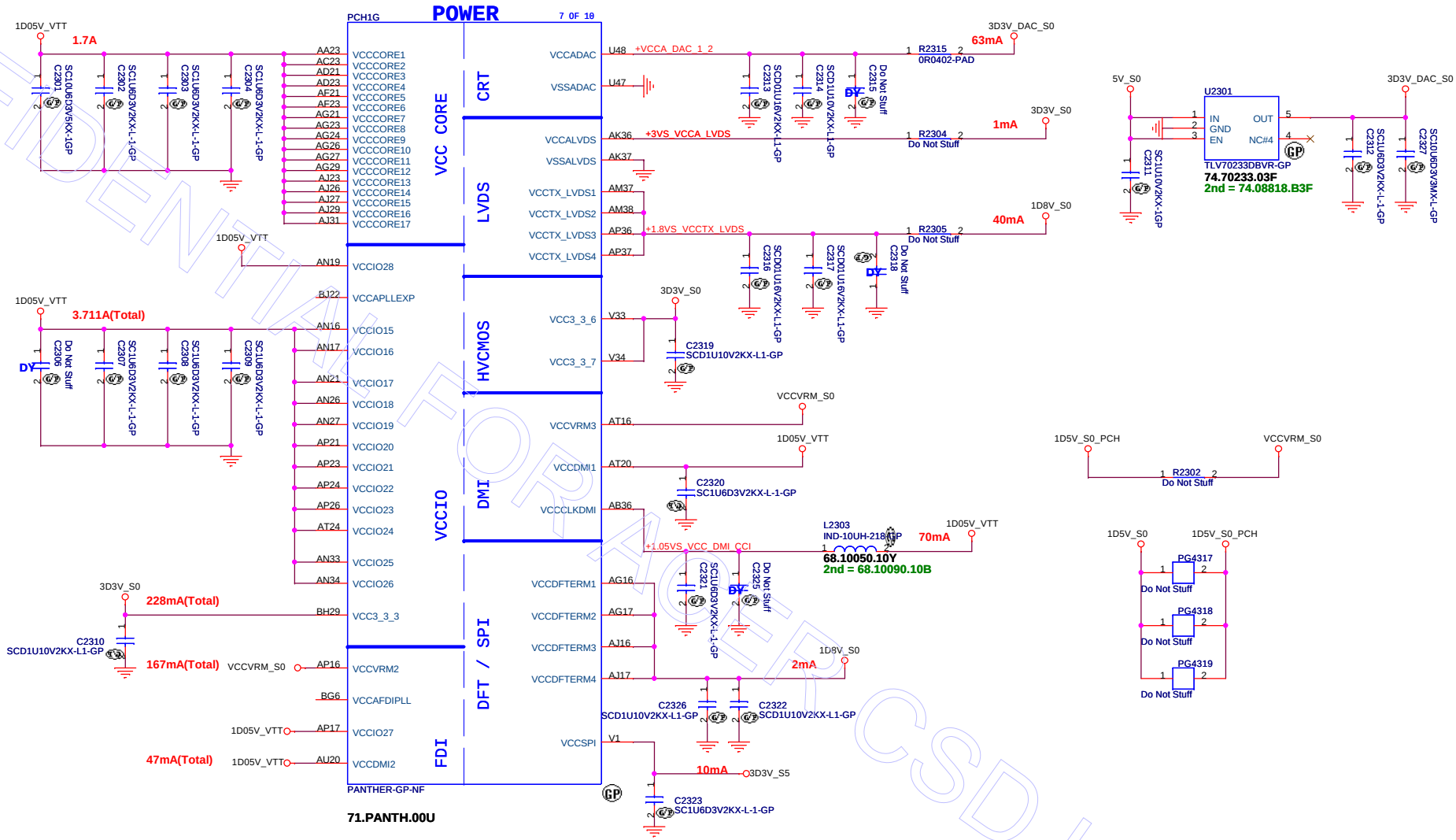
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 22 of 103

SSID = PCH



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 23 of 103

SSID = PCH

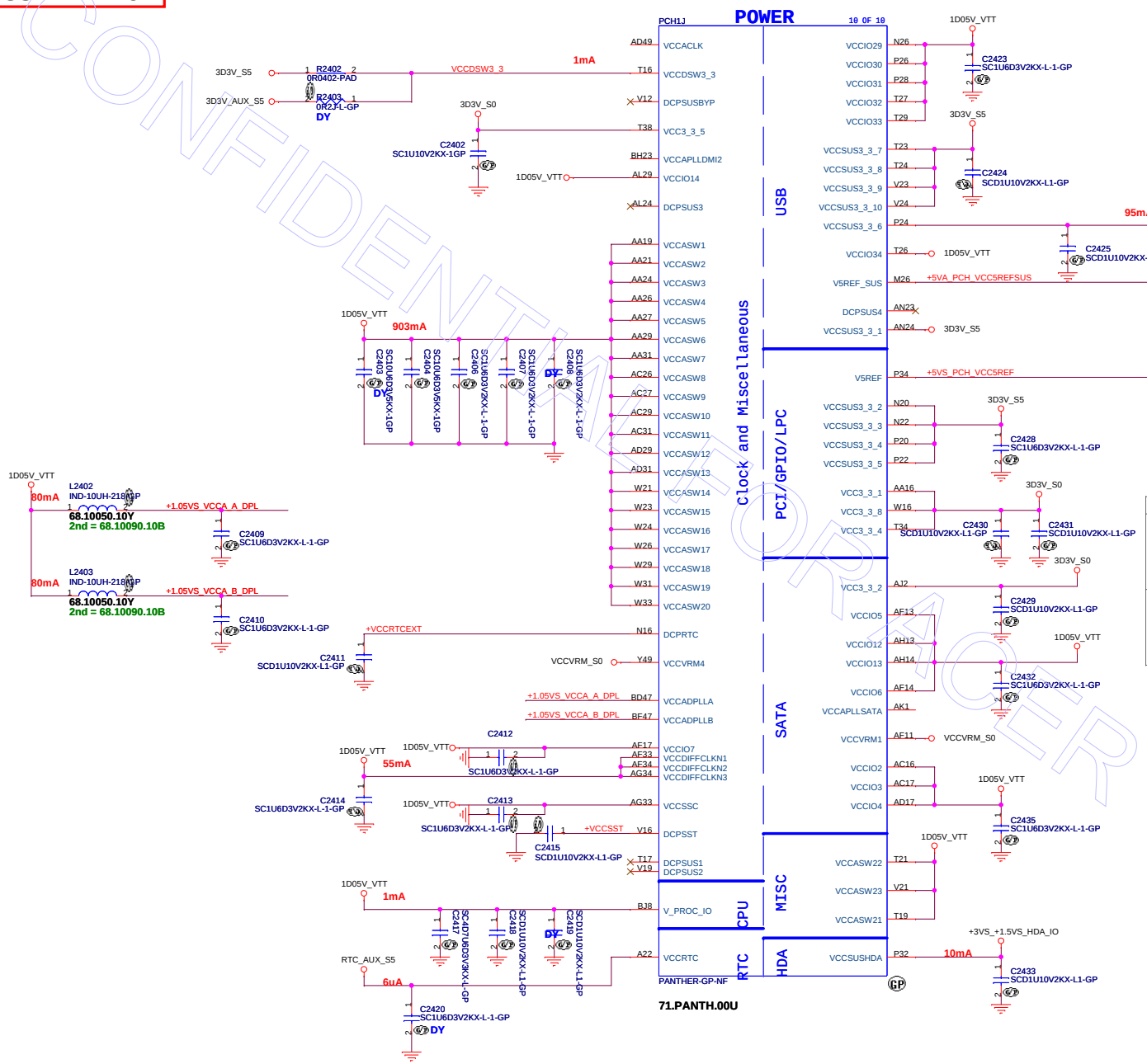
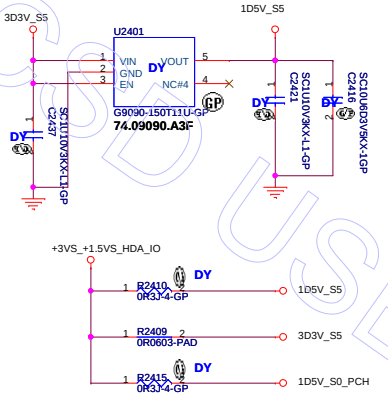


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



DIS IVB Touch

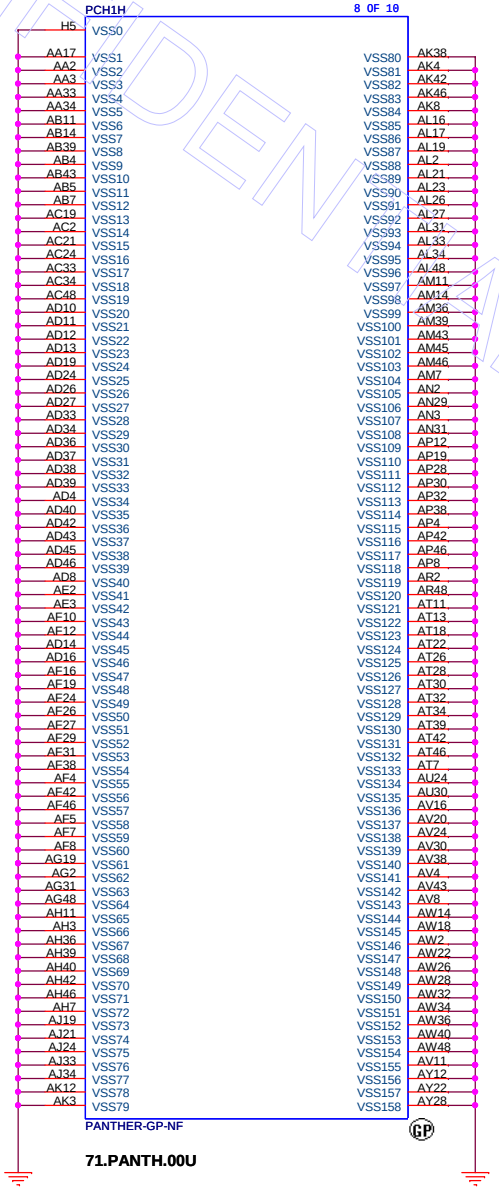
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

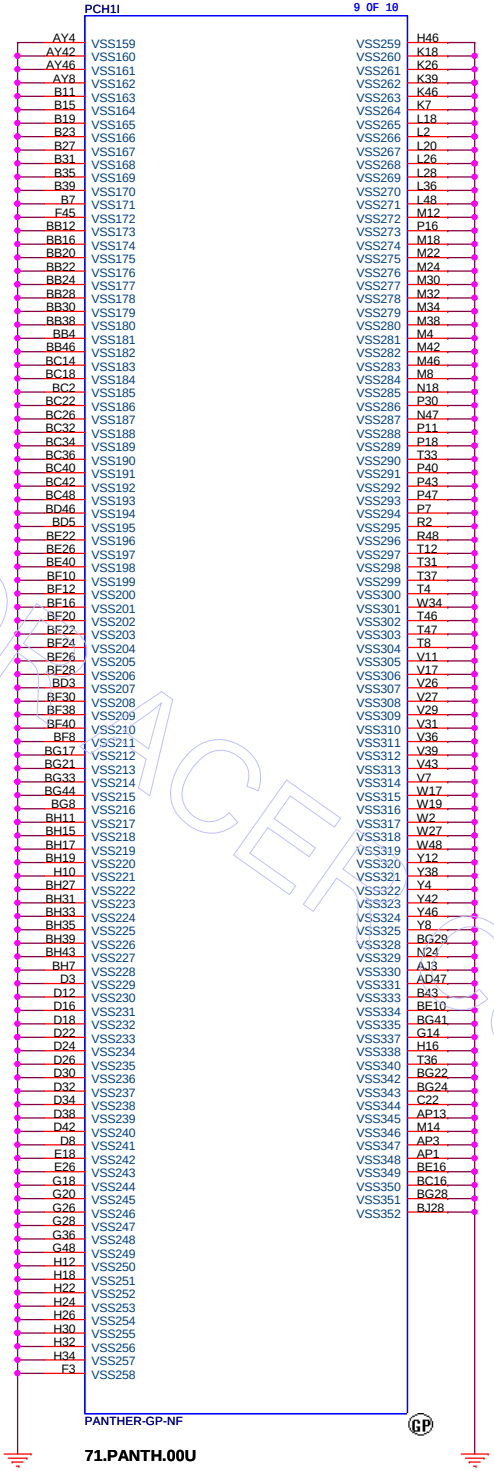
Title: PCH (POWER2)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Monday, September 17, 2012 Sheet 24 of 103

SSID = PCH





DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 25 of 103

DIS IVB Touch

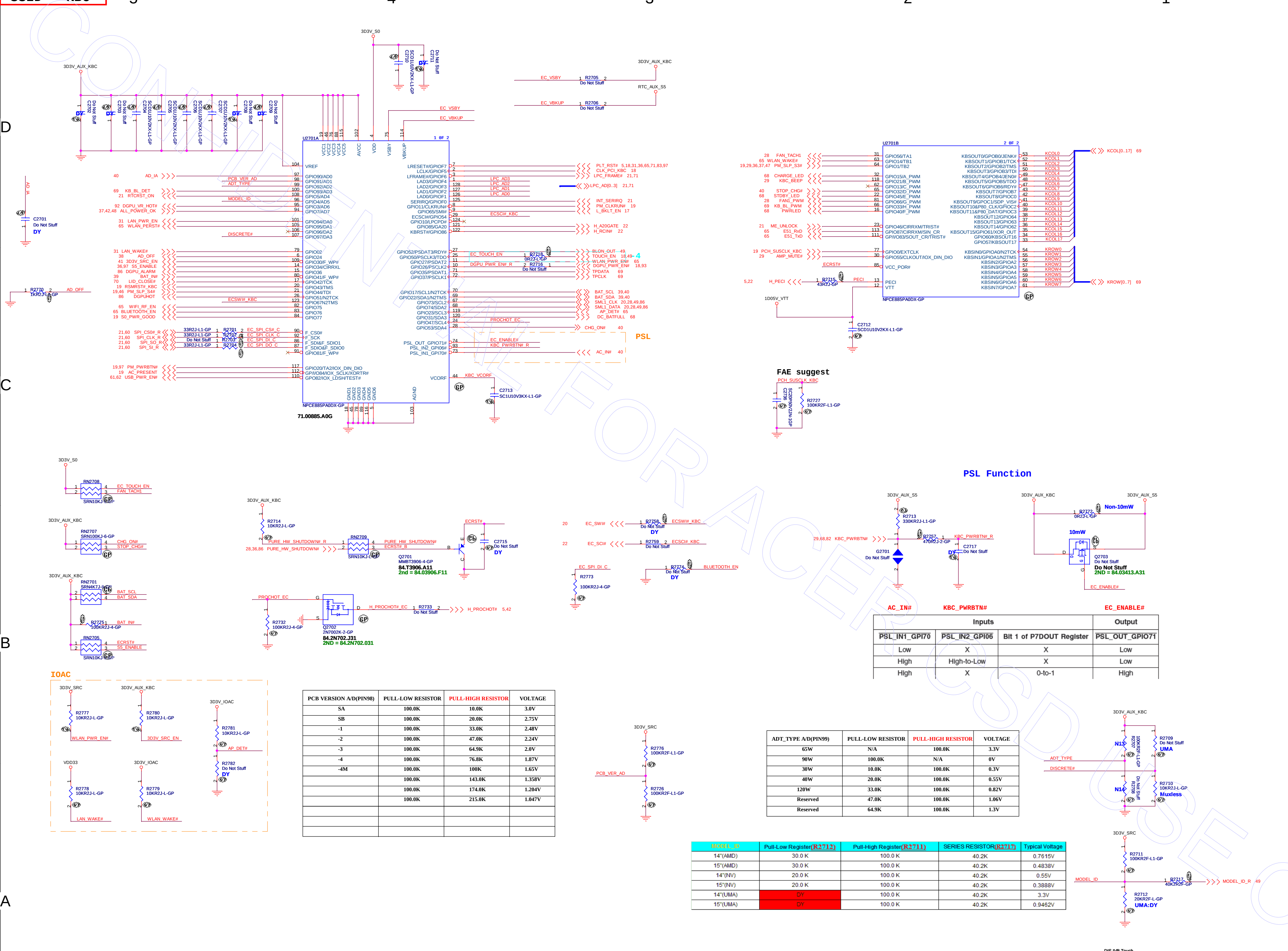
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Clock(colay)

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 26 of 103

SSID = KBC



Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.48V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

MODEL_ID	Pull-Low Register(R2712)	Pull-High Register(R2711)	SERIES RESISTOR(R2717)	Typical Voltage
14"(AMD)	30.0 K	100.0 K	40.2K	0.7615V
15"(AMD)	30.0 K	100.0 K	40.2K	0.4838V
14"(NV)	20.0 K	100.0 K	40.2K	0.55V
15"(NV)	20.0 K	100.0 K	40.2K	0.3888V
14"(UMA)	DY	100.0 K	40.2K	3.3V
15"(UMA)	DY	100.0 K	40.2K	0.9462V

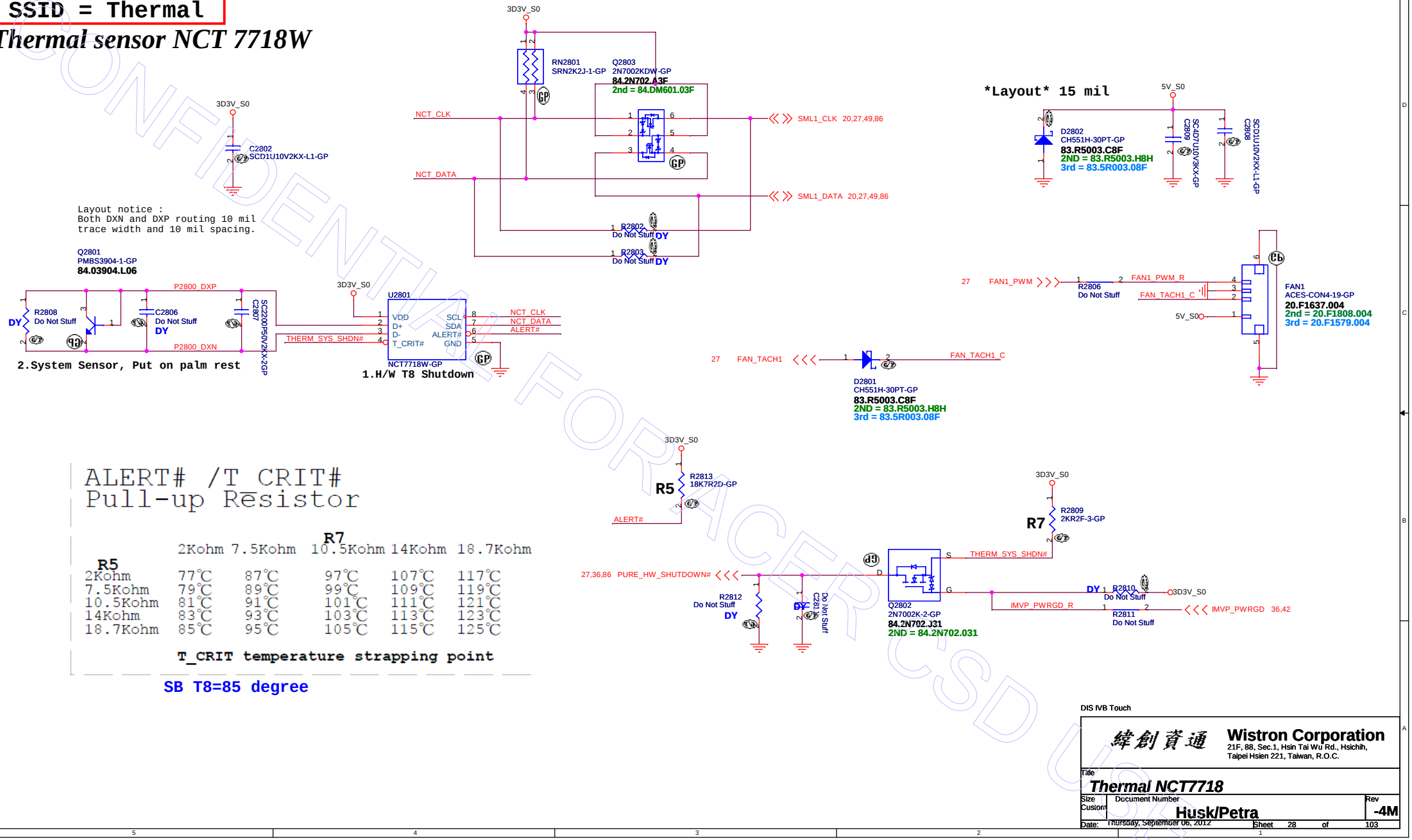
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC NPCE885
Size: Custom | Document Number: Husk/Petra | Rev: -4M
Date: Thursday, September 06, 2012 | Sheet 27 of 103

SSID = Thermal

Thermal sensor NCT 7718W



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree

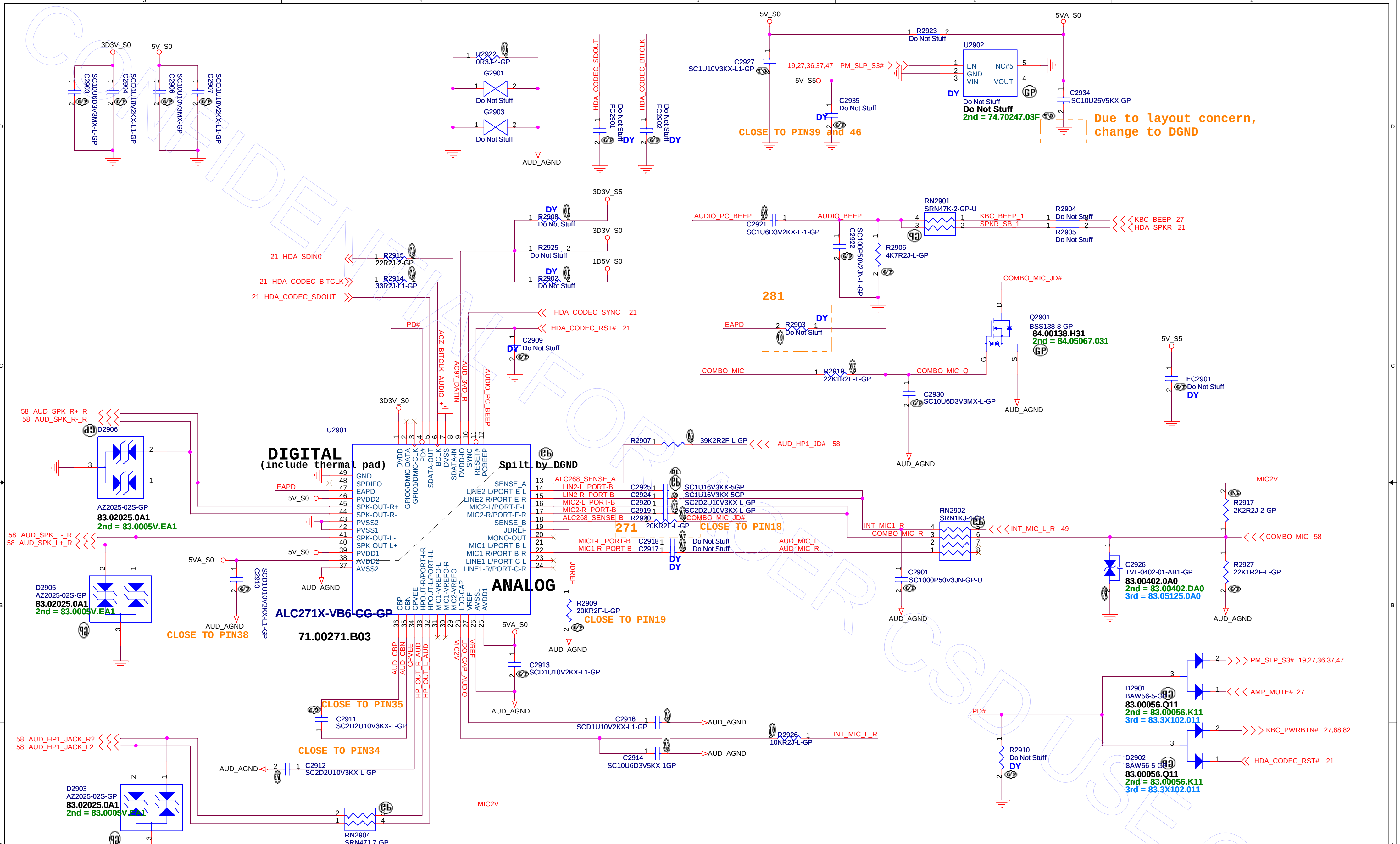
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 28 of 103



CONFIDENTIAL FOR CSD USE ONLY
DIGITAL
(include thermal pad)
ANALOG
Spilt by DGND
U2901
ALC271X-VB6-CG-GP
71.00271.B03
U2902
Due to layout concern, change to DGND
CLOSE TO PIN39 and 46
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
CLOSE TO PIN18
Q2901
BSS138-8-GP
84.00138.H31
2nd = 84.05067.031
D2906
AZ2025-02S-GP
83.02025.0A1
2nd = 83.0005V.EA1
D2905
AZ2025-02S-GP
83.02025.0A1
2nd = 83.0005V.EA1
D2903
AZ2025-02S-GP
83.02025.0A1
2nd = 83.0005V.EA1
C2926
TVL-0402-01-AB1-GP
83.00402.0A0
2nd = 83.00402.DA0
3rd = 83.05125.0A0
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
D2902
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
RN2901
SRN47K-2-GP-U
RN2902
SRN1KJ-4-GP
RN2904
SRN47J-7-GP
AUDIO_PC_BEEP
KBC_BEEP 27
HDA_SPKR 21
COMBO_MIC_JD#
COMBO_MIC 58
AUD_HP1_JD# 58
INT_MIC_L_R 49
PM_SLP_S3# 19,27,36,37,47
AMP_MUTE# 27
KBC_PWRBTN# 27,68,82
HDA_CODEC_RST# 21
HDA_CODEC_SYNC 21
21 HDA_SDIN0
21 HDA_CODEC_BITCLK
21 HDA_CODEC_SDOUT
58 AUD_SPK_R+_R
58 AUD_SPK_R-_R
58 AUD_SPK_L-_R
58 AUD_SPK_L+_R
58 AUD_HP1_JACK_R2
58 AUD_HP1_JACK_L2
AUD_AGND

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Codec	
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 29 of 103	

DIS IVB Touch

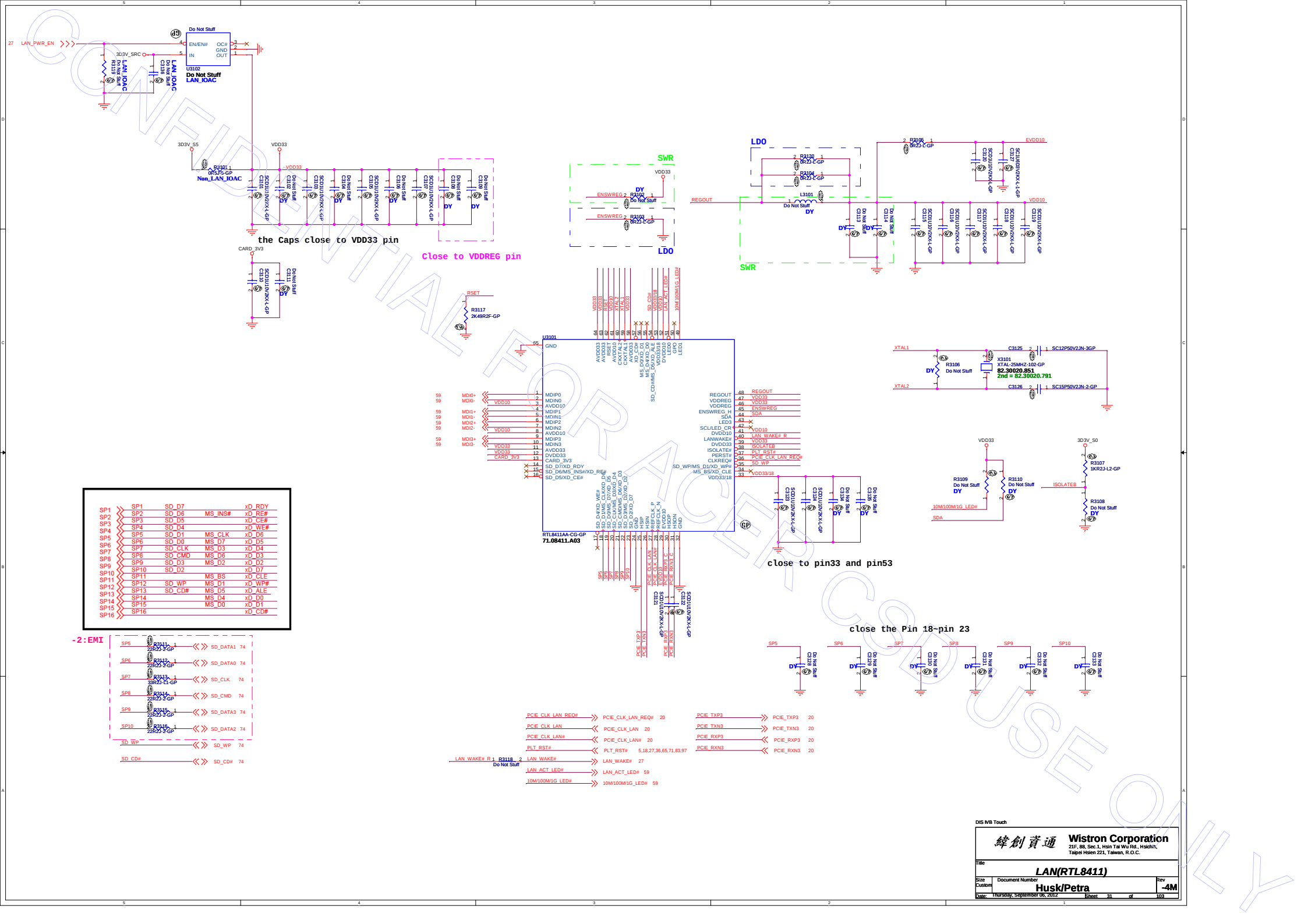
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 30 of 103



DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5159 (CARD READER)

Size	Document Number	Rev
Custom	Husk/Petra	-4M
Date: Thursday, September 06, 2012	Sheet 32 of 103	

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 33 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 34 of 103

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

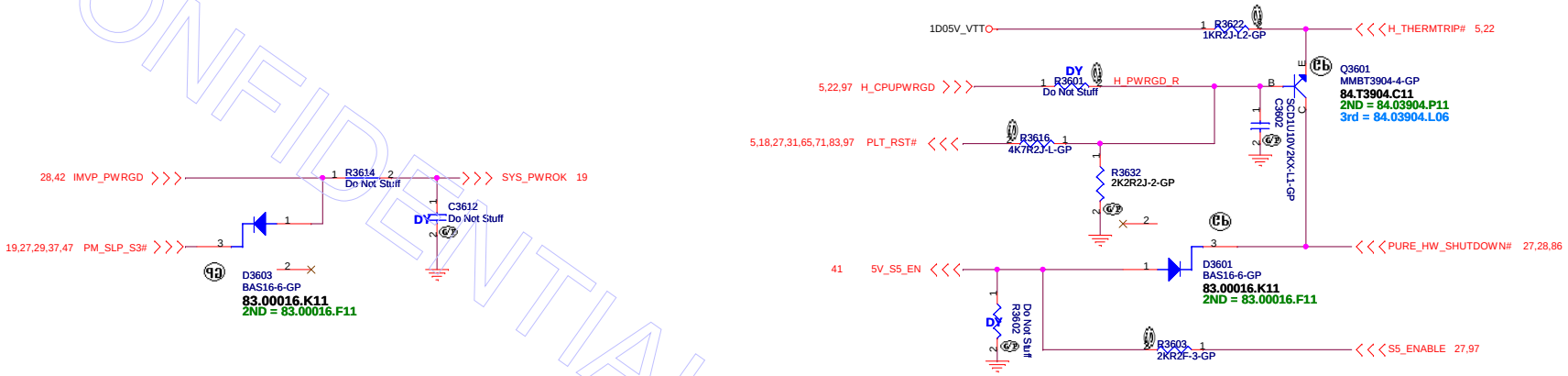
Title

USB 3.0 Controller

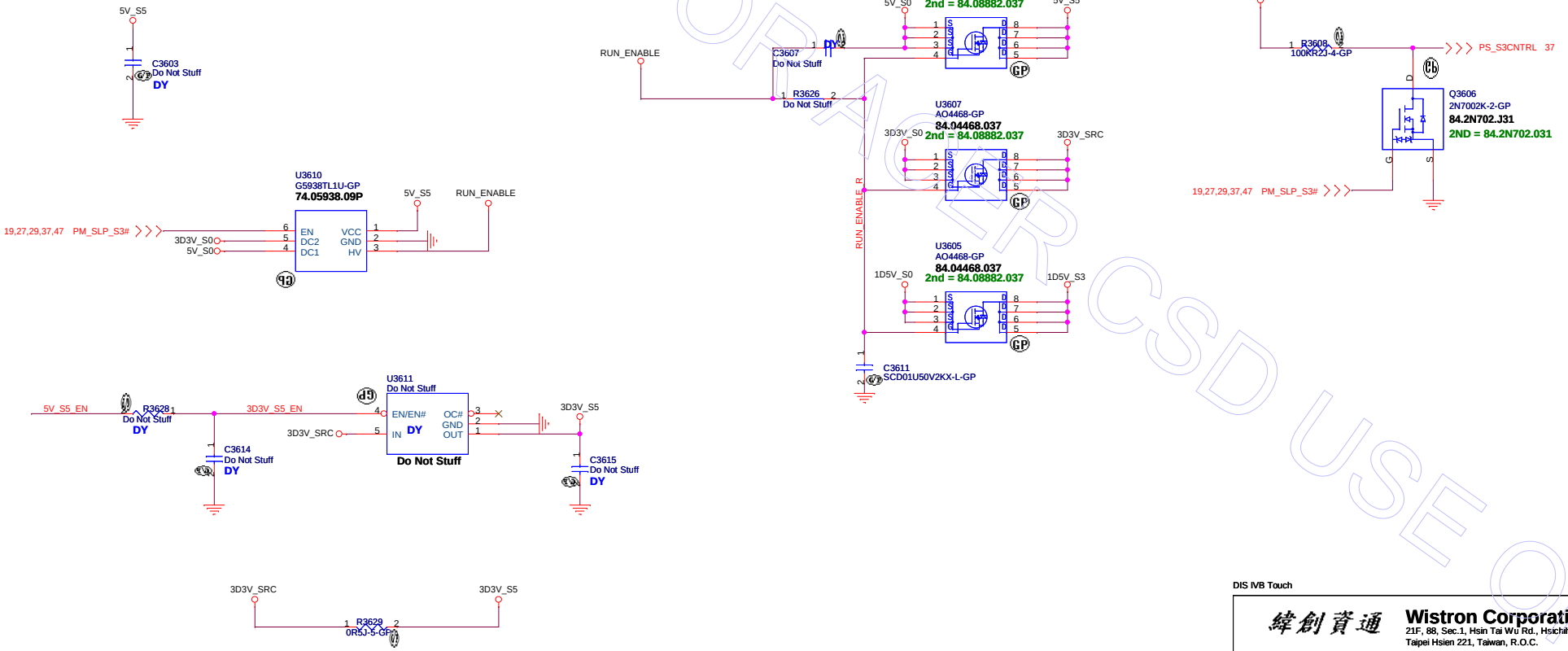
Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 35 of 103

Power Sequence



ANNIE Run Power



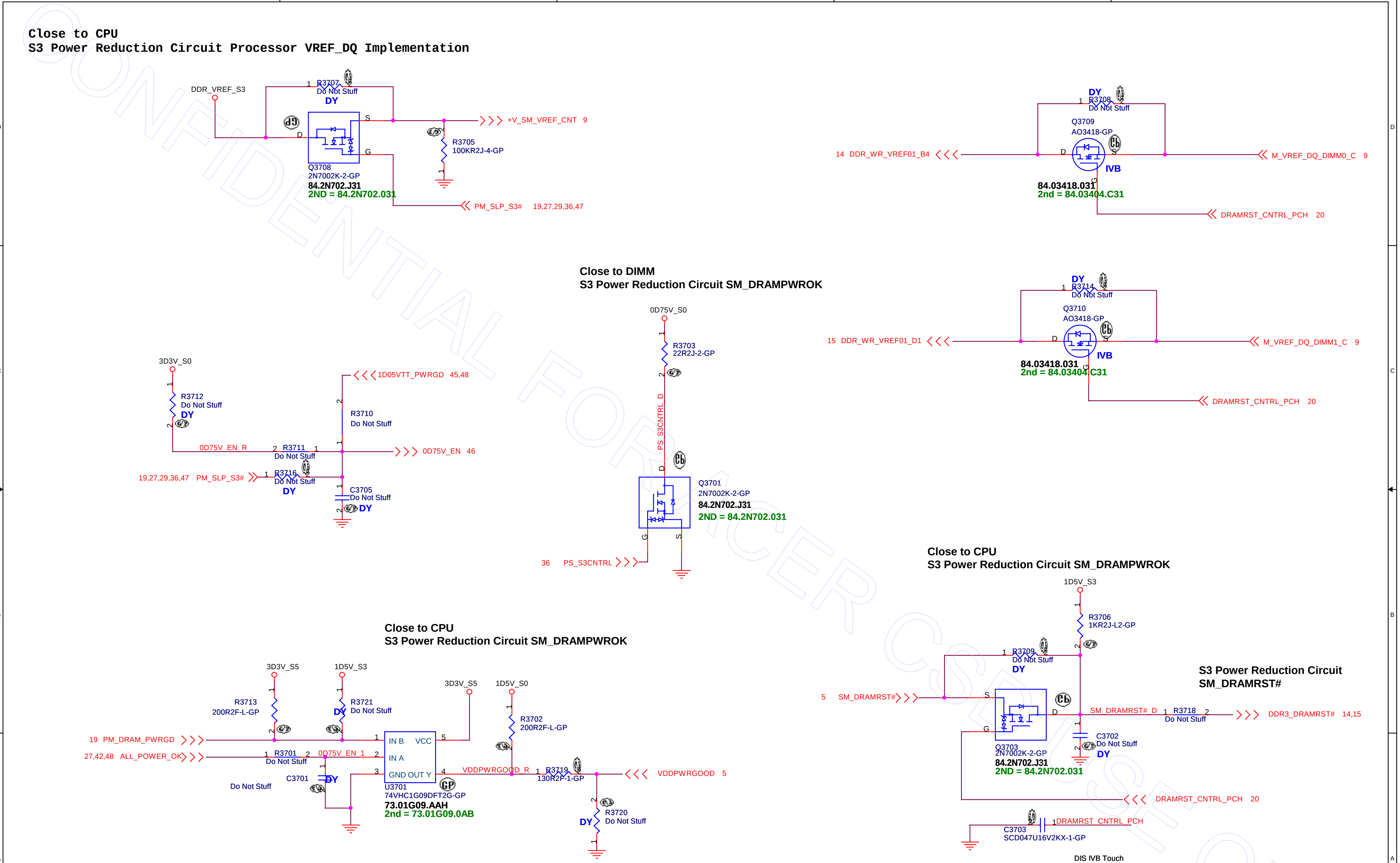
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 36 of 103

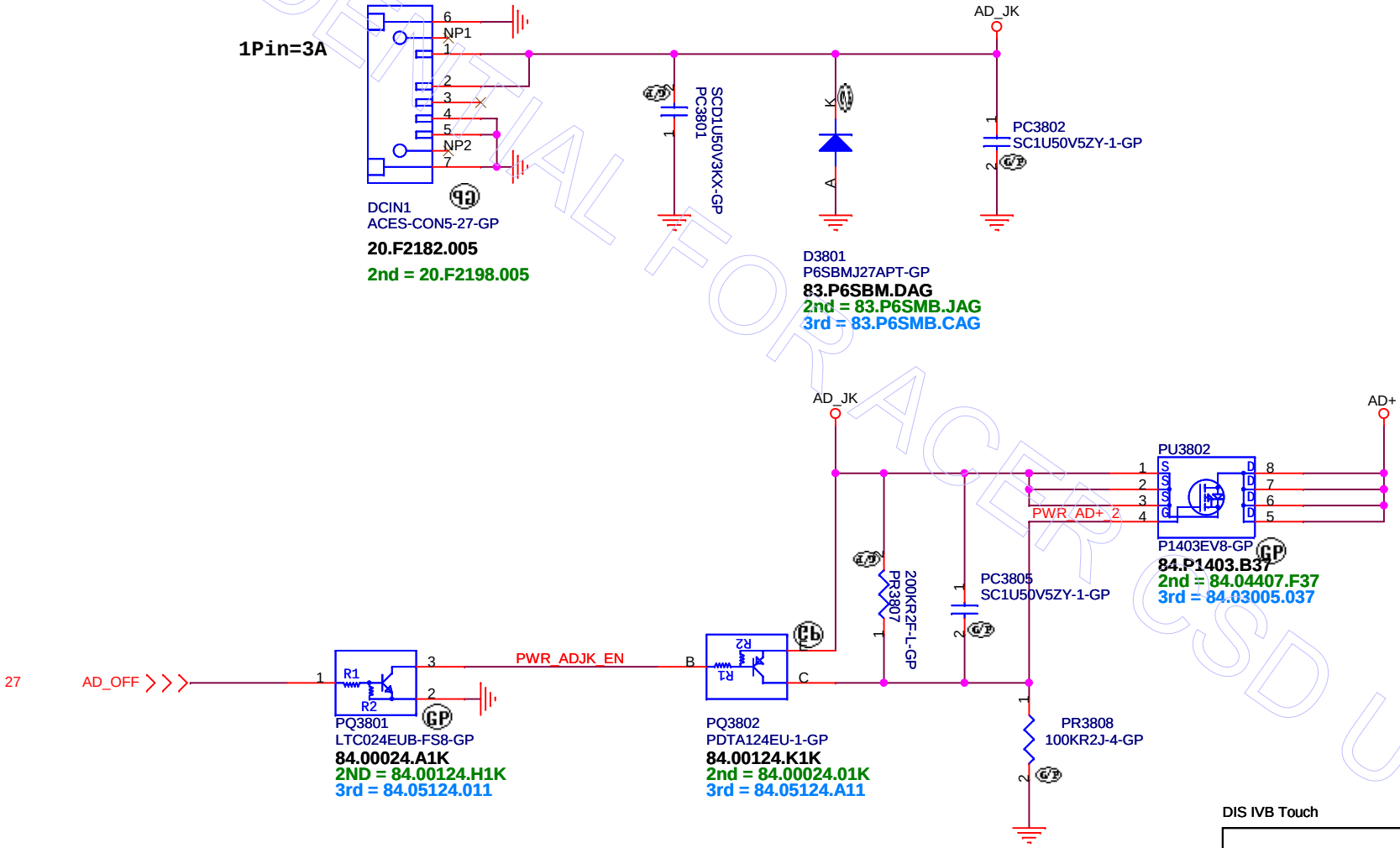

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation
DDR_VREF_S3
R3707 Do Not Stuff DY
Q3708 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
+V_SM_VREF_CNT 9
R3705 100KR2J-4-GP
PM_SLP_S3# 19,27,29,36,47
DY R3708 Do Not Stuff
Q3709 AO3418-GP
14 DDR_WR_VREF01_B4
M_VREF_DQ_DIMM0_C 9
IVB
84.03418.031
2nd = 84.03404.C31
DRAMRST_CNTRL_PCH 20
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK
0D75V_S0
R3703 22R2J-2-GP
PS_S3CNTRL_D
Q3701 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
36 PS_S3CNTRL
DY R3714 Do Not Stuff
Q3710 AO3418-GP
15 DDR_WR_VREF01_D1
M_VREF_DQ_DIMM1_C 9
IVB
84.03418.031
2nd = 84.03404.C31
DRAMRST_CNTRL_PCH 20
3D3V_S0
R3712 Do Not Stuff DY
1D05VTT_PWRGD 45,48
R3710 Do Not Stuff
0D75V_EN_R
R3711 Do Not Stuff
0D75V_EN 46
19,27,29,36,47 PM_SLP_S3#
R3716 Do Not Stuff DY
C3705 Do Not Stuff DY
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
1D5V_S3
R3706 1KR2J-L2-GP
R3709 Do Not Stuff DY
S3 Power Reduction Circuit
SM_DRAMRST#
5 SM_DRAMRST#
SM_DRAMRST#_D
R3718 Do Not Stuff
DDR3_DRAMRST# 14,15
Q3703 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
C3702 Do Not Stuff DY
DRAMRST_CNTRL_PCH 20
C3703 SCD047U16V2KX-1-GP
DRAMRST_CNTRL_PCH
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
3D3V_S5
1D5V_S3
R3713 200R2F-L-GP
R3721 Do Not Stuff DY
3D3V_S5
1D5V_S0
R3702 200R2F-L-GP
19 PM_DRAM_PWRGD
27,42,48 ALL_POWER_OK
R3701 Do Not Stuff
0D75V_EN_1
C3701 Do Not Stuff DY
IN B VCC
IN A
GND OUT Y
U3701 74VHC1G09DFT2G-GP
73.01G09.AAH
2nd = 73.01G09.0AB
VDDPWRGOOD_R
R3719 130R2F-1-GP
VDDPWRGOOD 5
R3720 Do Not Stuff DY
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 37 of 103



DIS IVB Touch

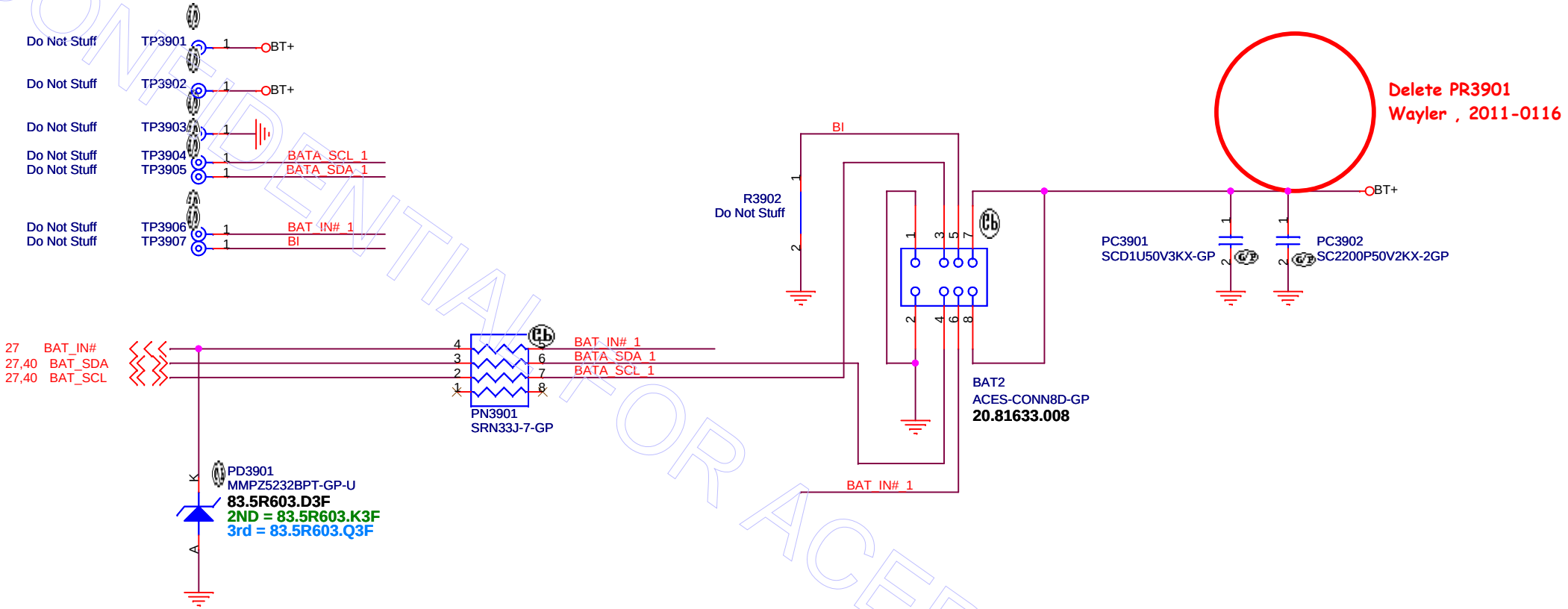
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 38 of 103

BATTERY CONNECTOR



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

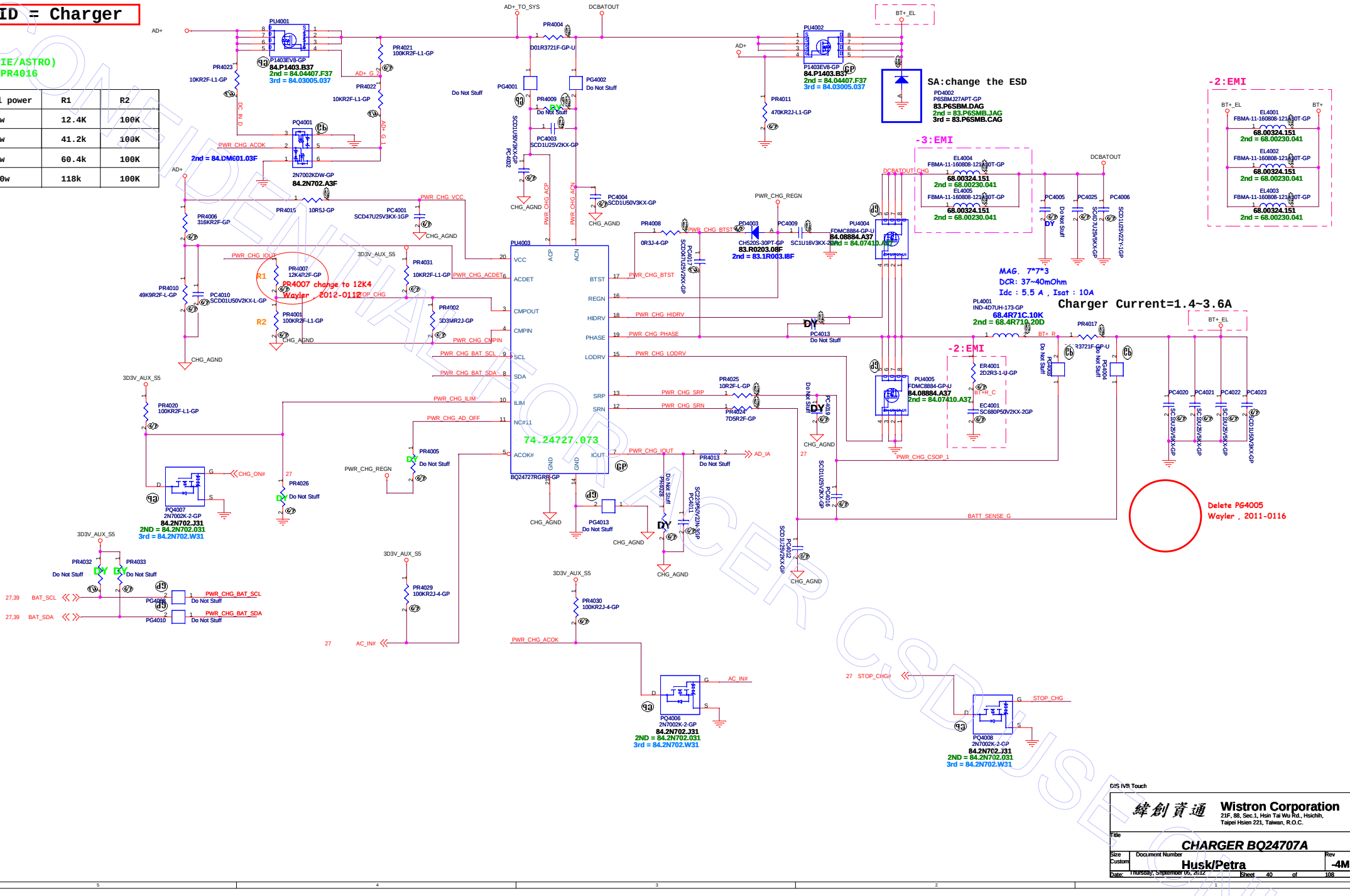
Size	Document Number	Rev
A4	Husk/Petra	-4M

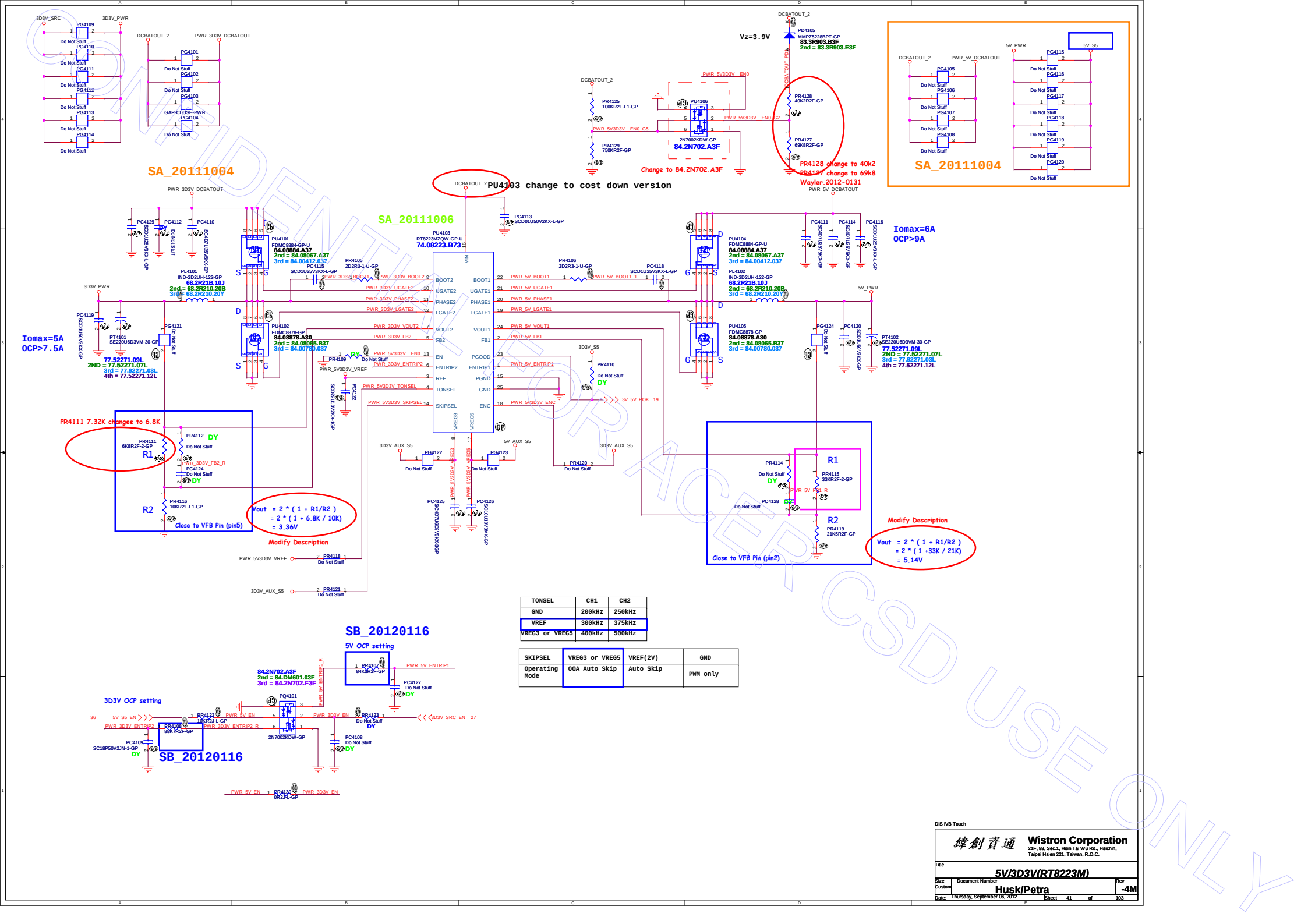
Date: Thursday, September 06, 2012 Sheet 39 of 103

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K





TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

DIS IVB Touch

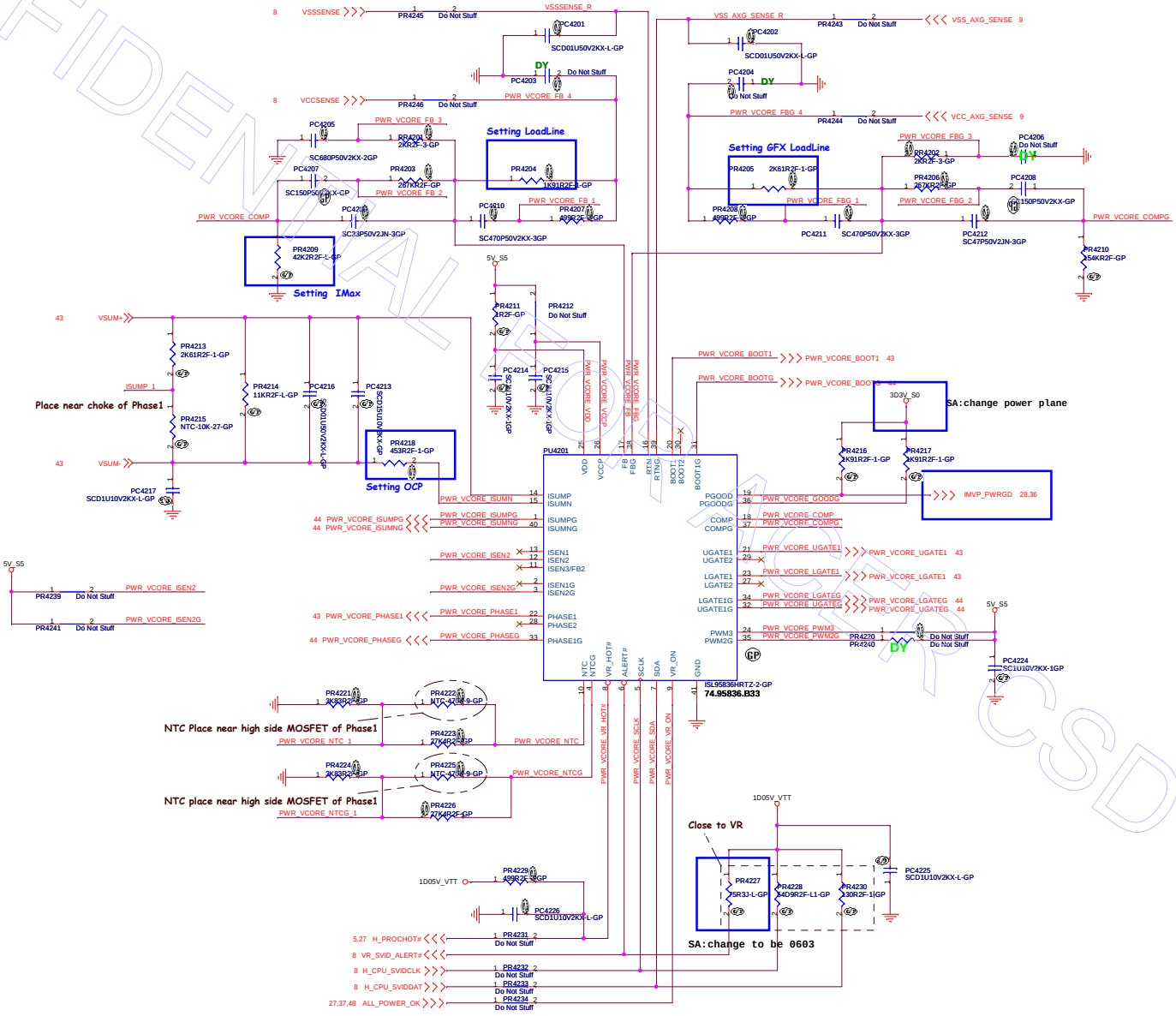
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(RT8223M)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



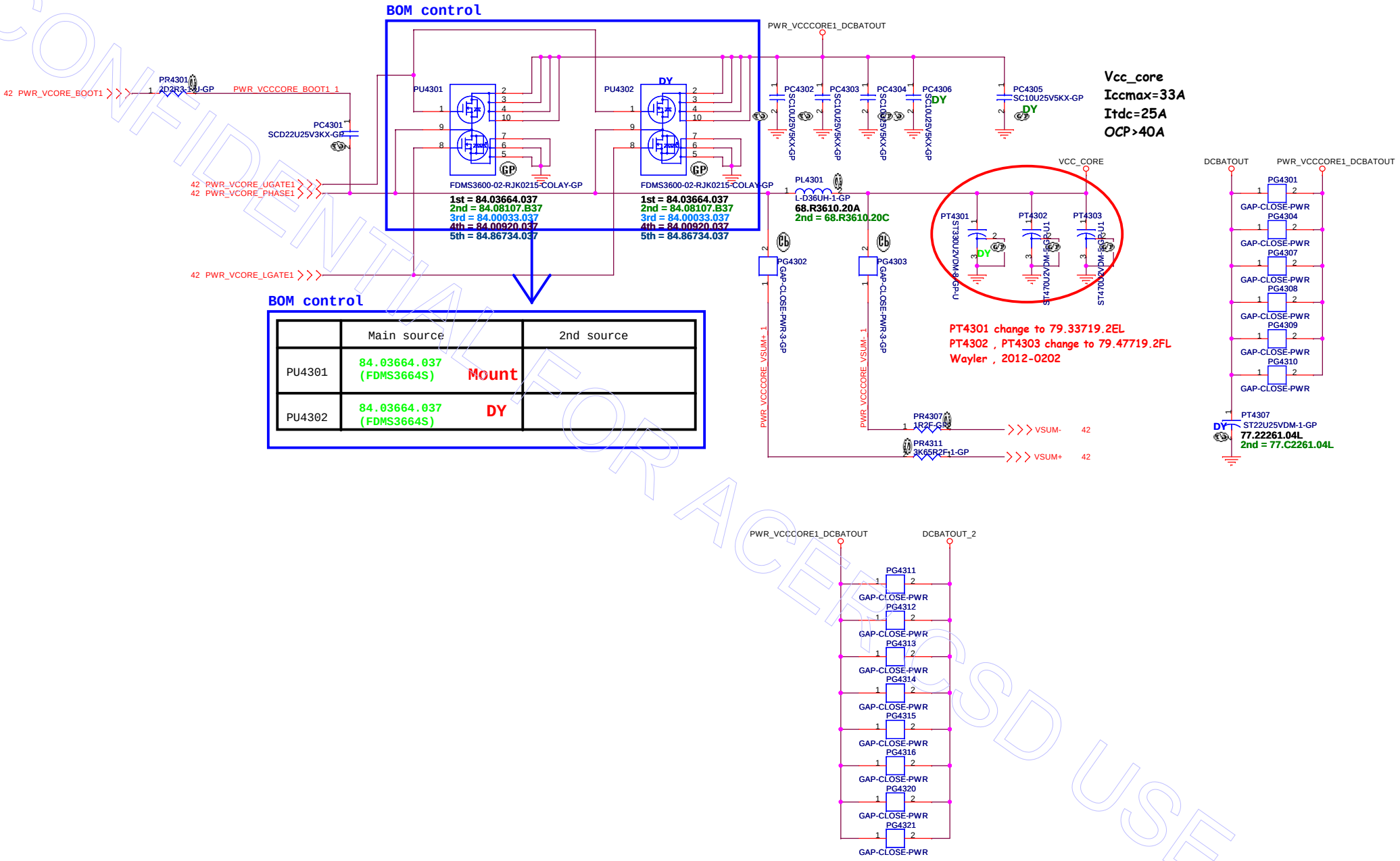
DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(1/3)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 42 of 102



BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

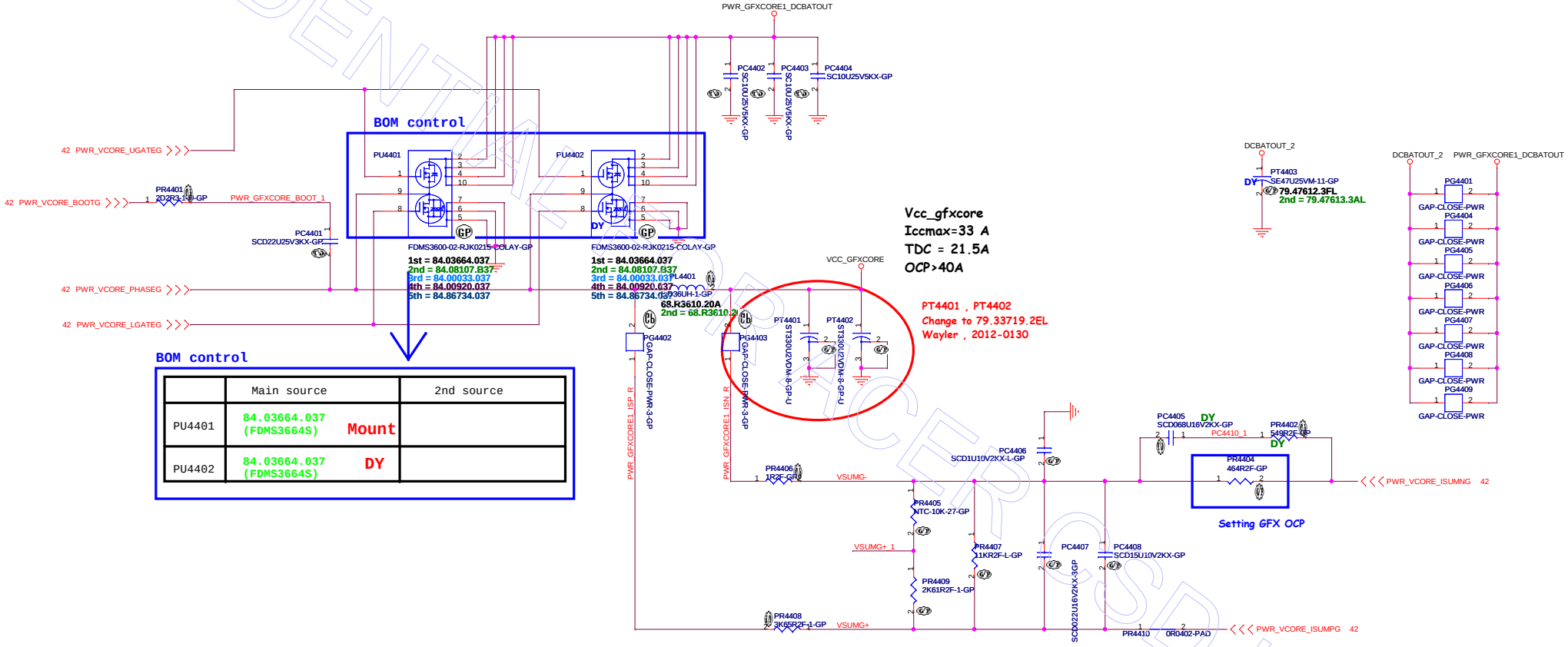
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Monday, September 17, 2012 Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

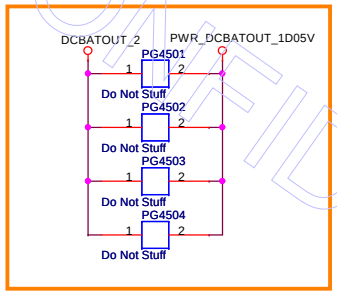
Title: ISL95836_CPU_CORE(3/3)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

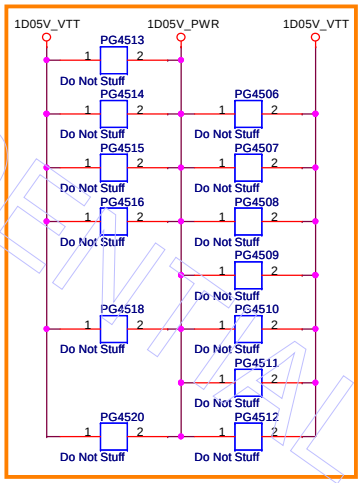
Date: Monday, September 17, 2012 Sheet 44 of 102

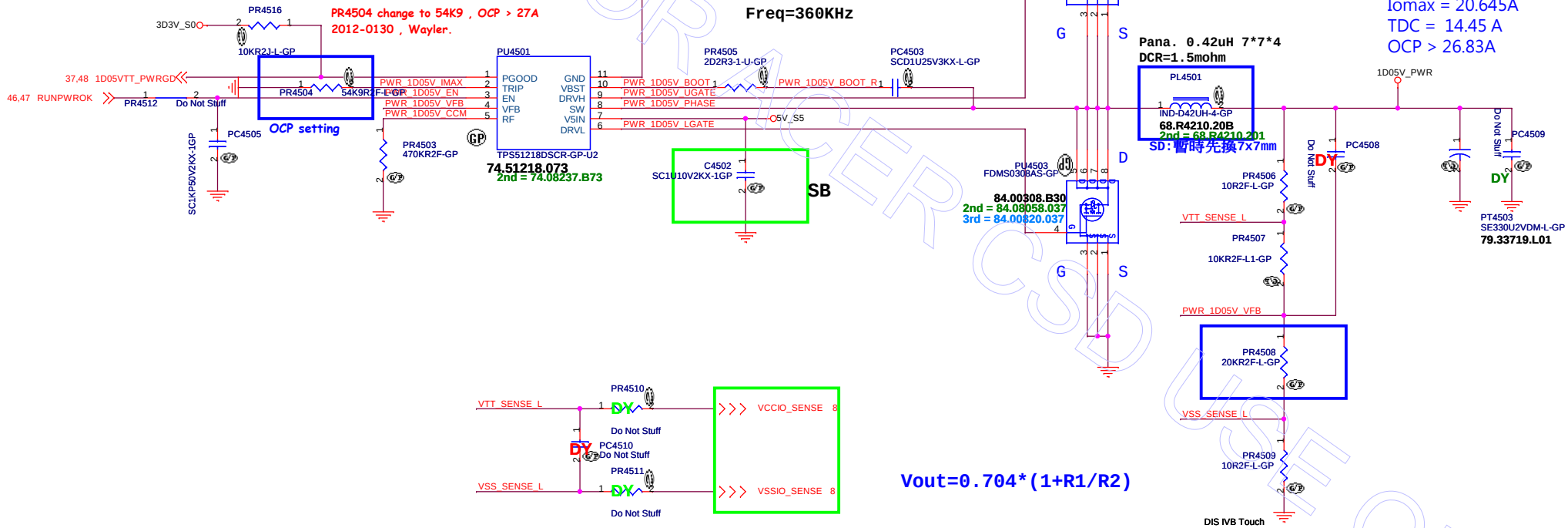
TPS51218D for 1D05V

SA_20111004



SA_20111013





DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v

Change power source

SA_20111004

SC:delete PT4601

RT8207L for 1D5V

OCP setting

PR4603 change to 8K87 , OCP>24A
2012 - 0111 - Wayler

Close to pin23

20100728

Close to pin23

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 change to 74.08207.D73
2012 - 0111 - Wayler

PR4608 change to 30.9K
2012 - 0111 - Wayler

Close to PIN9

+0.75VS
Iomax: 1.2A

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

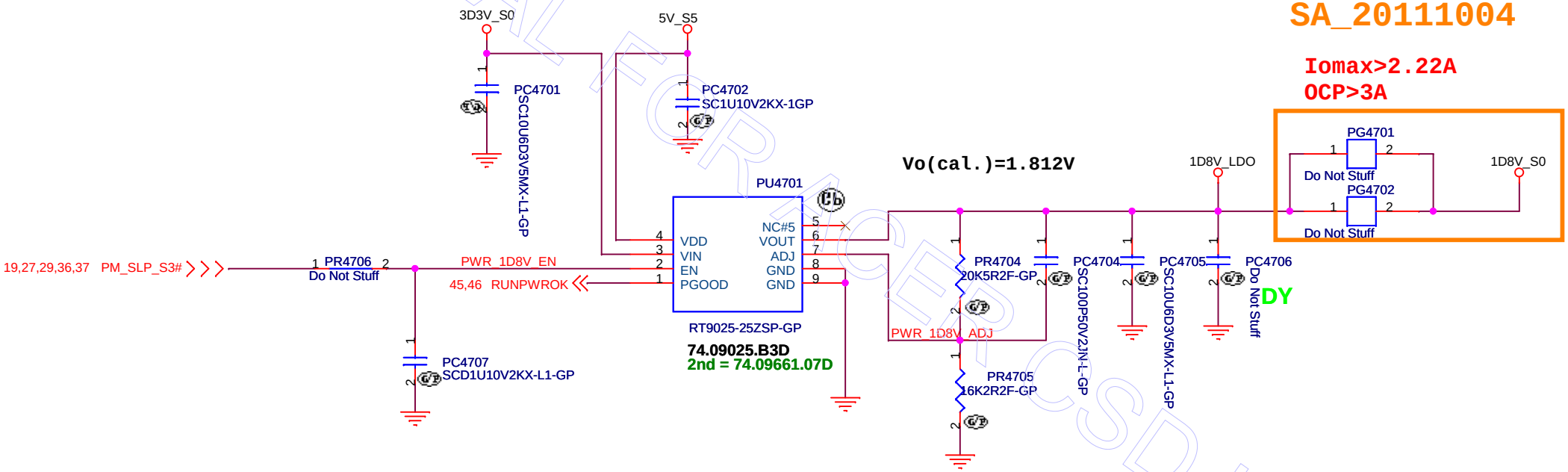
SD:暫時先換7x7mm

Vout=0.75*(1+R1/R2)

DIS IVB Touch	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8207
Size: Custom	Document Number: Husk/Petra
Rev	-4M
Date: Thursday, September 06, 2012	Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

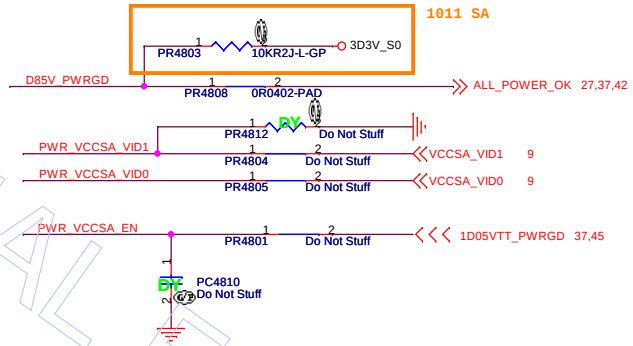
RT9025 for 1D8V_S0



DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 47 of 103	

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O MODE=0	V_O MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

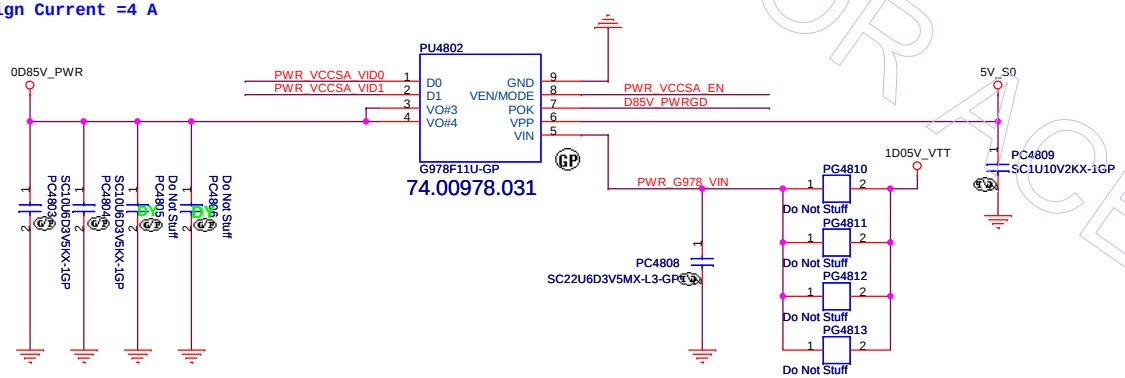
"x" means "don't care".

VEN/MODE Logic

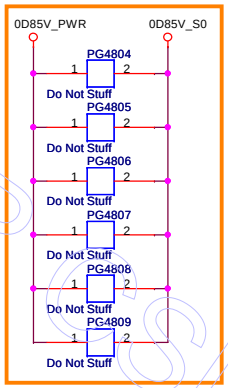
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



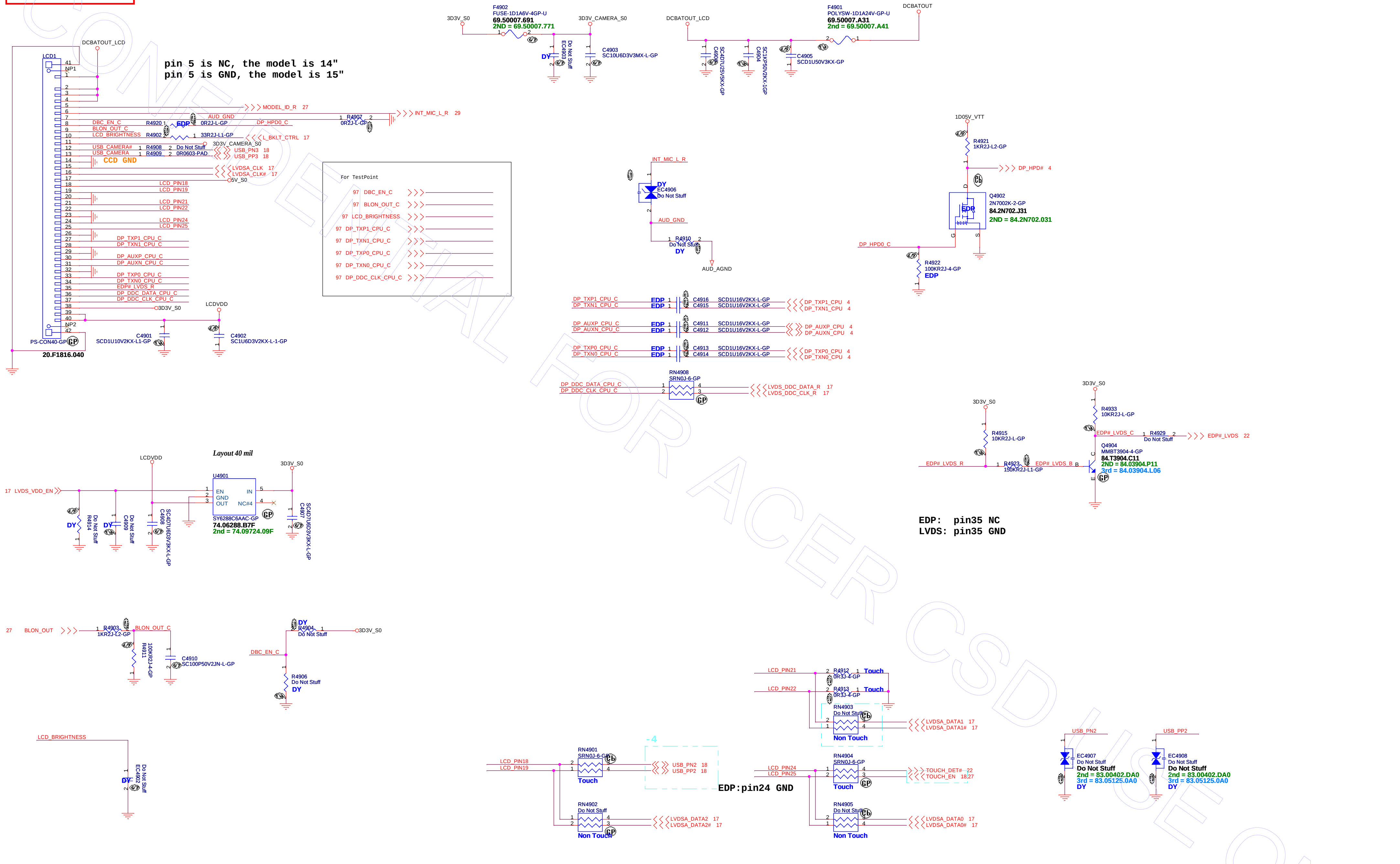
1011 SA



DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VCCSA LDO G978		
Size: A3	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 48 of 103	

SSID = VIDEO



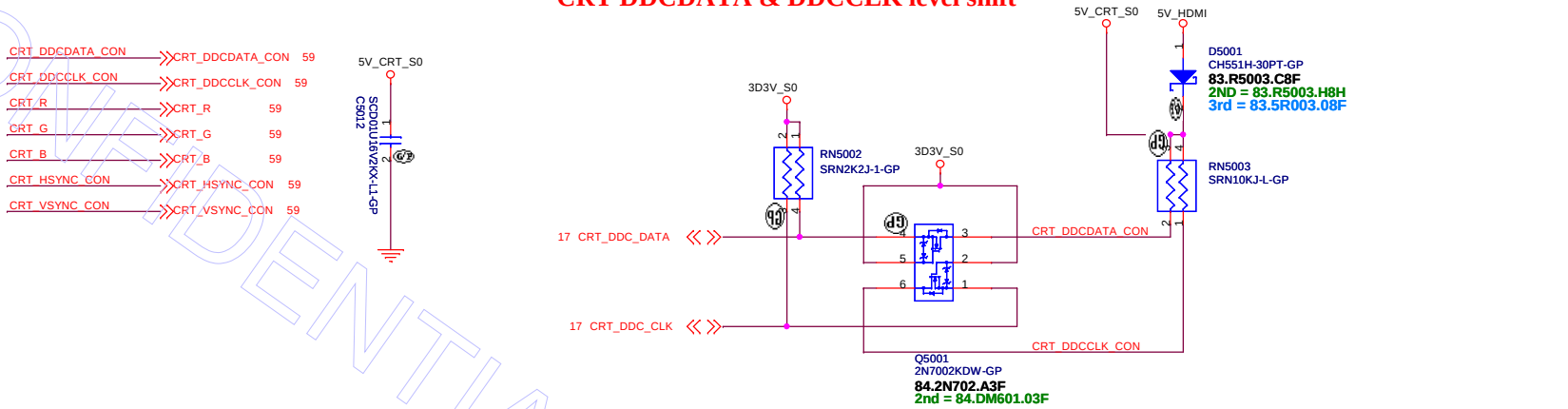
pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"
DCBATOUT_LCD
LCD1
PS-CON40-GP
20.F1816.040
MODEL_ID_R 27
INT_MIC_L_R 29
AUD_GND
DBC_EN_C
BLON_OUT_C
LCD_BRIGHTNESS
DP_HPD0_C
R4920 0R2J-L-GP
R4907 0R2J-L-GP
R4902 33R2J-L1-GP
L_BKLT_CTRL 17
3D3V_CAMERA_S0
USB_CAMERA#
USB_CAMERA
R4908 Do Not Stuff
R4909 0R0603-PAD
USB_PN3 18
USB_PP3 18
CCD GND
LVDSA_CLK 17
LVDSA_CLK# 17
5V_S0
LCD_PIN18
LCD_PIN19
LCD_PIN21
LCD_PIN22
LCD_PIN24
LCD_PIN25
DP_TXP1_CPU_C
DP_TXN1_CPU_C
DP_AUXP_CPU_C
DP_AUXN_CPU_C
DP_TXP0_CPU_C
DP_TXN0_CPU_C
EDP#_LVDS_R
DP_DDC_DATA_CPU_C
DP_DDC_CLK_CPU_C
3D3V_S0
LCDVDD
C4901 SC1U10V2KX-L1-GP
C4902 SC1U6D3V2KX-L-1-GP
For TestPoint
97 DBC_EN_C
97 BLON_OUT_C
97 LCD_BRIGHTNESS
97 DP_TXP1_CPU_C
97 DP_TXN1_CPU_C
97 DP_TXP0_CPU_C
97 DP_TXN0_CPU_C
97 DP_DDC_CLK_CPU_C
3D3V_S0
F4902
FUSE-1D1A6V-4GP-U
69.50007.691
2ND = 69.50007.771
3D3V_CAMERA_S0
EC4903 Do Not Stuff
C4903 SC10U6D3V3MX-L-GP
DCBATOUT_LCD
C4906 SC4D7U25V5KX-GP
C4904 SC1KP50V2KX-1GP
C4905 SCD1U50V3KX-GP
F4901
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.A41
DCBATOUT
INT_MIC_L_R
EC4906 Do Not Stuff
AUD_GND
R4910 Do Not Stuff
AUD_AGND
1D05V_VTT
R4921 1KR2J-L2-GP
DP_HPD# 4
Q4902
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
DP_HPD0_C
R4922 100KR2J-4-GP
EDP
C4916 SCD1U16V2KX-L-GP
C4915 SCD1U16V2KX-L-GP
DP_TXP1_CPU 4
DP_TXN1_CPU 4
C4911 SCD1U16V2KX-L-GP
C4912 SCD1U16V2KX-L-GP
DP_AUXP_CPU 4
DP_AUXN_CPU 4
C4913 SCD1U16V2KX-L-GP
C4914 SCD1U16V2KX-L-GP
DP_TXP0_CPU 4
DP_TXN0_CPU 4
RN4908 SRN0J-6-GP
LVDS_DDC_DATA_R 17
LVDS_DDC_CLK_R 17
3D3V_S0
R4933 10KR2J-L-GP
EDP#_LVDS_C
R4929 Do Not Stuff
EDP#_LVDS 22
R4915 10KR2J-L-GP
Q4904
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06
EDP#_LVDS_R
R4923 150KR2J-L1-GP
EDP#_LVDS_B
EDP: pin35 NC
LVDS: pin35 GND
Layout 40 mil
LCDVDD
U4901
EN
GND
OUT
IN
NC#4
SY6288C6AAC-GP
74.06288.B7F
2nd = 74.09724.09F
17 LVDS_VDD_EN
R4914 Do Not Stuff
C4909 Do Not Stuff
C4908 SC4D7U6D3V3KX-L-GP
C4907 SC4D7U6D3V3KX-L-GP
27 BLON_OUT
R4903 1KR2J-L2-GP
BLON_OUT_C
R4911 100KR2J-4-GP
C4910 SC100P50V2JN-L-GP
R4904 Do Not Stuff
DBC_EN_C
R4906 Do Not Stuff
LCD_BRIGHTNESS
EC4902 Do Not Stuff
LCD_PIN21
LCD_PIN22
R4912 0R3J-4-GP Touch
R4913 0R3J-4-GP Touch
RN4903 Do Not Stuff Non Touch
LVDSA_DATA1 17
LVDSA_DATA1# 17
LCD_PIN18
LCD_PIN19
RN4901 SRN0J-6-GP Touch
USB_PN2 18
USB_PP2 18
EDP:pin24 GND
RN4902 Do Not Stuff Non Touch
LVDSA_DATA2 17
LVDSA_DATA2# 17
LCD_PIN24
LCD_PIN25
RN4904 SRN0J-6-GP Touch
TOUCH_DET# 22
TOUCH_EN 18,27
RN4905 Do Not Stuff Non Touch
LVDSA_DATA0 17
LVDSA_DATA0# 17
USB_PN2
EC4907 Do Not Stuff
Do Not Stuff
2nd = 83.00402.DA0
3rd = 83.05125.0A0
USB_PP2
EC4908 Do Not Stuff
Do Not Stuff
2nd = 83.00402.DA0
3rd = 83.05125.0A0

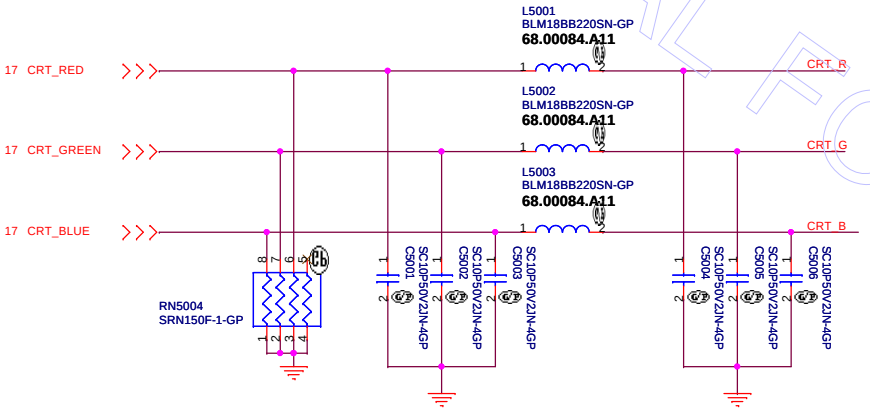
DIS IVB Touch

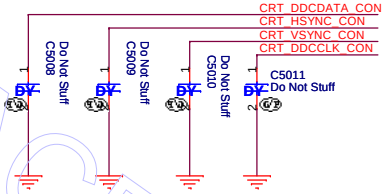
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

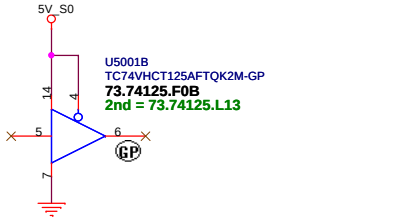
Title		
LCD Connector		
Size A2	Document Number Husk/Petra	Rev -4M
Date: Thursday, September 06, 2012	Sheet 49 of 103	

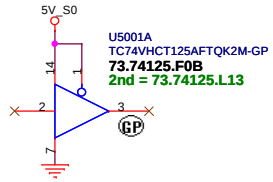
CRT DDCDATA & DDCCLK level shift

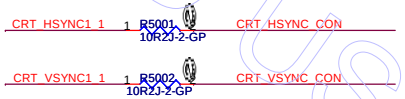


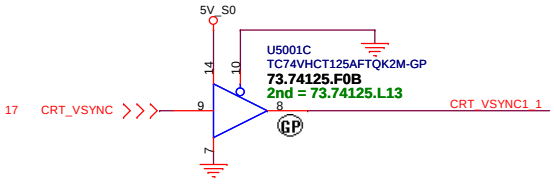


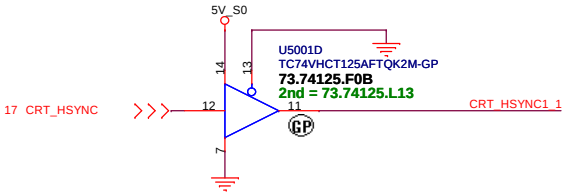












DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

HDMI_DATA2_R#
HDMI_DATA2_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_CLK_R
HDMI_CLK_R#

RN5114
SRN499F-GP

RN5115
SRN499F-GP

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

HDMI1
SKT-HDMI23-45-GP
22.10296.631
2nd = 22.10296.821

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI

5V_HDMI
5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771

HPD_HDMI_CON
R5111
150KR2J-L1-GP
HDMI_HPD_B

3D3V_S0
Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06

R5110
Do Not Stuff

HDMI_HPD_E
R5129
Do Not Stuff
HDMI_PCH_DET 17

R5112
10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011

5V_S0_D1
5V_S0_D2
5V_S0

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

3D3V_S0

RN5102
SRN2K2J-1-GP

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

DDC_CLK_HDMI
DDC_DATA_HDMI

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 52 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **S-VIDEO**

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 53 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

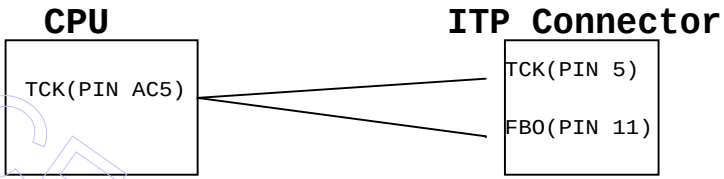
Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

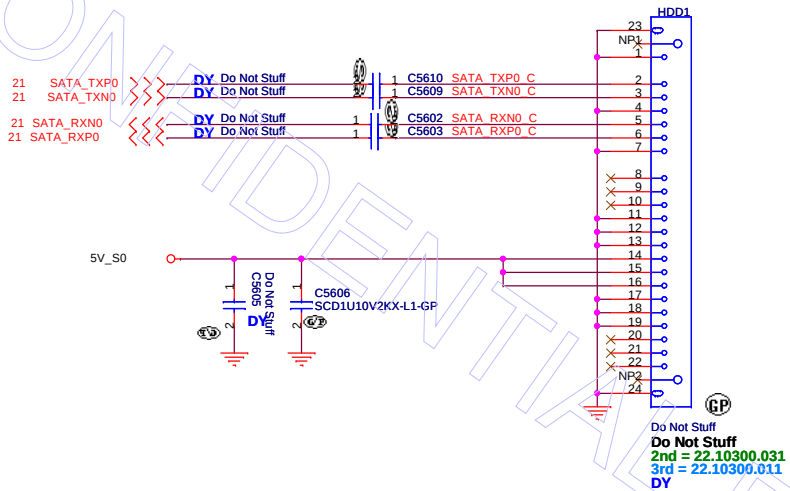
Title: ITP

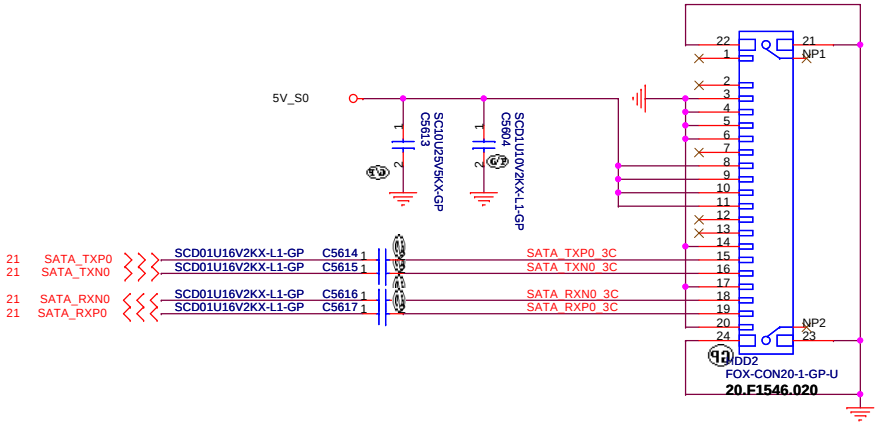
Size: A4 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 55 of 103

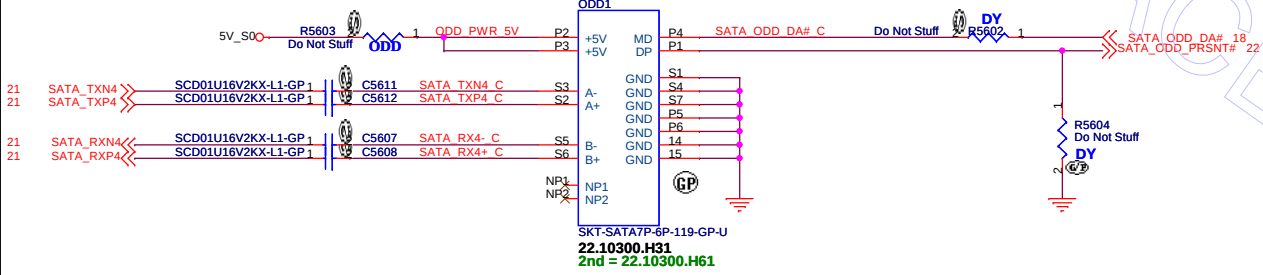
SSID = SATA

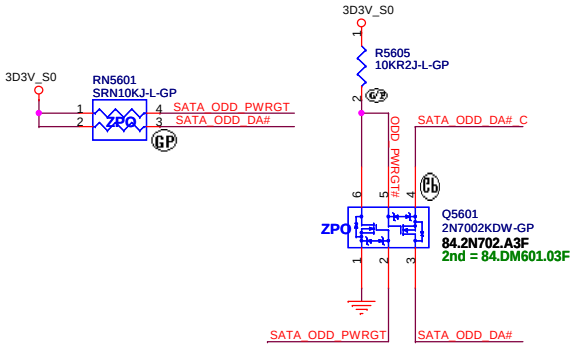
SATA HDD Connector



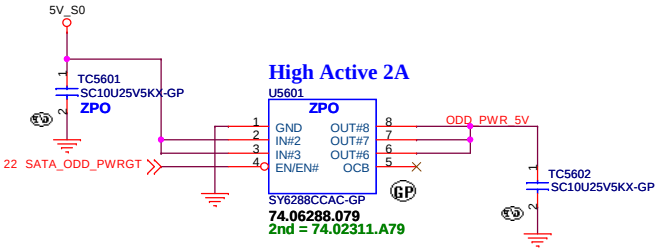


ODD Connector





SATA Zero Power ODD



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 56 of 103

DIS IVB Touch

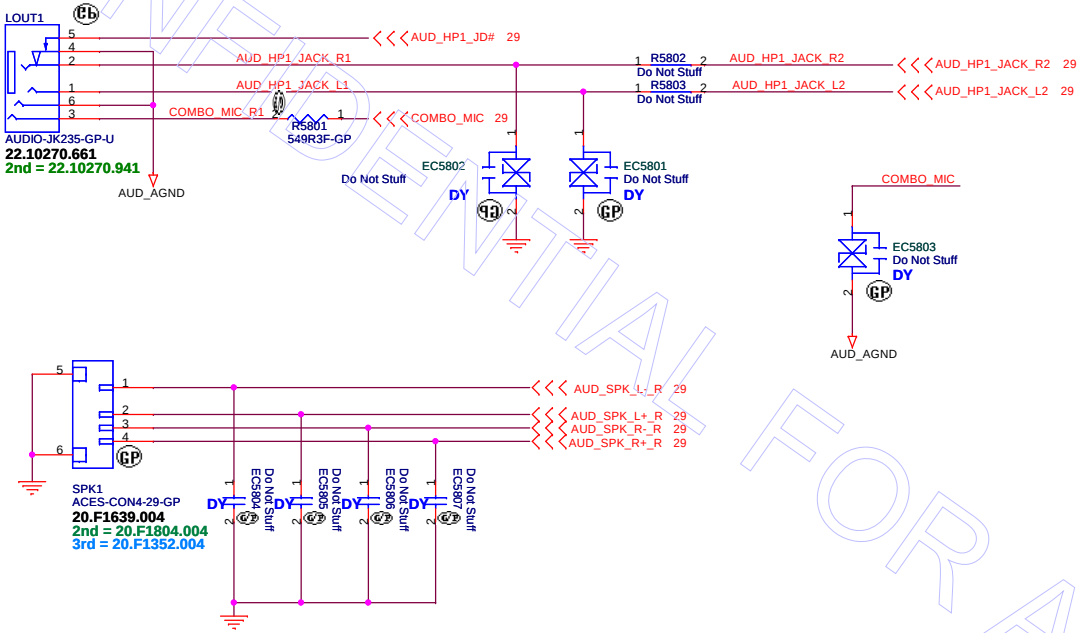
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **E-SATA/USB CHARGER**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 57 of 103

SSID = AUDIO



DIS IVB Touch

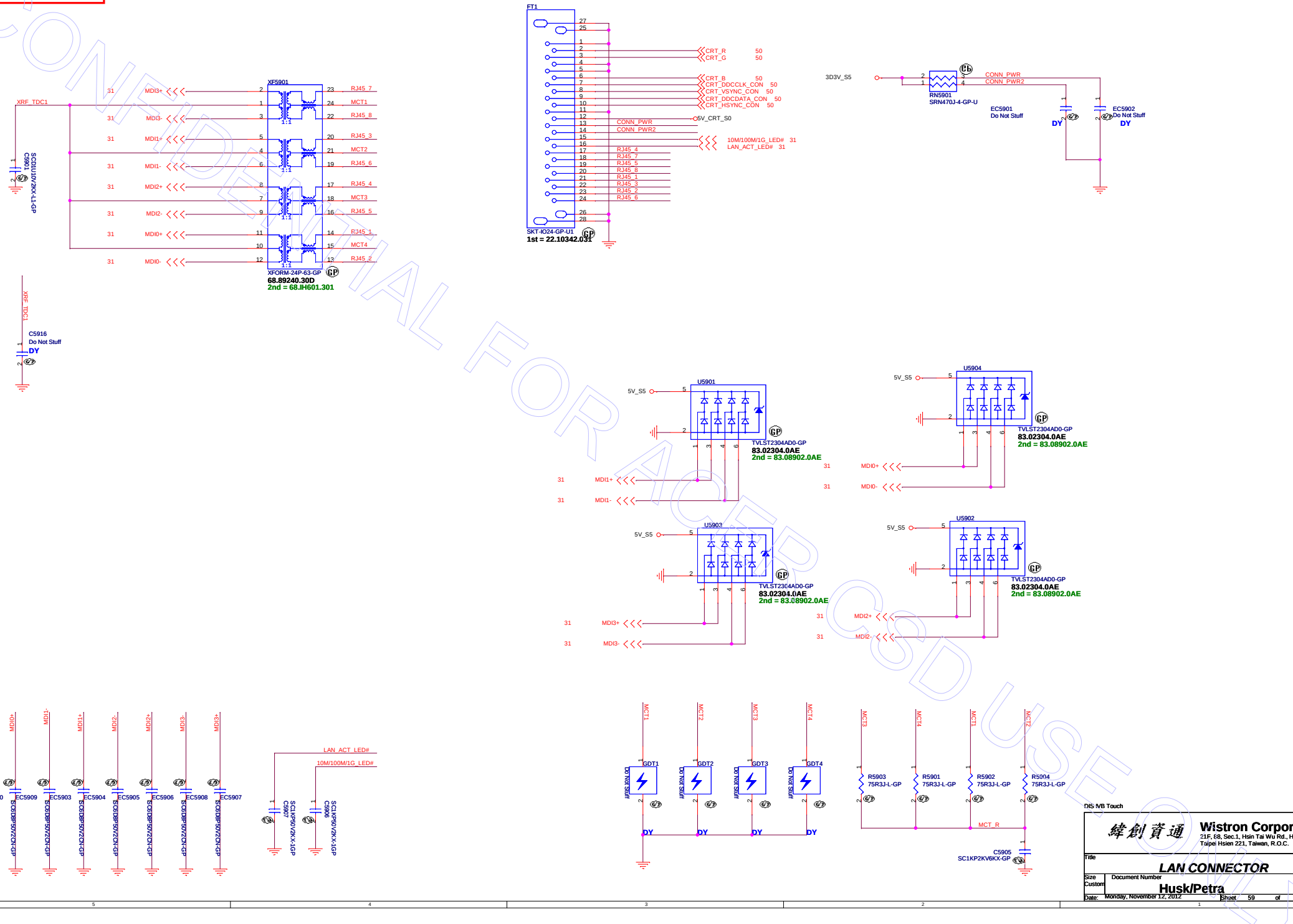
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio Jack***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 58 of 103

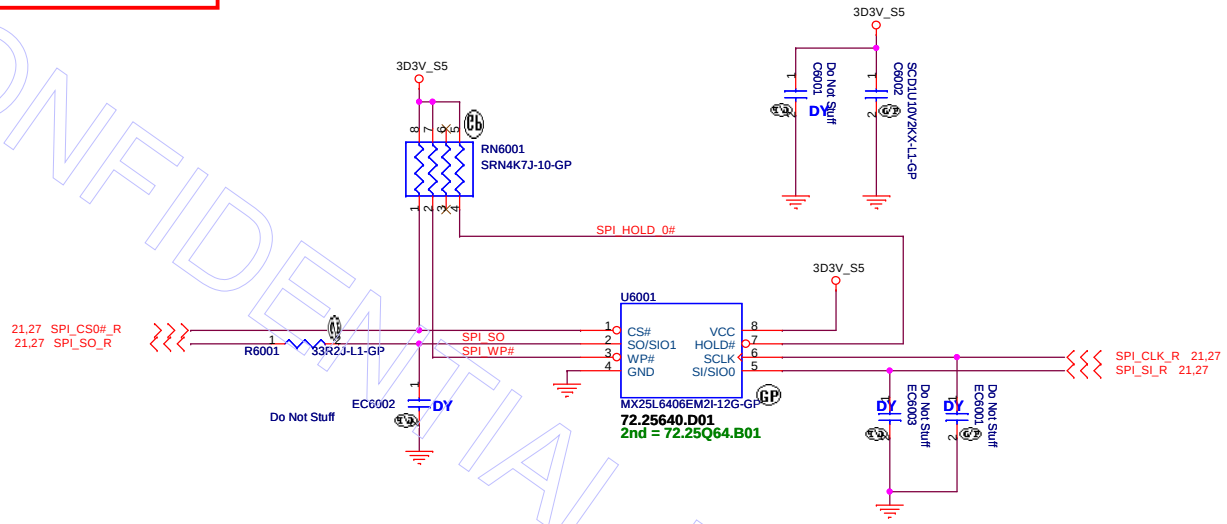
SSID = LAN



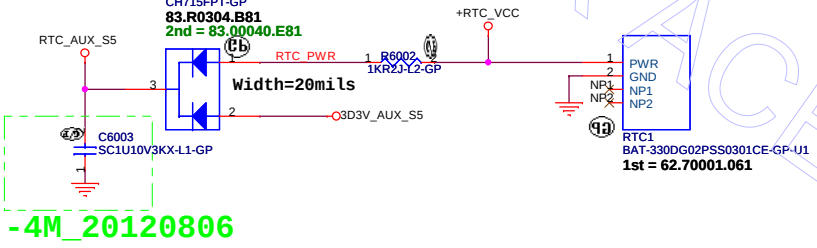
DIS IVB Touch

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **LAN CONNECTOR**		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Monday, November 12, 2012	Sheet 59 of 103	

SSID = Flash.ROM



SSID = RTC



-4M_20120806

DIS IVB Touch

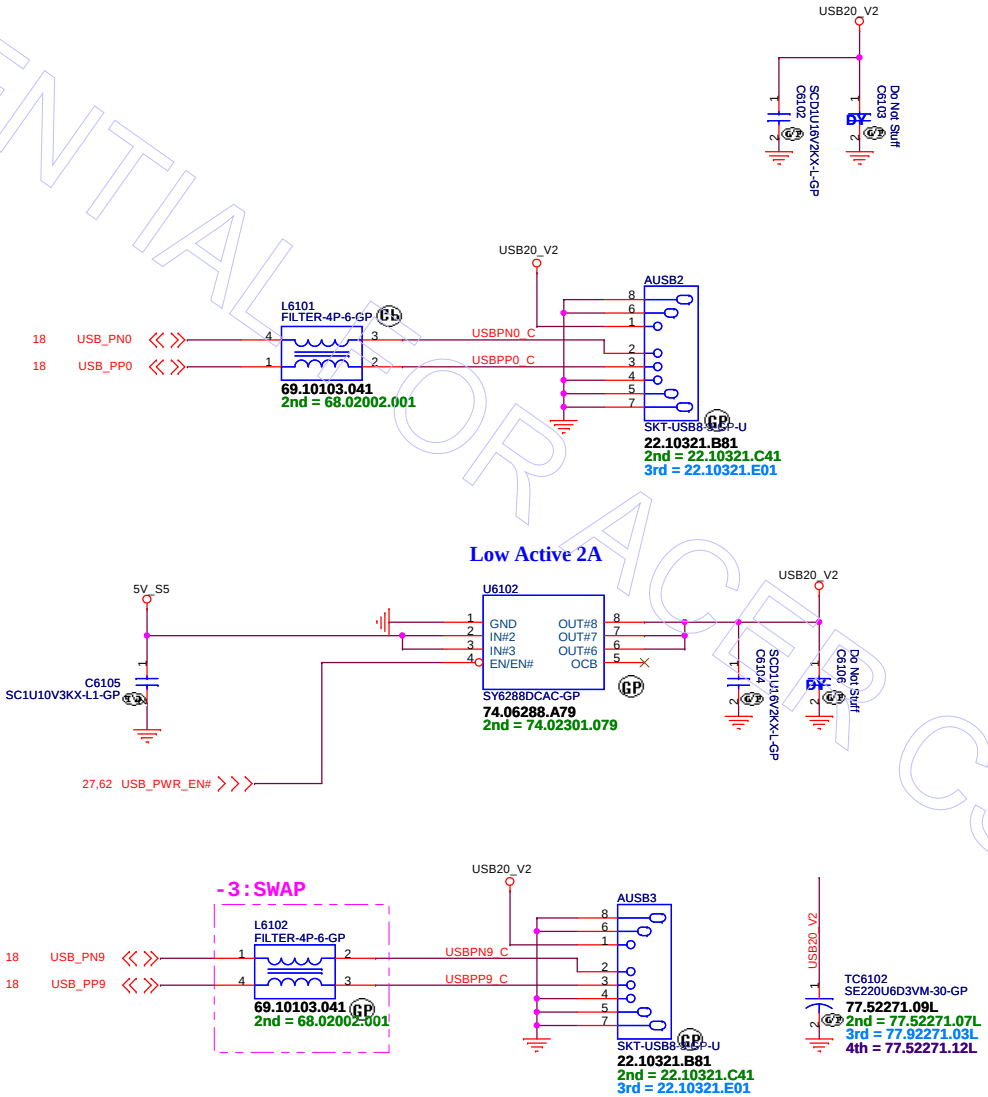
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash/RTC***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 60 of 103

SSID = USB



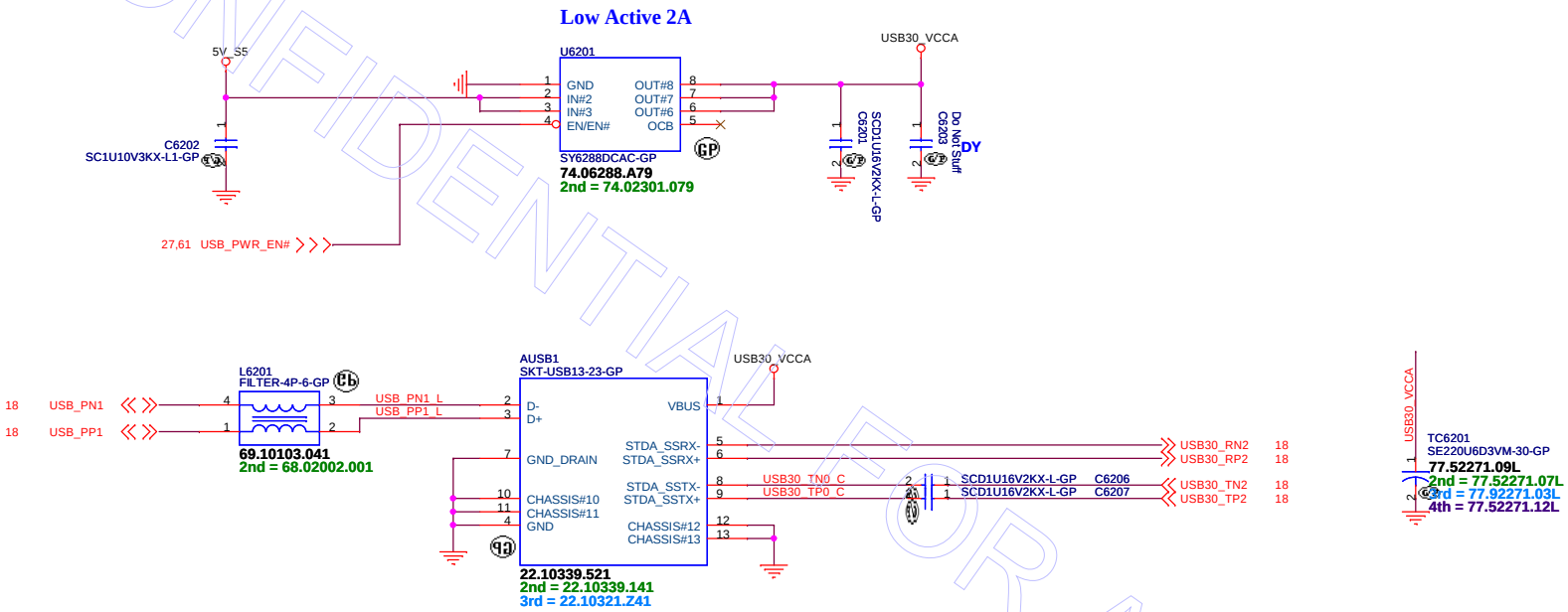
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 13, 2012 Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 13, 2012 | Sheet 62 of 103

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 63 of 103

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

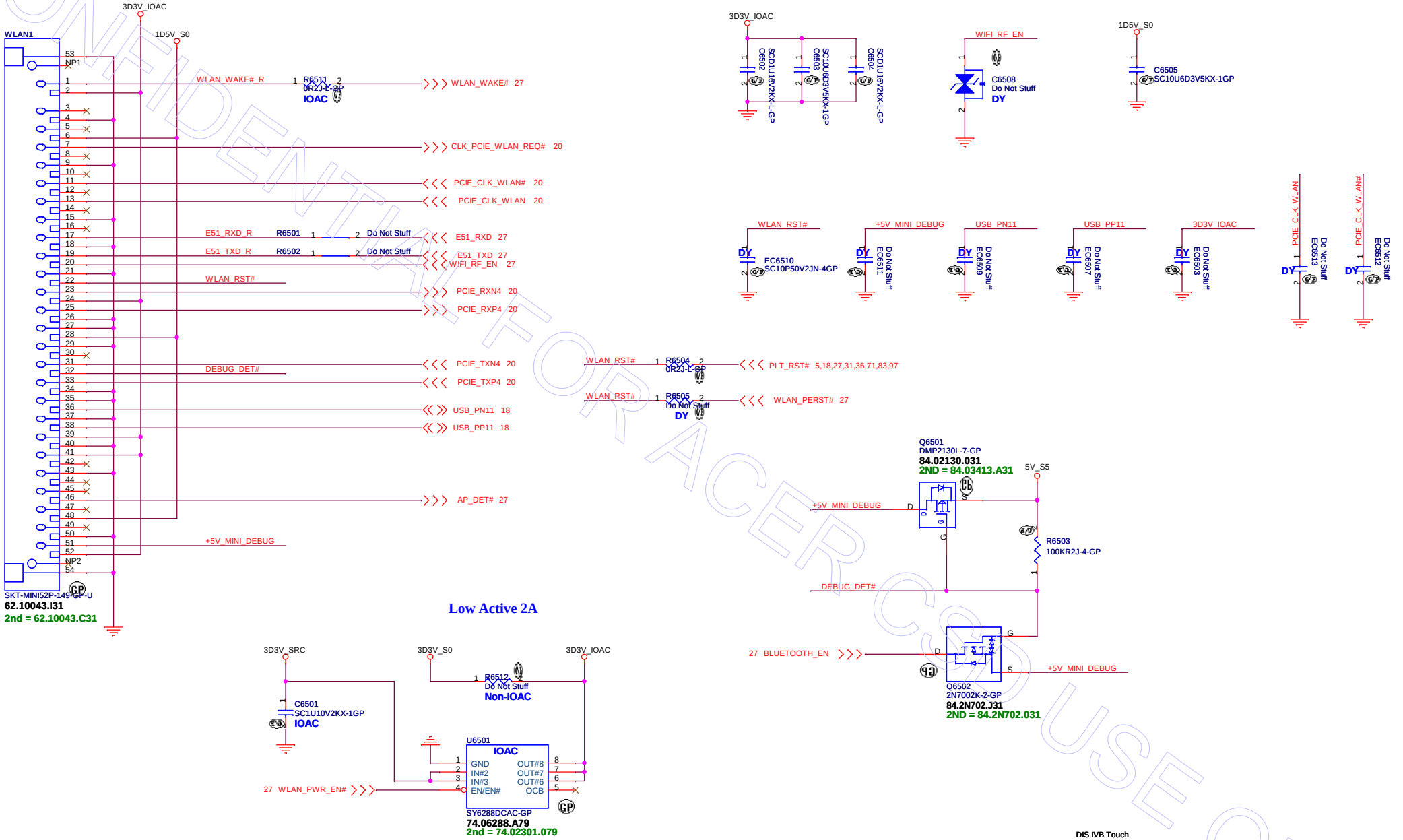
RESERVED

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Friday, December 21, 2012 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 66 of 103

(Blanking)

DIS IVB Touch

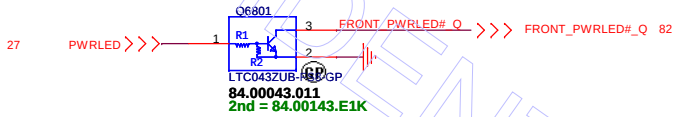
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

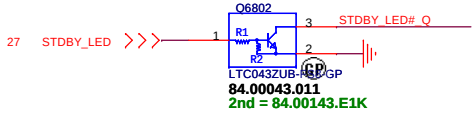
Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 67 of 103

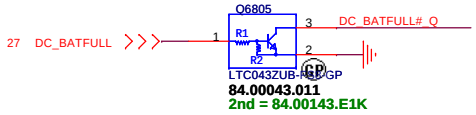
Power button LED



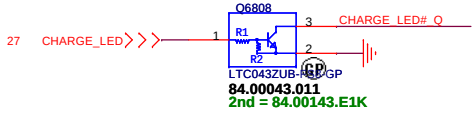
Power STDBY_LED

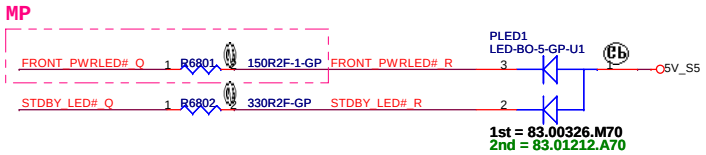


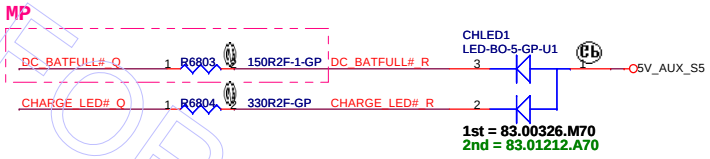
Battery LED2(DC_BATFULL)

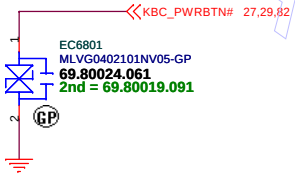


Battery LED1(CHARGE)









DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

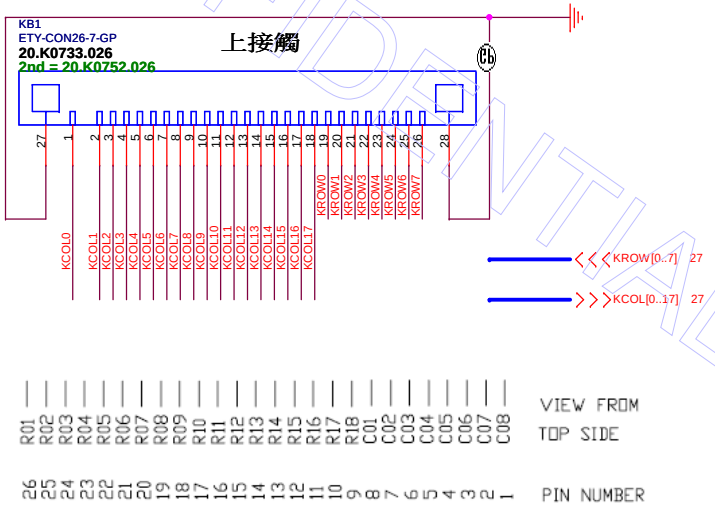
Title: LED Bard/Power Button

Size	Document Number	Rev
Custom	Husk/Petra	-4M

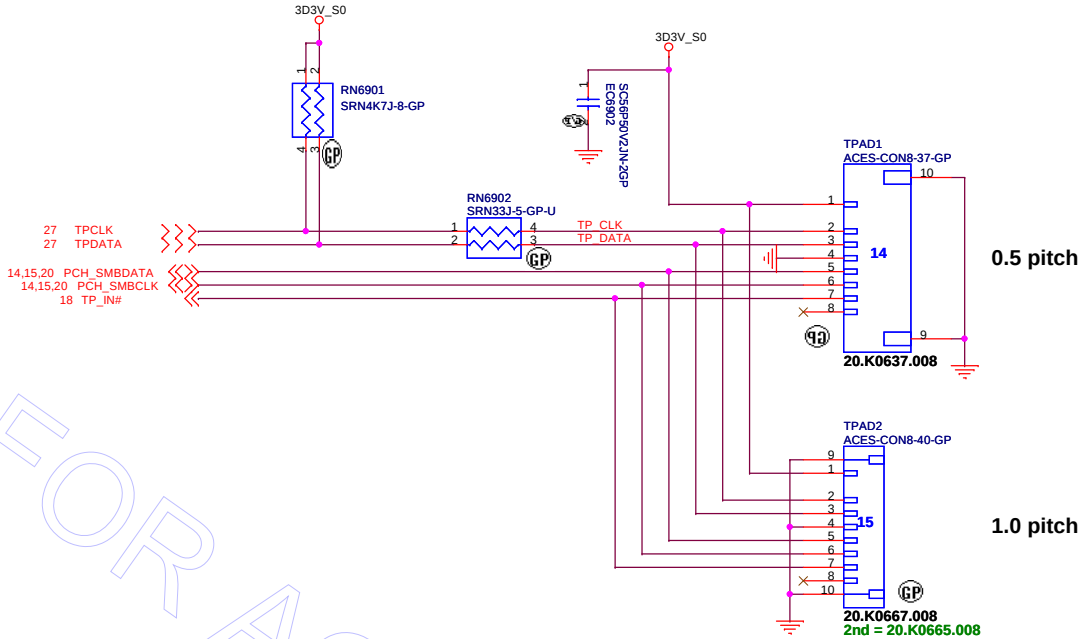
Date: Thursday, September 06, 2012 Sheet 68 of 103

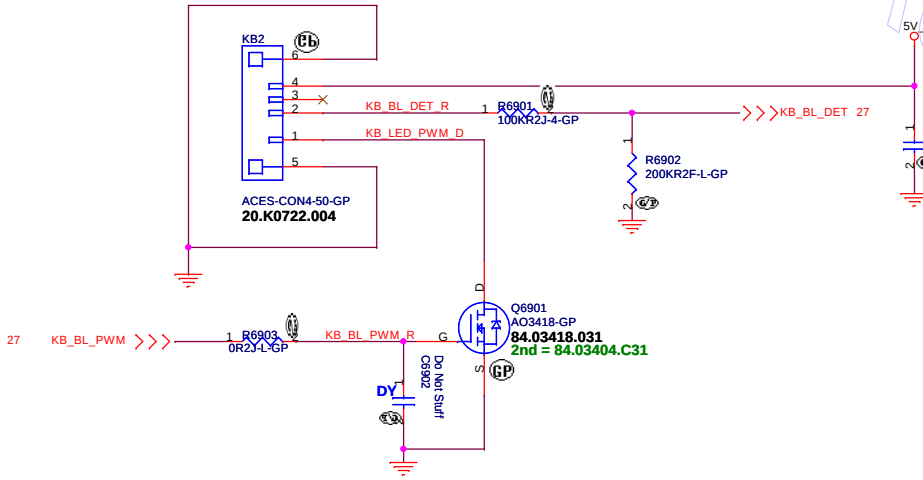
SSID = KBC

Internal KeyBoard Connector



TOUCH PAD





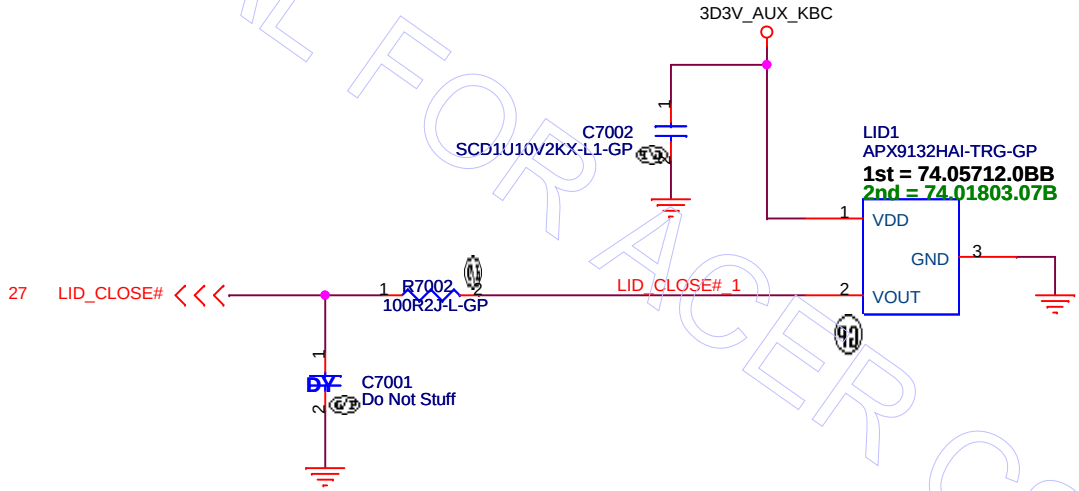
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 69 of 103



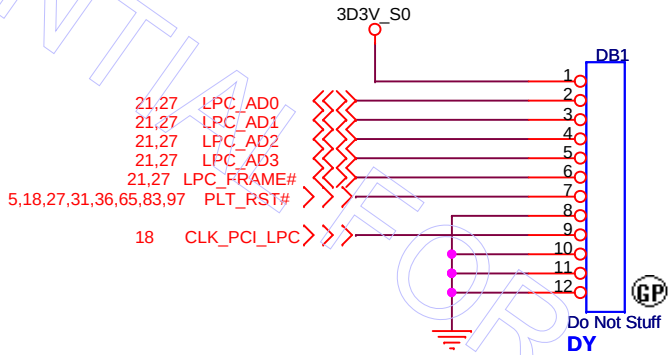
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 70 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 71 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 72 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

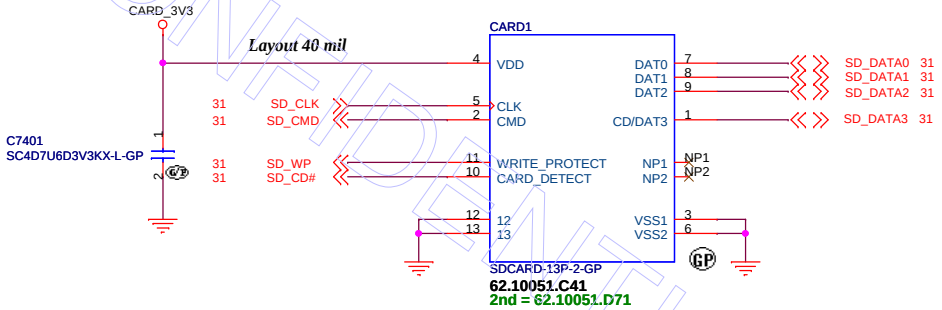
Title: ***Reserved***

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 73 of 103

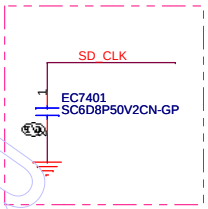
SD/MMC Card Reader

SSID = SDIO



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#

-2:EMI



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 75 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 76 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 77 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G- Sensor

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 79 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 80 of 103

(Blanking)

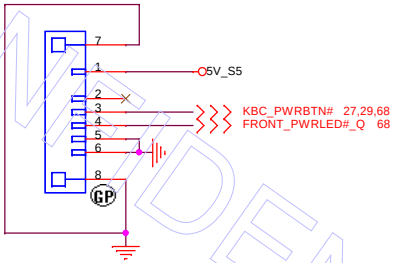
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 81 of 103



PWRCN1
ACES-CON6-52-GP
20.K0721.006
2nd = 20.K0382.006

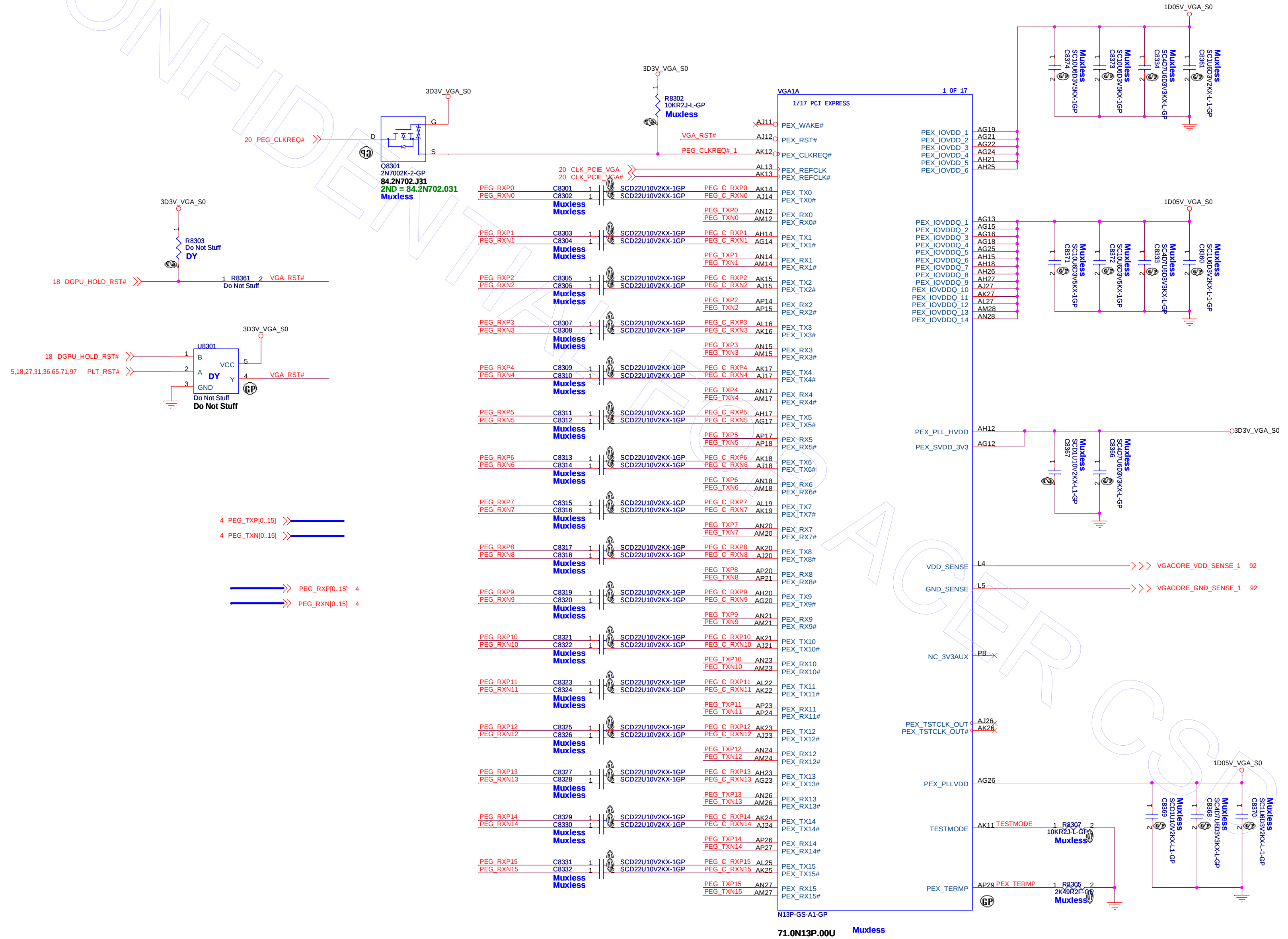
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 82 of 103



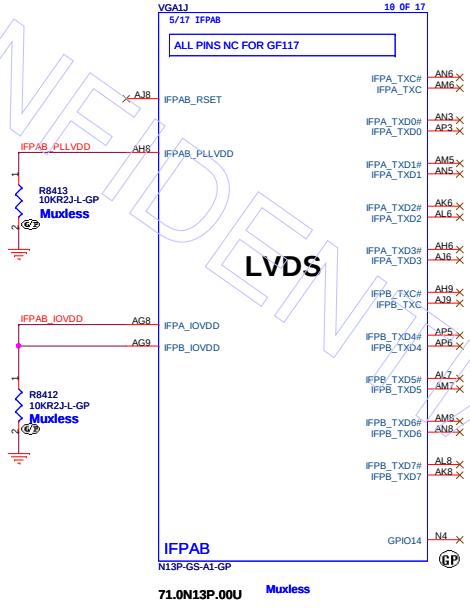
DIS IVB Touch

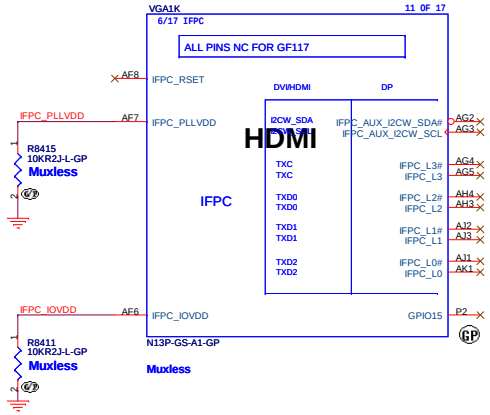
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

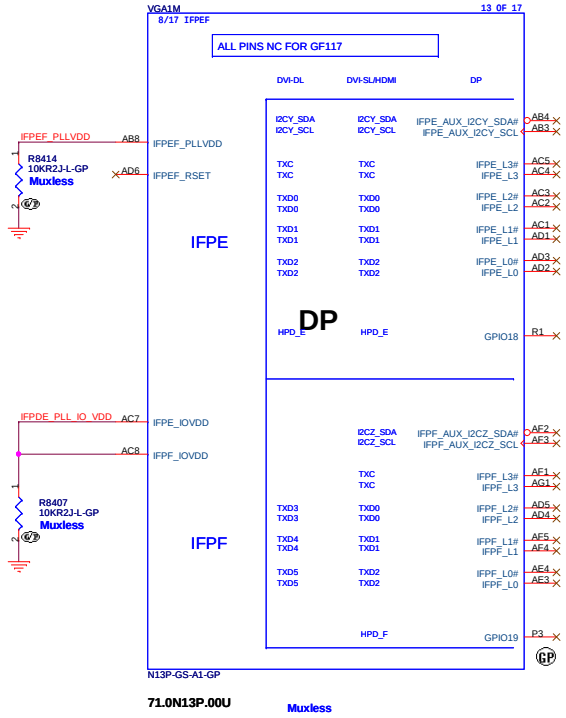
Title
GPU_PCIE/STRAPPING(1/5)

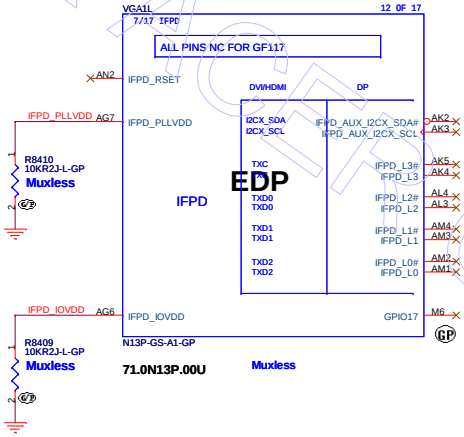
Size A2 | Document Number **Husk/Petra** | Rev **-4M**

Date: Thursday, September 06, 2012 | Sheet 83 of 103







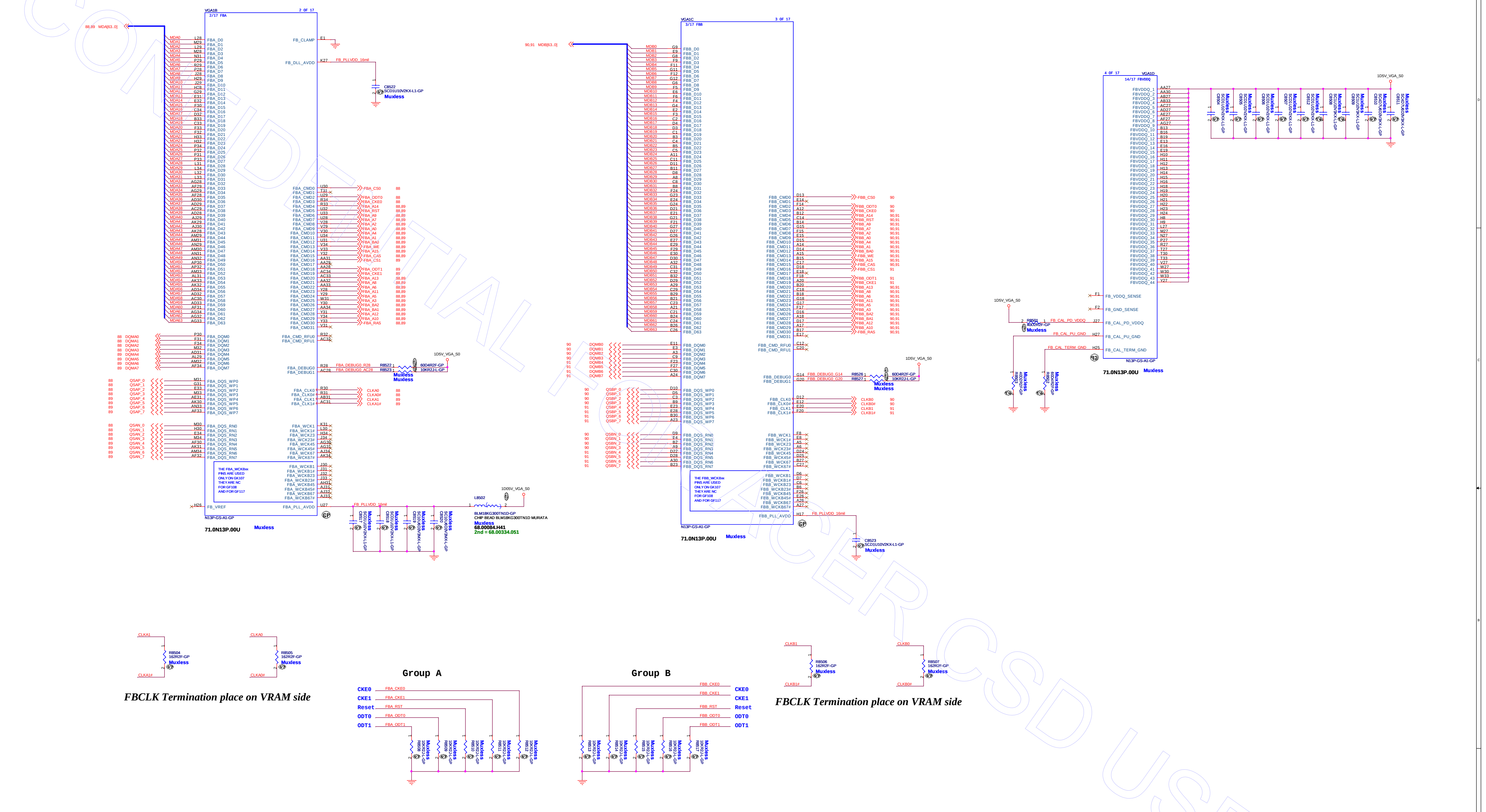


DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	Husk/Petra	-4M
Date: Thursday, September 06, 2012	Sheet 84 of 103	



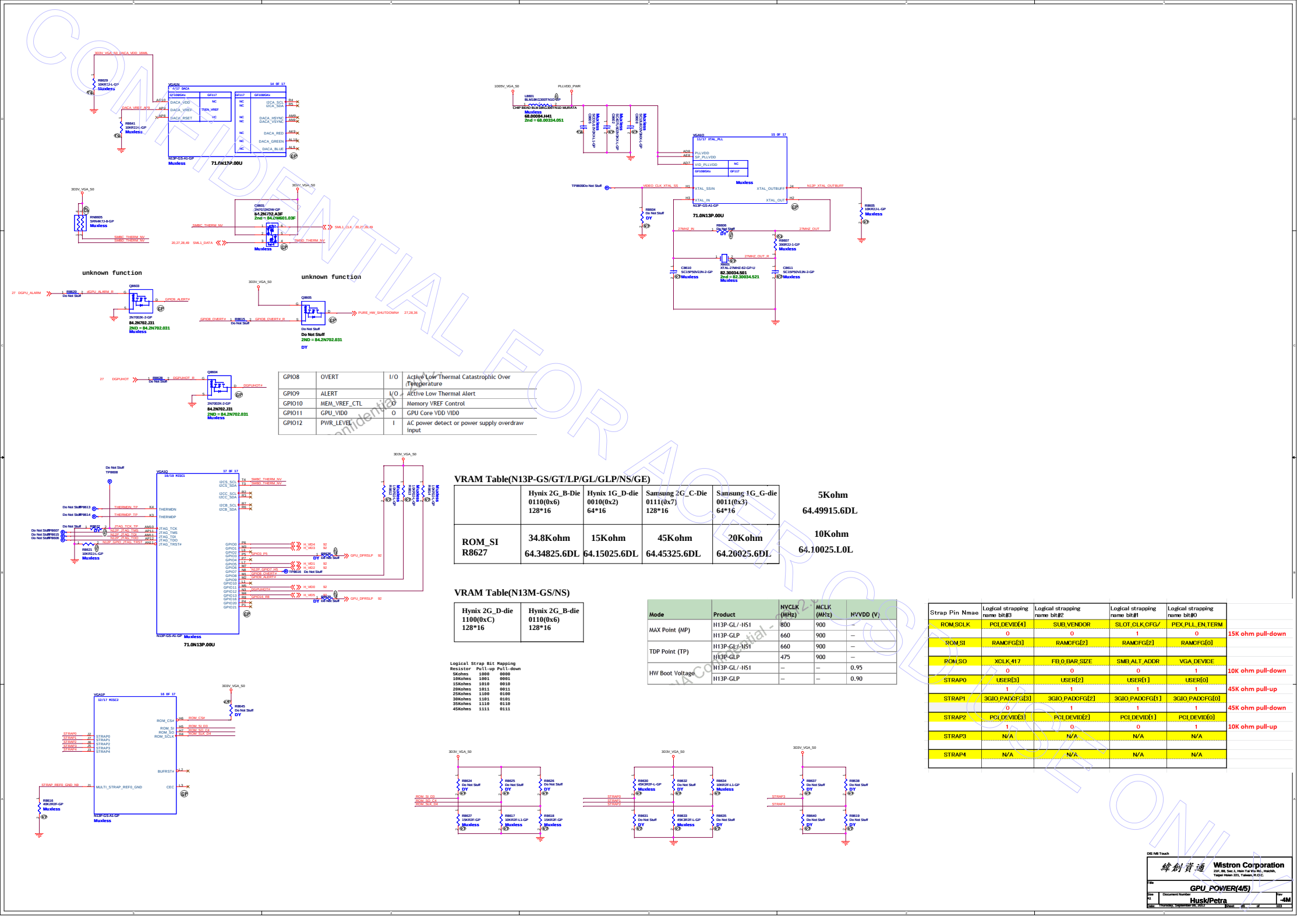
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_DP/LVDS/CRT/GPIO(3/5)**

Size: A1 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 85 of 103



GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input

VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm 64.49915.6DL

10Kohm 64.10025.L0L

VRAM Table(N13M-GS/NS)

Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVDD (V)
MAX Point (MP)	N13P-GL/-NS1	800	900	–
	N13P-GLP	660	900	–
TDP Point (TP)	N13P-GL/-NS1	660	900	–
	N13P-GLP	475	900	–
HW Boot Voltage	N13P-GL/-NS1	–	–	0.95
	N13P-GLP	–	–	0.90

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/	PEX_PLL_EN_TERM	
	0	0	1	0	15K ohm pull-down
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	
	0	0	0	1	10K ohm pull-down
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	1	1	1	45K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	1	0	0	1	10K ohm pull-up
STRAP3	N/A	N/A	N/A	N/A	
STRAP4	N/A	N/A	N/A	N/A	

DIS N8 Touch

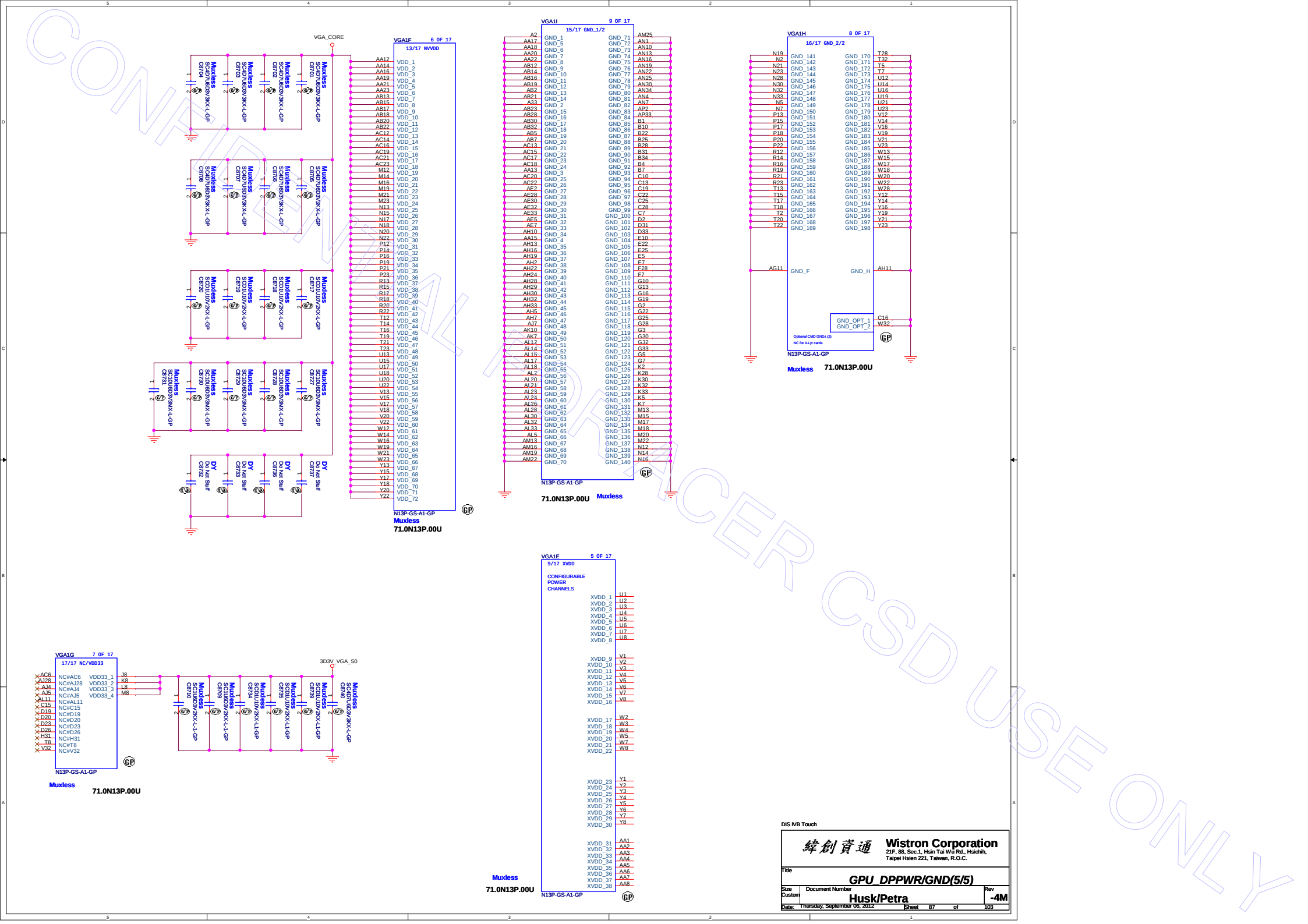
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A1 | Document Number: | Rev: -4M

Husk/Petra

Date: Thursday, September 06, 2012 | Sheet 05 of 103



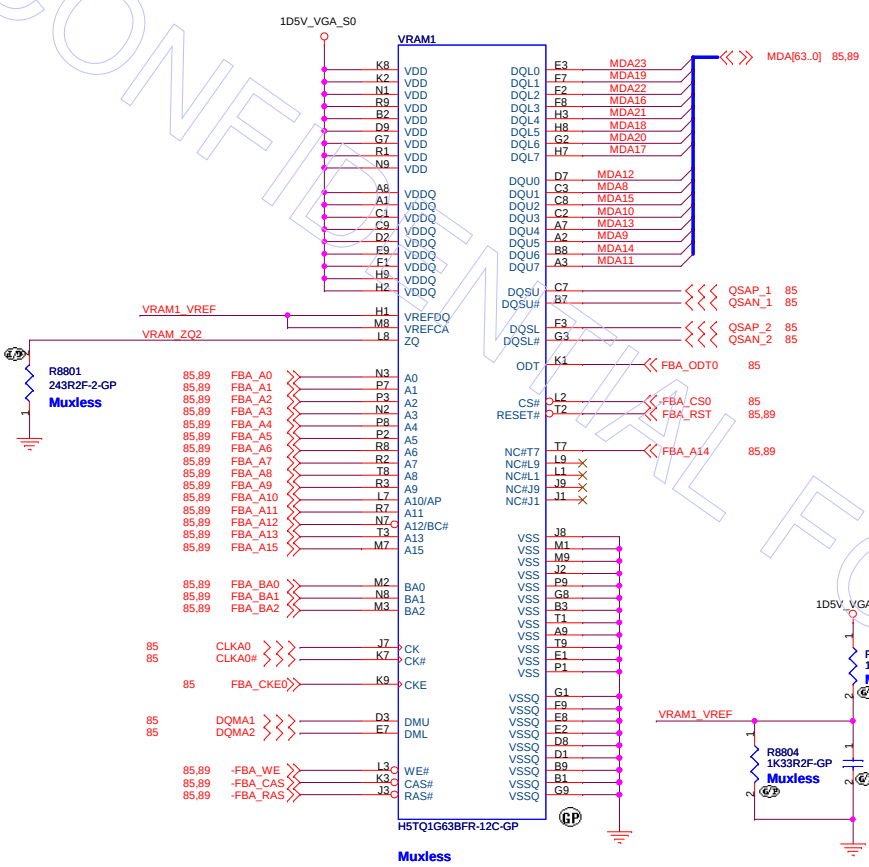
DIS IVB Touch

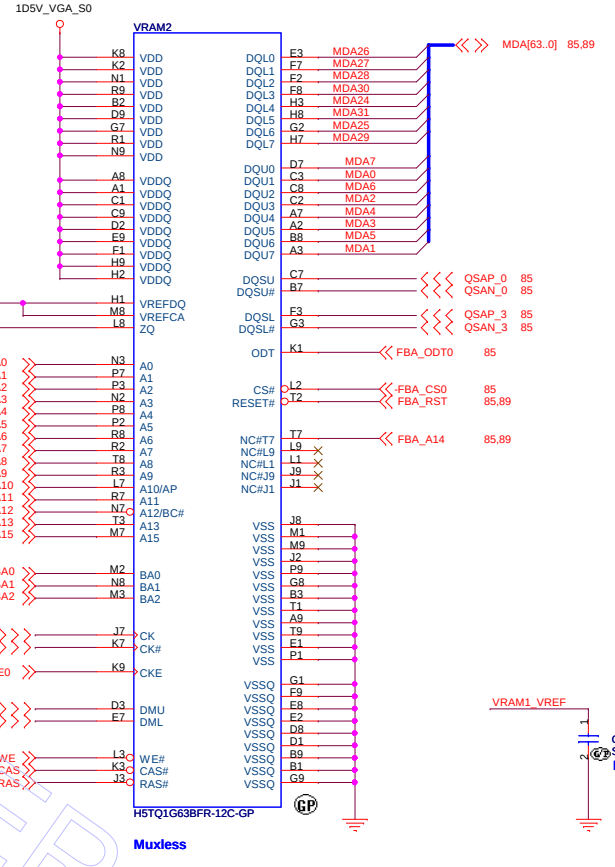
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

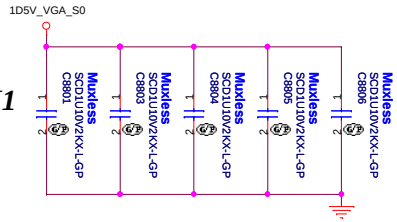
Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 87 of 103

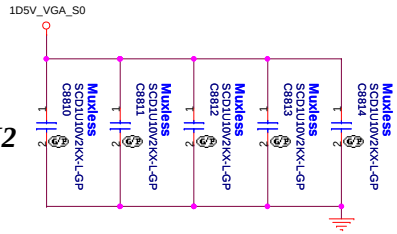


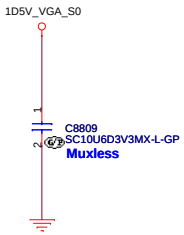


FOR VRAM1



FOR VRAM2





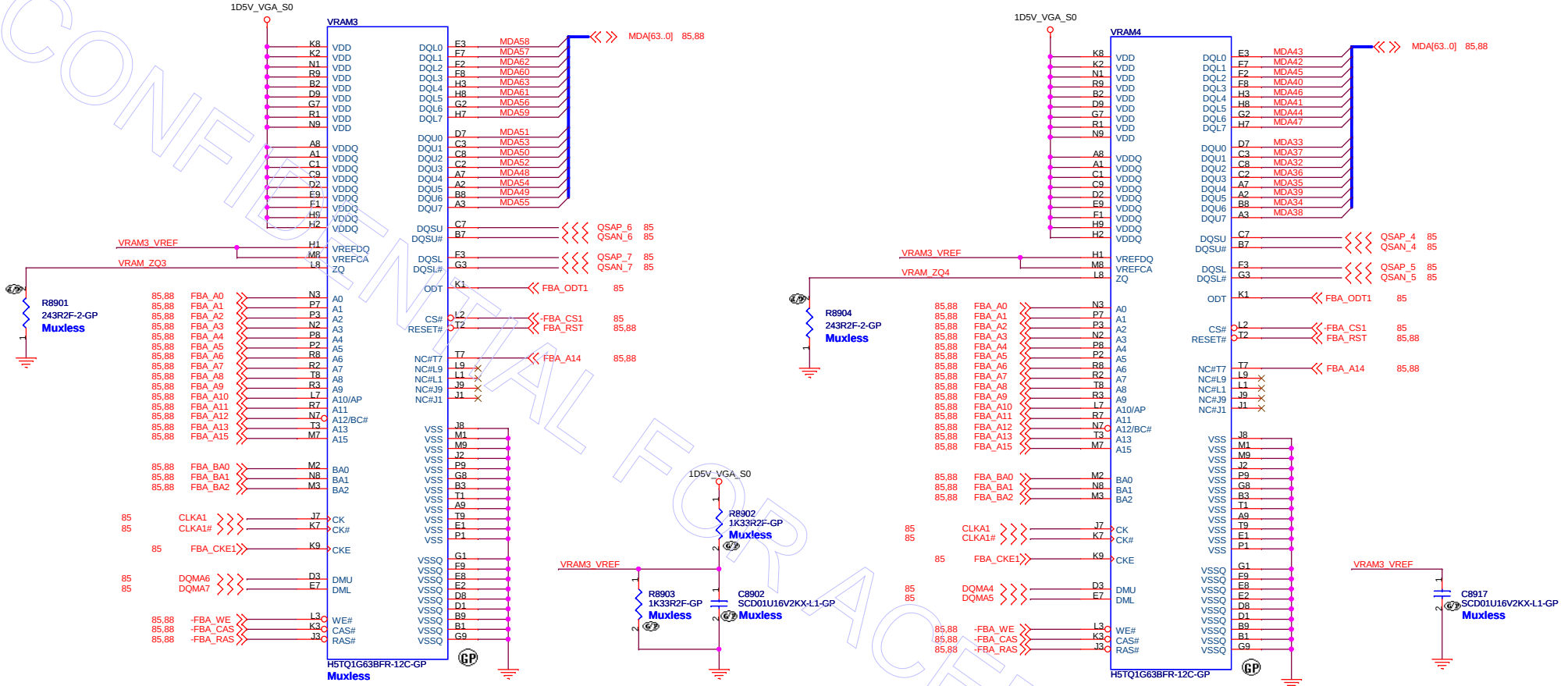
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

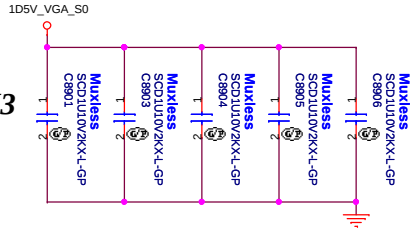
Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

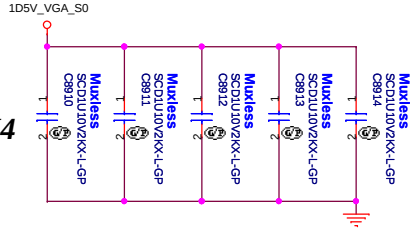
Date: Thursday, September 06, 2012 Sheet 88 of 103

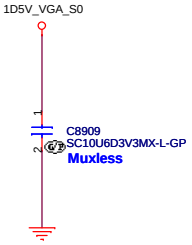


FOR VRAM3



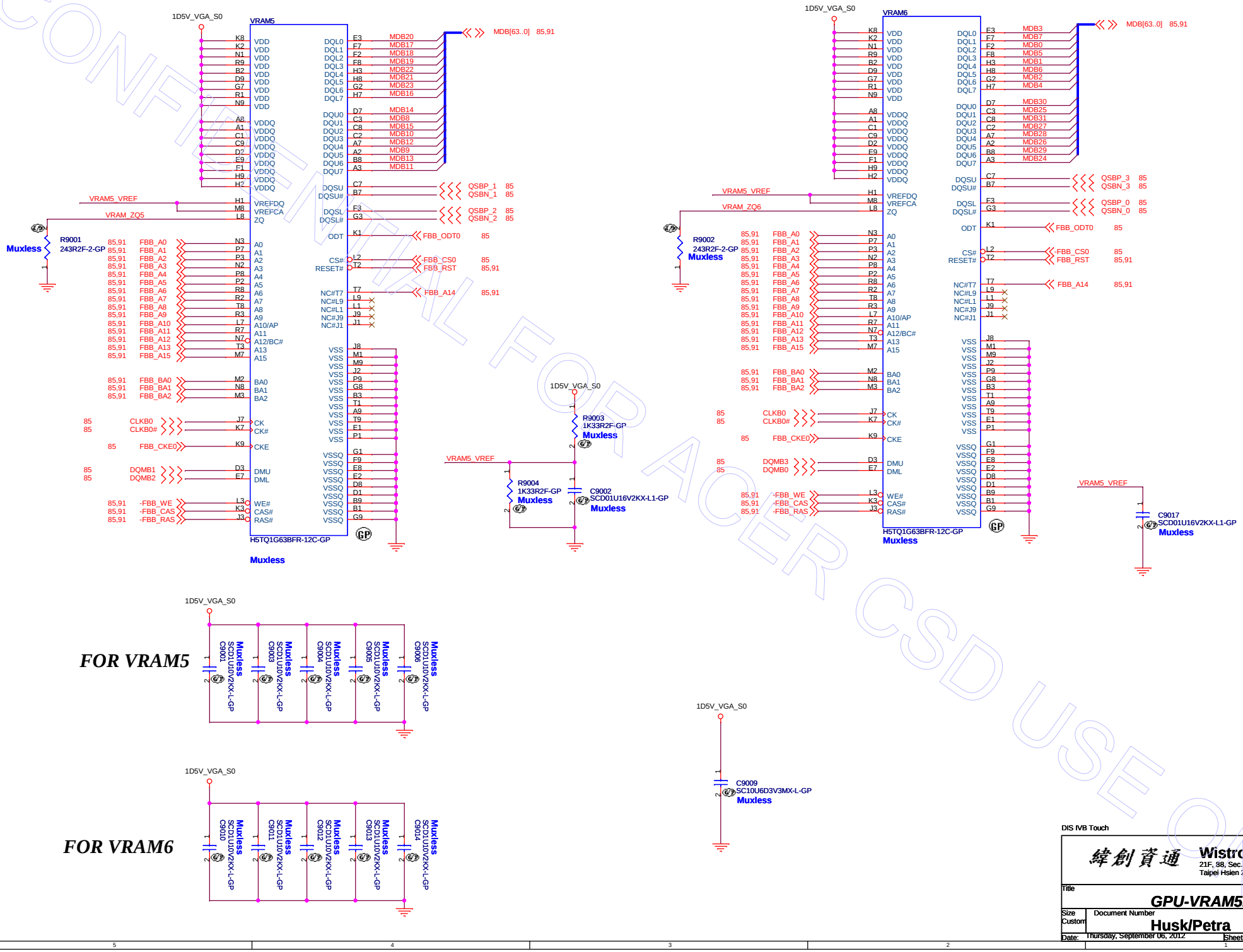
FOR VRAM4





DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM3,4 (2/4)		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 89 of 103	



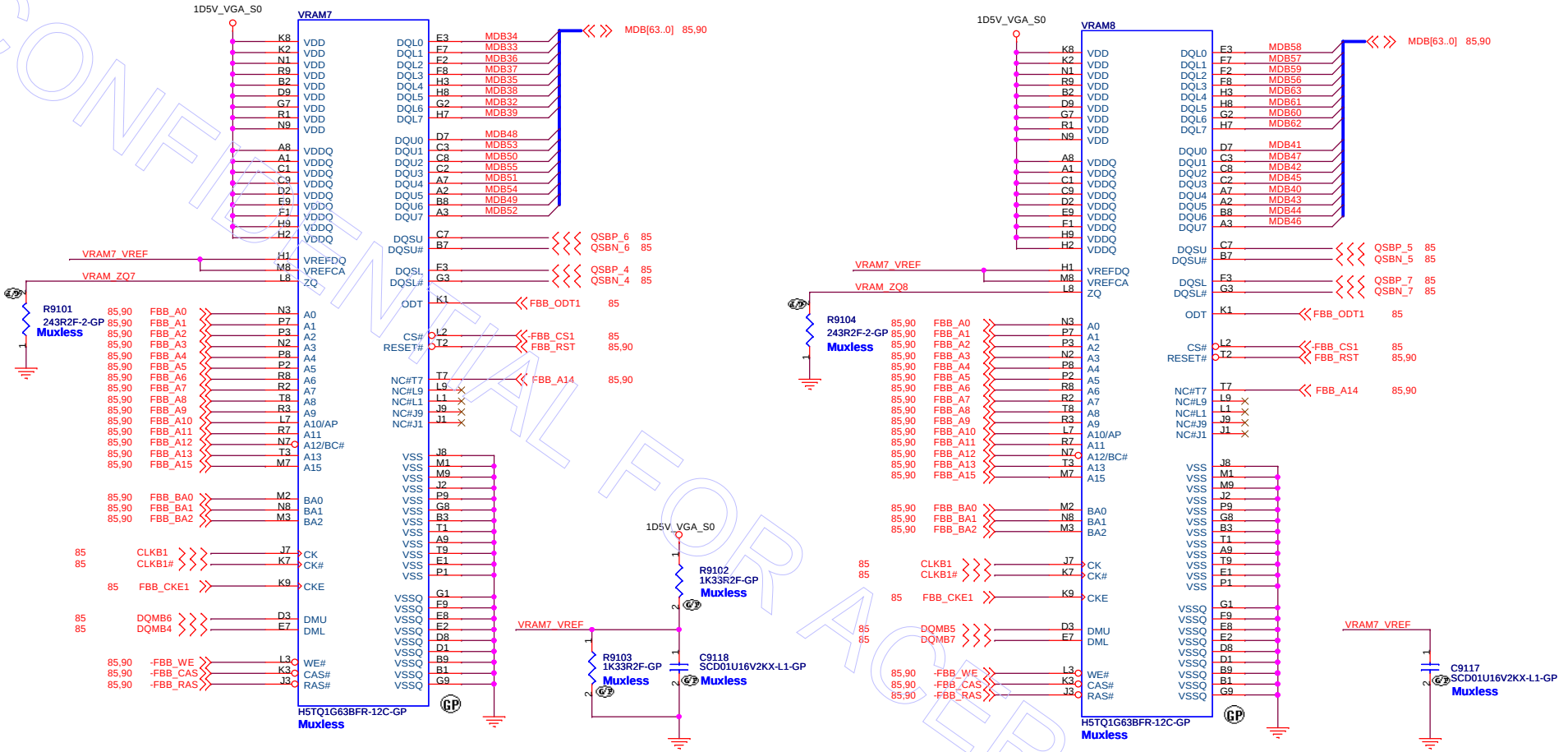
DIS IVB Touch

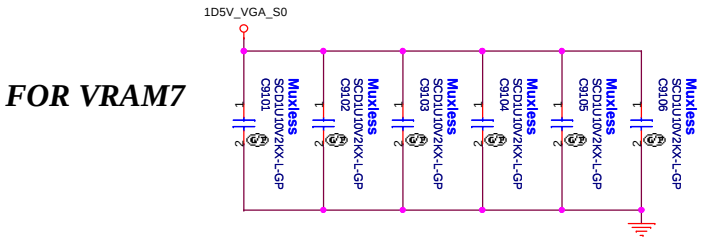
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

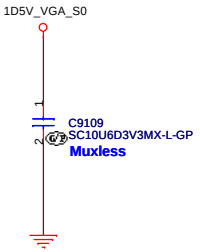
Title: GPU-VRAM5,6 (3/4)

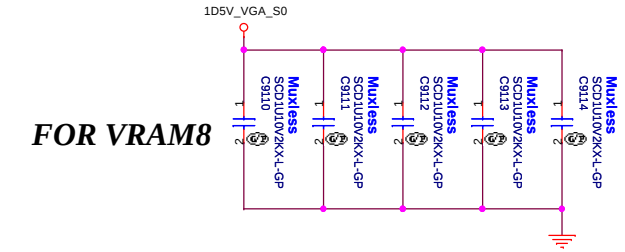
Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 90 of 103









DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM7,8 (4/4)		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 91 of 103	

SSID = PWR.Plane.Regulator_GFX

		N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	DY	63.10334.L0L
	PR9230	63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217	DY	63.10334.L0L	DY
	PR9232	63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218	63.10334.L0L	DY	63.10334.L0L
	PR9233	DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

1phase PR9261 mount
2phase PR9261 DY

1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY

Change power source Net
Wayler 12/07

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

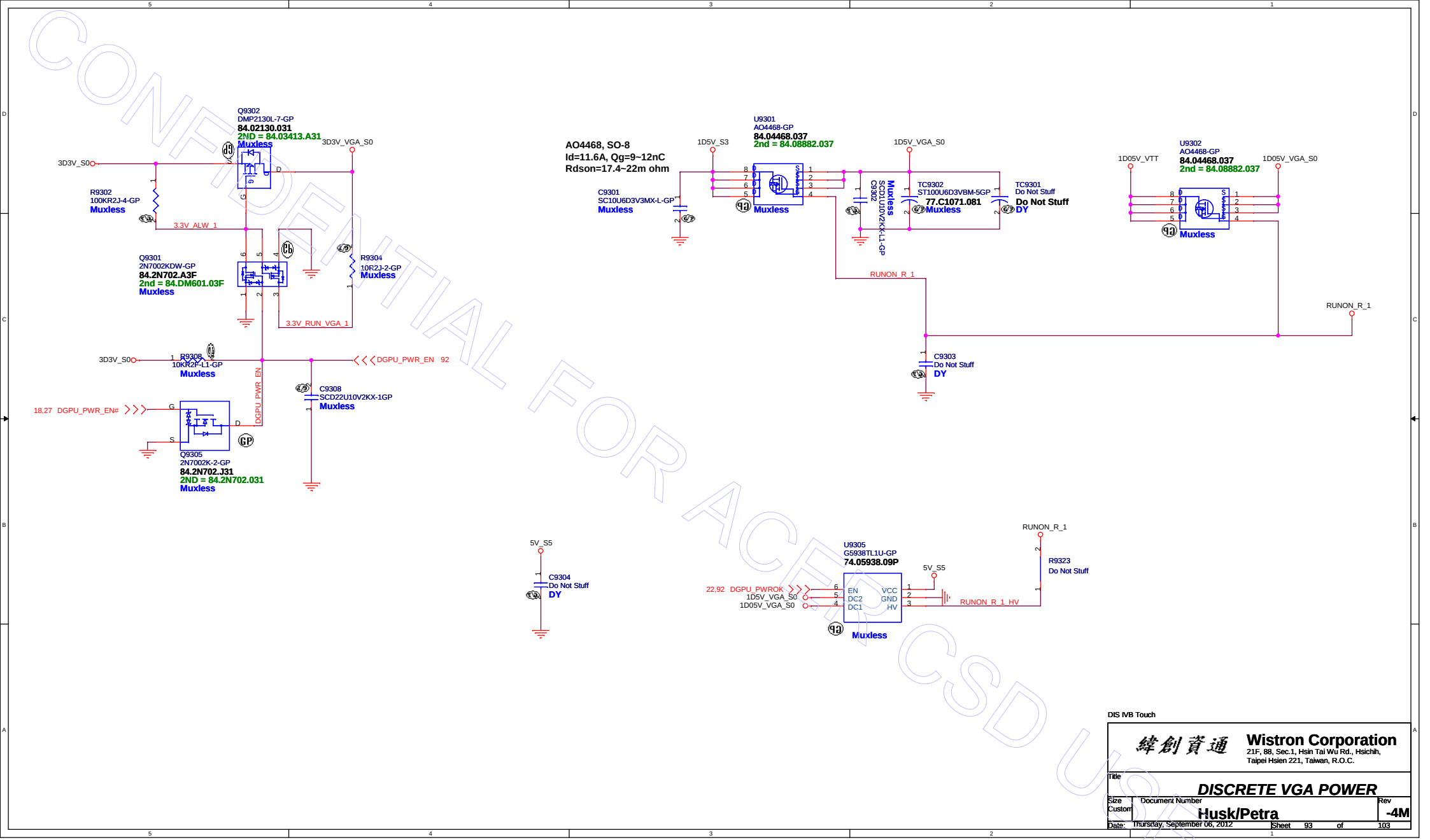
Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51728_VGA_CORE
Size: Document Number: Husk/Petra Rev: -4M
Date: Thursday, September 06, 2012 Sheet 92 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCRETE VGA POWER**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 93 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LVDS_Switch

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 94 of 103

DIS IVB Touch

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT_Switch

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 95 of 103

SSID = SDIO

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size	Document Number	Rev
A2	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 96 of 103

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff

CPU

HS3 STF237R128H41-GP
HS2 STF237R128H41-GP
HS1 STF237R128H41-GP

34.4TU18.001
2nd = 34.4TU18.101

34.4TU18.001
2nd = 34.4TU18.101

34.4TU18.001
2nd = 34.4TU18.101

HS4 STF237R128H41-GP
HS5 STF237R128H41-GP

34.4TU18.001
2nd = 34.4TU18.101
Muxless

34.4TU18.001
2nd = 34.4TU18.101
Muxless

VGA

Check test point

3D3V_S0	1	AFTP1
3D3V_AUX_S5	1	AFTP7
3D3V_S5	1	AFTP8
5V_S5	1	AFTP9
19,27 PM_PWRBTN#	1	AFTP10
5,22,36 H_CPUPWRGD	1	AFTP11
27,36 S5_ENABLE	1	AFTP12
5,18,27,31,36,65,71,83 PLT_RST#	1	AFTP13

Test Point放在Dimm Door打開可量測處

-4

PWR_VCCCORE1_DCBATOUT
PWR_GFXCORE1_DCBATOUT

EC9704 Do Not Stuff
EC9709 Do Not Stuff
EC9710 Do Not Stuff
EC9724 Do Not Stuff

1D05V_VTT
EC9705 Do Not Stuff
EC9706 Do Not Stuff

DCBATOUT
EC9701 SCD1U50V3KX-GP

DCBATOUT_2
EC9702 Do Not Stuff
EC9707 SCD1U50V3KX-GP
EC9723 Do Not Stuff
EC9722 SCD1U50V3KX-GP
EC9721 SCD1U50V3KX-GP

EC9728 Do Not Stuff
EC9729 Do Not Stuff
AUD_AGND

AD_JK	1	AFTP41
AD_JK	1	AFTP42

-4M_201208070840

39 BATA_SDA_1	1	AFTP2
39 BI	1	AFTP3
39 BAT_IN#_1	1	AFTP4
BT+	1	AFTP5
BT+	1	AFTP6
BT+	1	AFTP14
BT+	1	AFTP15
27,29,68,82 KBC_PWRBTN#	1	AFTP16
68,82 FRONT_PWRLED#_Q	1	AFTP17
DCBATOUT_LCD	1	AFTP18
DCBATOUT_LCD	1	AFTP19
49 DBC_EN_C	1	AFTP22
49 BLON_OUT_C	1	AFTP23
49 LCD_BRIGHTNESS	1	AFTP24
49 DP_TXP1_CPU_C	1	AFTP32
49 DP_TXN1_CPU_C	1	AFTP33
49 DP_TXP0_CPU_C	1	AFTP34
49 DP_TXN0_CPU_C	1	AFTP35
49 DP_DDC_CLK_CPU_C	1	AFTP37
LCDVDD	1	AFTP38
LCDVDD	1	AFTP39
50,59 CRT_DDCCLK_CON	1	AFTP44
50,59 CRT_VSYNC_CON	1	AFTP45
50,59 CRT_DDCDATA_CON	1	AFTP46
50,59 CRT_HSYNC_CON	1	AFTP47

-4M-201208031615

1D5V_S3
EC9711 Do Not Stuff
EC9712 Do Not Stuff
EC9713 Do Not Stuff
EC9714 Do Not Stuff
EC9715 Do Not Stuff
EC9716 Do Not Stuff

5V_S0
EC9717 Do Not Stuff
EC9718 Do Not Stuff
EC9719 SCD1U10V2KX-L1-GP
EC9720 Do Not Stuff

-2:EMI

DCBATOUT
EC9703 SCD1U50V3KX-GP

LCDVDD
EC9726 SCD1U10V2KX-L1-GP

DCBATOUT
EC9730 SCD1U50V3KX-GP
EC9731 SCD1U50V3KX-GP

5V_S5
EC9725 Do Not Stuff

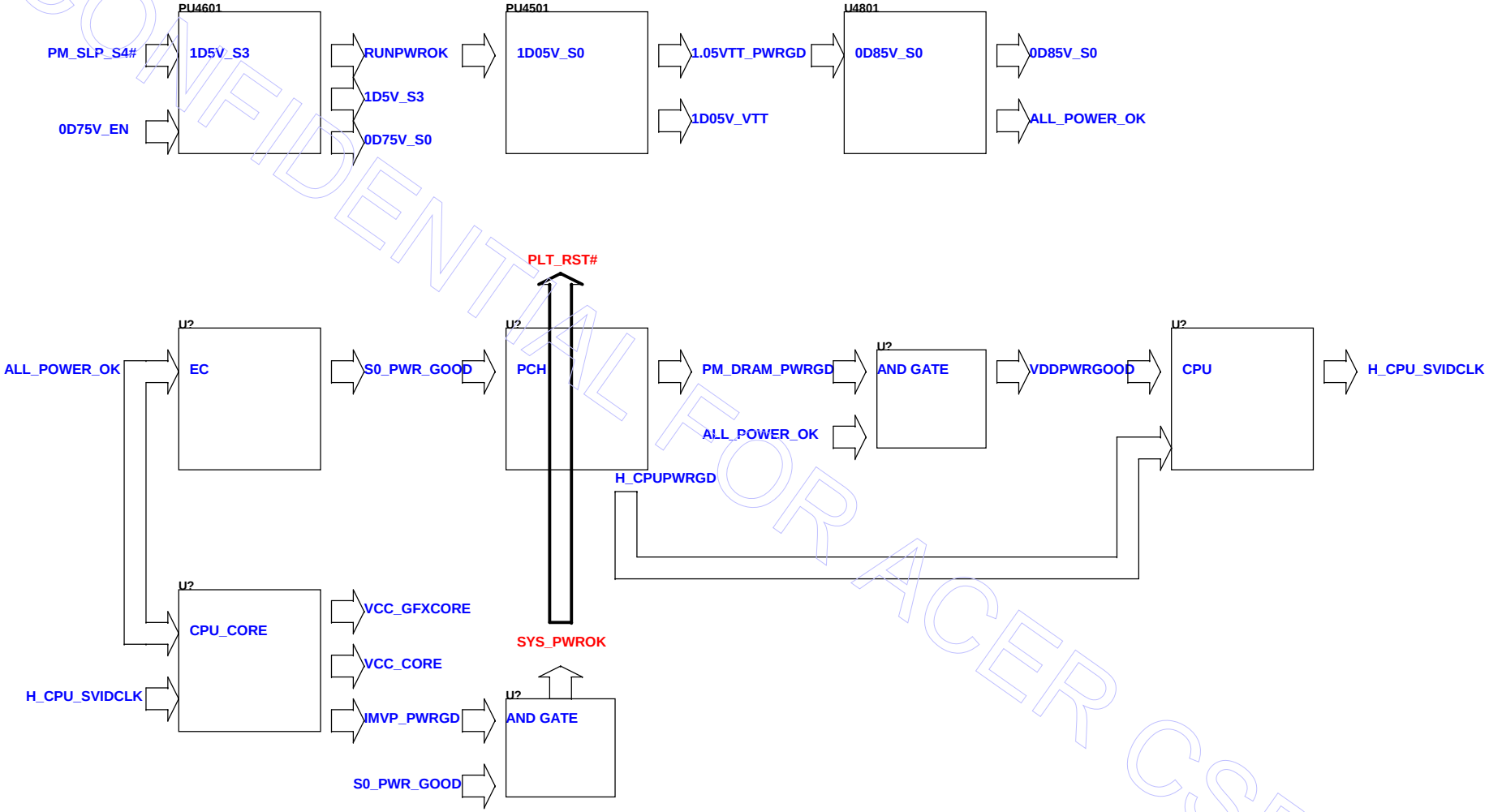
3D3V_S0
EC9708 Do Not Stuff

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Husk/Petra
Rev: -4M
Date: Thursday, September 06, 2012
Sheet 97 of 103

Power Sequence



DIS IVB Touch

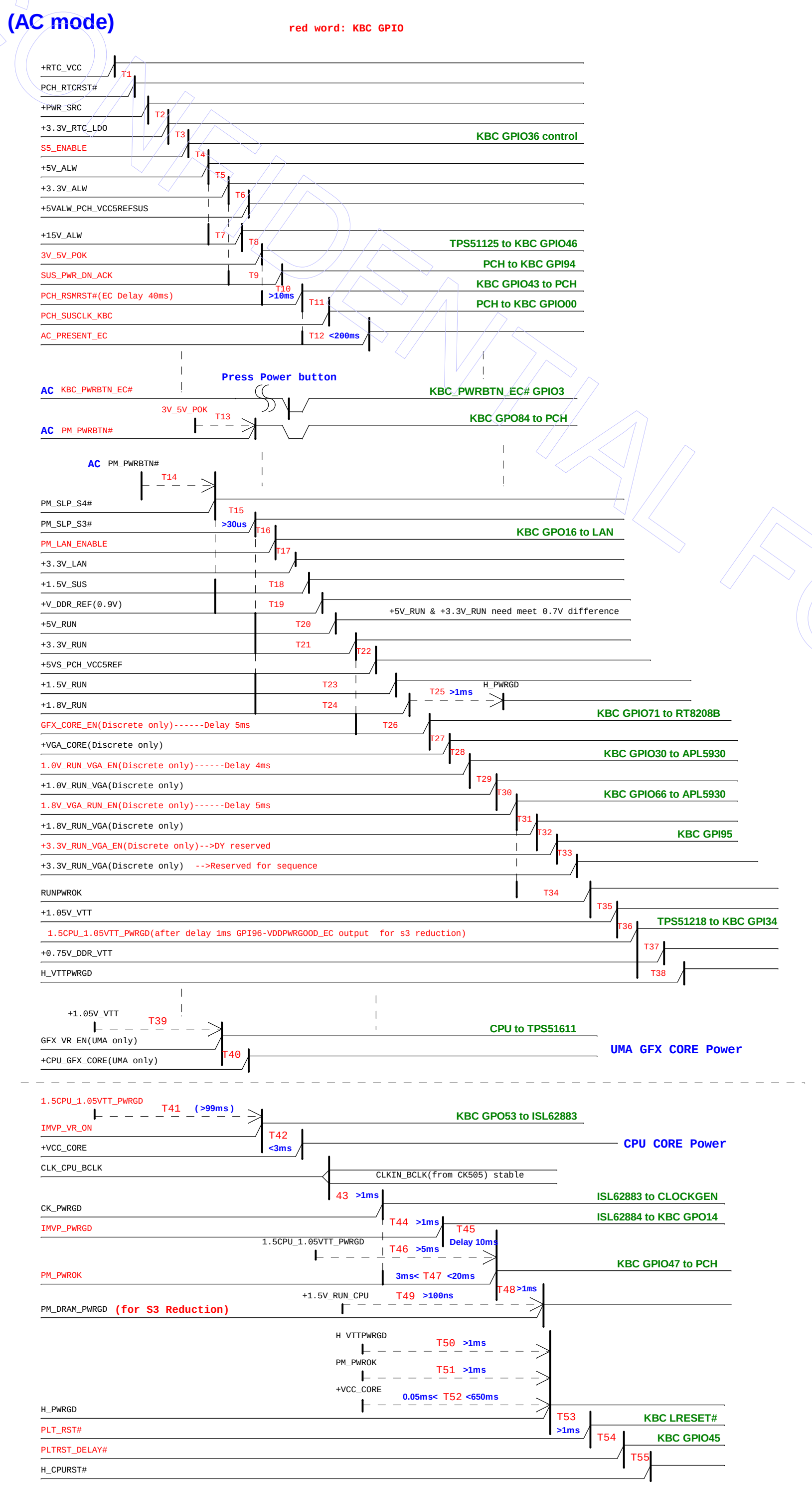
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

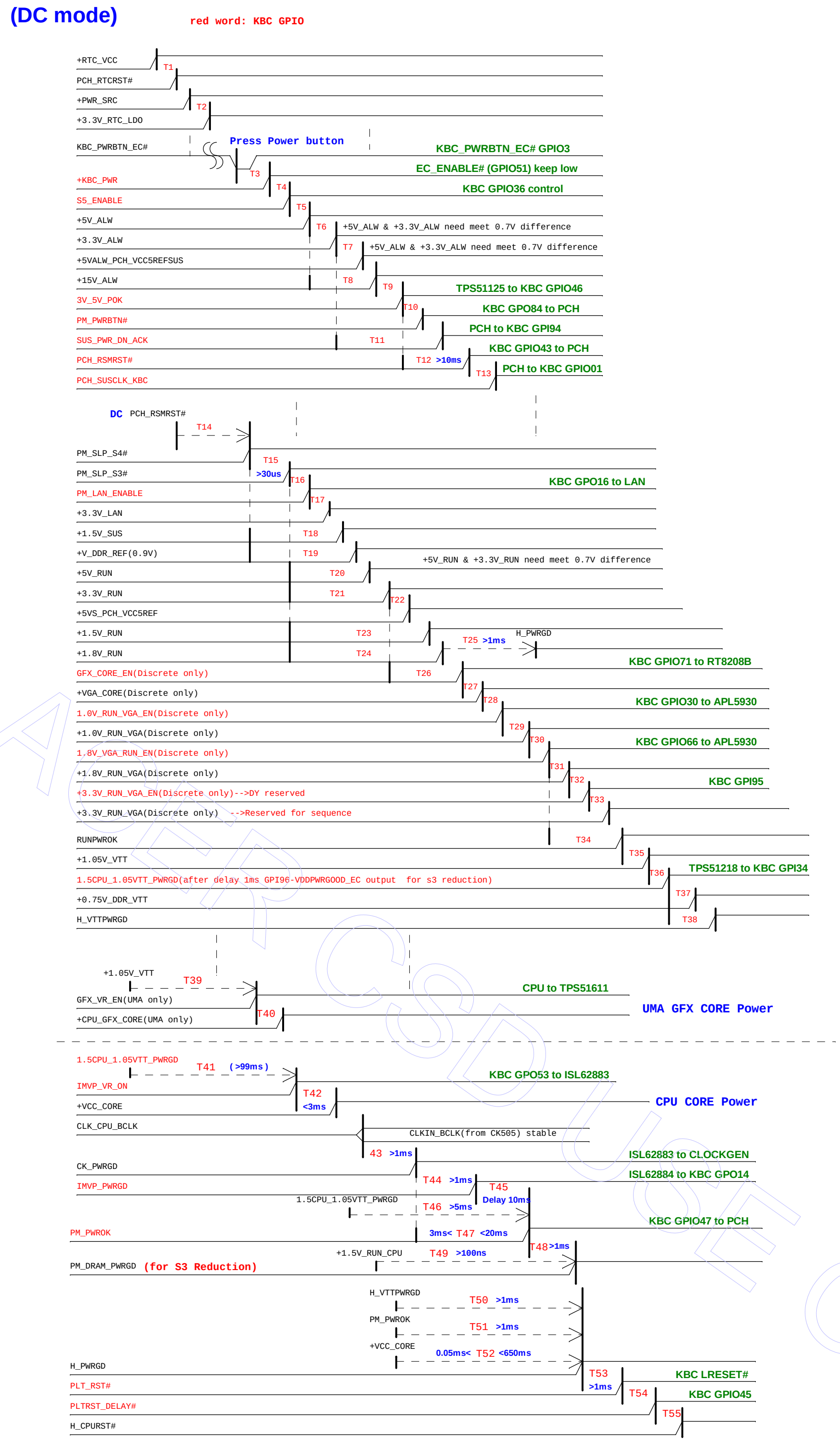
Title: Change History

Size	Document Number	Rev
A3	Husk/Petra	-4M

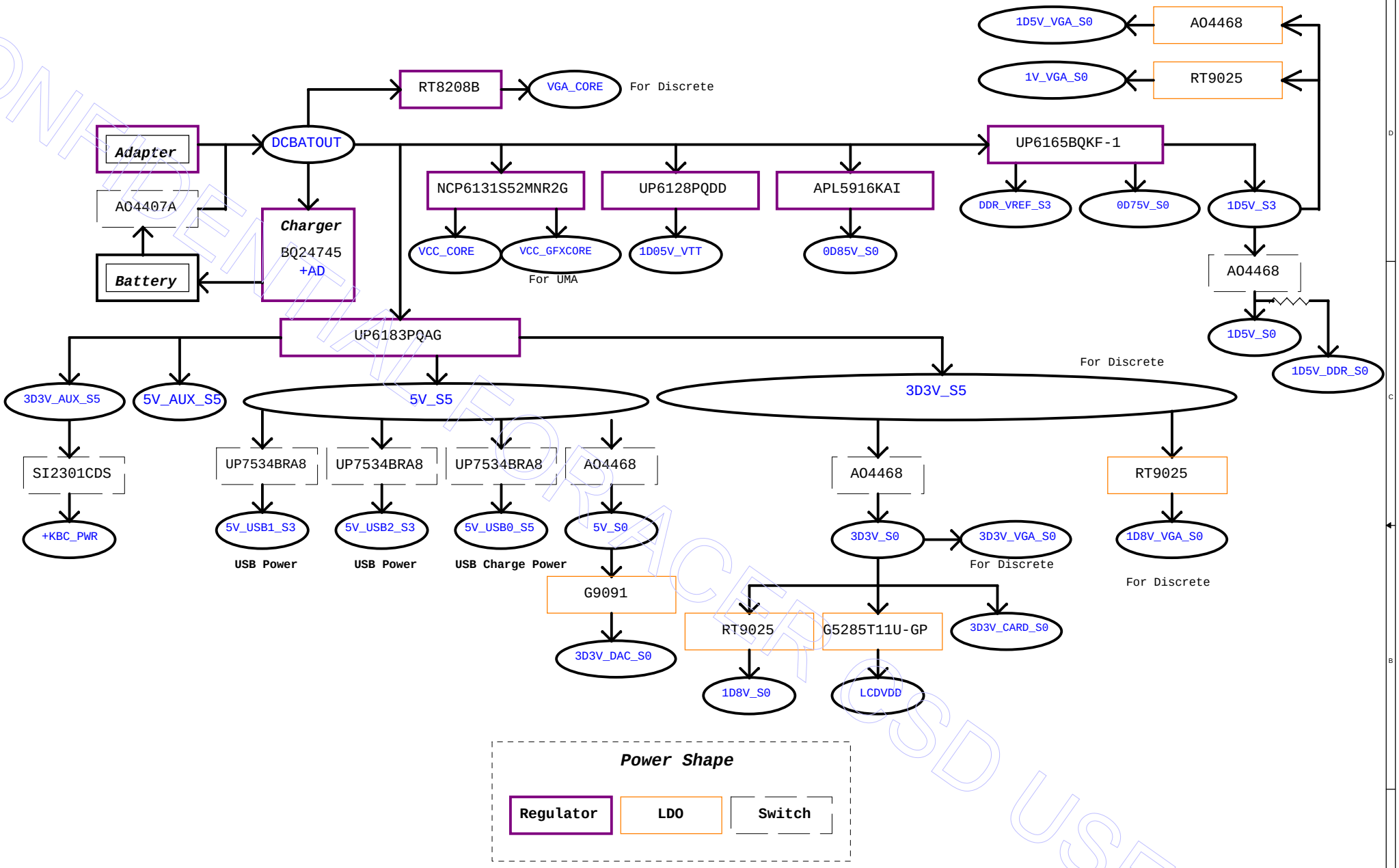
Date: Thursday, September 06, 2012 Sheet 98 of 103

Intel-Power Up Sequence


(AC mode)
red word: KBC GPIO
+RTC_VCC
PCH_RTCRST#
+PWR_SRC
+3.3V_RTC_LDO
S5_ENABLE
+5V_ALW
+3.3V_ALW
+5VALW_PCH_VCC5REFSUS
+15V_ALW
3V_5V_POK
SUS_PWR_DN_ACK
PCH_RSMRST#(EC Delay 40ms)
PCH_SUSCLK_KBC
AC_PRESENT_EC
KBC GPIO36 control
TPS51125 to KBC GPIO46
PCH to KBC GPI94
KBC GPIO43 to PCH
PCH to KBC GPIO00
T10 >10ms
T12 <200ms
Press Power button
AC KBC_PWRBTN_EC#
KBC_PWRBTN_EC# GPIO3
AC PM_PWRBTN#
KBC GPO84 to PCH
AC PM_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
PM_LAN_ENABLE
+3.3V_LAN
+1.5V_SUS
+V_DDR_REF(0.9V)
+5V_RUN
+3.3V_RUN
+5VS_PCH_VCC5REF
+1.5V_RUN
+1.8V_RUN
GFX_CORE_EN(Discrete only)------Delay 5ms
+VGA_CORE(Discrete only)
1.0V_RUN_VGA_EN(Discrete only)------Delay 4ms
+1.0V_RUN_VGA(Discrete only)
1.8V_VGA_RUN_EN(Discrete only)------Delay 5ms
+1.8V_RUN_VGA(Discrete only)
+3.3V_RUN_VGA_EN(Discrete only)-->DY reserved
+3.3V_RUN_VGA(Discrete only) -->Reserved for sequence
RUNPWROK
+1.05V_VTT
1.5CPU_1.05VTT_PWRGD(after delay 1ms GPI96-VDDPWRGOOD_EC output for s3 reduction)
+0.75V_DDR_VTT
H_VTTPWRGD
T15 >30us
KBC GPO16 to LAN
+5V_RUN & +3.3V_RUN need meet 0.7V difference
T25 >1ms
H_PWRGD
KBC GPIO71 to RT8208B
KBC GPIO30 to APL5930
KBC GPIO66 to APL5930
KBC GPI95
TPS51218 to KBC GPI34
+1.05V_VTT
GFX_VR_EN(UMA only)
+CPU_GFX_CORE(UMA only)
CPU to TPS51611
UMA GFX CORE Power
1.5CPU_1.05VTT_PWRGD
IMVP_VR_ON
+VCC_CORE
CLK_CPU_BCLK
CK_PWRGD
IMVP_PWRGD
PM_PWROK
PM_DRAM_PWRGD (for S3 Reduction)
T41 (>99ms)
KBC GPO53 to ISL62883
T42 <3ms
CPU CORE Power
CLKIN_BCLK(from CK505) stable
43 >1ms
ISL62883 to CLOCKGEN
T44 >1ms
T45 Delay 10ms
ISL62884 to KBC GPO14
1.5CPU_1.05VTT_PWRGD
T46 >5ms
3ms< T47 <20ms
KBC GPIO47 to PCH
+1.5V_RUN_CPU
T49 >100ms
T48 >1ms
H_VTTPWRGD
T50 >1ms
PM_PWROK
T51 >1ms
+VCC_CORE
0.05ms< T52 <650ms
H_PWRGD
PLT_RST#
PLTRST_DELAY#
H_CPURST#
T53 >1ms
KBC LRESET#
T54
KBC GPIO45
T55


(DC mode)
red word: KBC GPIO
+RTC_VCC
PCH_RTCRST#
+PWR_SRC
+3.3V_RTC_LDO
KBC_PWRBTN_EC#
Press Power button
KBC_PWRBTN_EC# GPIO3
+KBC_PWR
EC_ENABLE# (GPIO51) keep low
S5_ENABLE
KBC GPIO36 control
+5V_ALW
+3.3V_ALW
+5VALW_PCH_VCC5REFSUS
+15V_ALW
3V_5V_POK
PM_PWRBTN#
SUS_PWR_DN_ACK
PCH_RSMRST#
PCH_SUSCLK_KBC
+5V_ALW & +3.3V_ALW need meet 0.7V difference
TPS51125 to KBC GPIO46
KBC GPO84 to PCH
PCH to KBC GPI94
KBC GPIO43 to PCH
PCH to KBC GPIO01
T12 >10ms
DC PCH_RSMRST#
PM_SLP_S4#
PM_SLP_S3#
PM_LAN_ENABLE
+3.3V_LAN
+1.5V_SUS
+V_DDR_REF(0.9V)
+5V_RUN
+3.3V_RUN
+5VS_PCH_VCC5REF
+1.5V_RUN
+1.8V_RUN
GFX_CORE_EN(Discrete only)
+VGA_CORE(Discrete only)
1.0V_RUN_VGA_EN(Discrete only)
+1.0V_RUN_VGA(Discrete only)
1.8V_VGA_RUN_EN(Discrete only)
+1.8V_RUN_VGA(Discrete only)
+3.3V_RUN_VGA_EN(Discrete only)-->DY reserved
+3.3V_RUN_VGA(Discrete only) -->Reserved for sequence
RUNPWROK
+1.05V_VTT
1.5CPU_1.05VTT_PWRGD(after delay 1ms GPI96-VDDPWRGOOD_EC output for s3 reduction)
+0.75V_DDR_VTT
H_VTTPWRGD
T15 >30us
KBC GPO16 to LAN
+5V_RUN & +3.3V_RUN need meet 0.7V difference
T25 >1ms
H_PWRGD
KBC GPIO71 to RT8208B
KBC GPIO30 to APL5930
KBC GPIO66 to APL5930
KBC GPI95
TPS51218 to KBC GPI34
+1.05V_VTT
GFX_VR_EN(UMA only)
+CPU_GFX_CORE(UMA only)
CPU to TPS51611
UMA GFX CORE Power
1.5CPU_1.05VTT_PWRGD
IMVP_VR_ON
+VCC_CORE
CLK_CPU_BCLK
CK_PWRGD
IMVP_PWRGD
PM_PWROK
PM_DRAM_PWRGD (for S3 Reduction)
T41 (>99ms)
KBC GPO53 to ISL62883
T42 <3ms
CPU CORE Power
CLKIN_BCLK(from CK505) stable
43 >1ms
ISL62883 to CLOCKGEN
T44 >1ms
T45 Delay 10ms
ISL62884 to KBC GPIO14
T46 >5ms
3ms< T47 <20ms
KBC GPIO47 to PCH
+1.5V_RUN_CPU
T49 >100ms
T48 >1ms
H_VTTPWRGD
T50 >1ms
PM_PWROK
T51 >1ms
+VCC_CORE
0.05ms< T52 <650ms
H_PWRGD
PLT_RST#
PLTRST_DELAY#
H_CPURST#
T53 >1ms
KBC LRESET#
T54
KBC GPIO45
T55

緯創資通	Wistron Corporation
Title	Power Sequence
Document Number	Husk/Petra
Rev	-4M



DIS IVB Touch

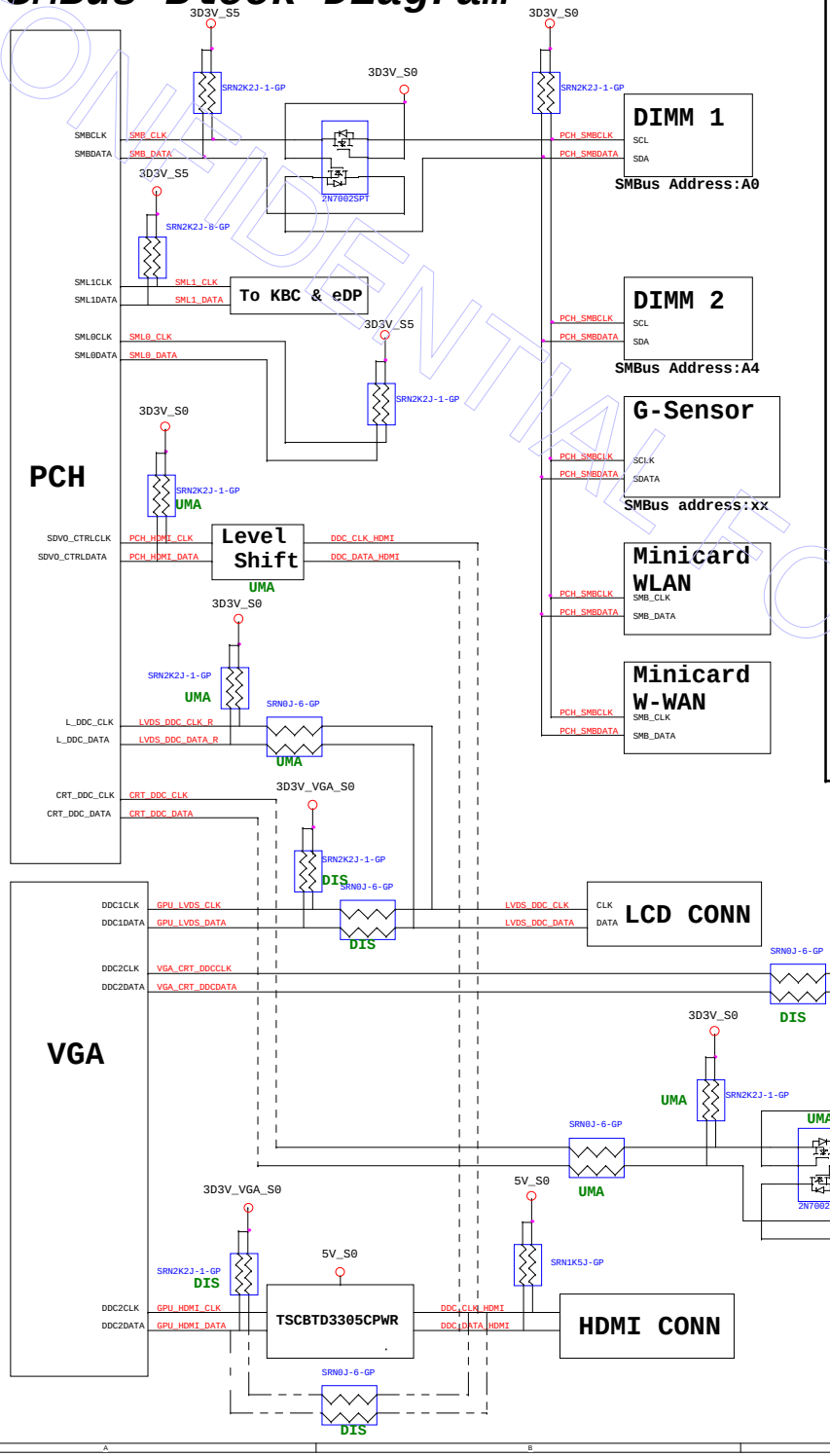
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

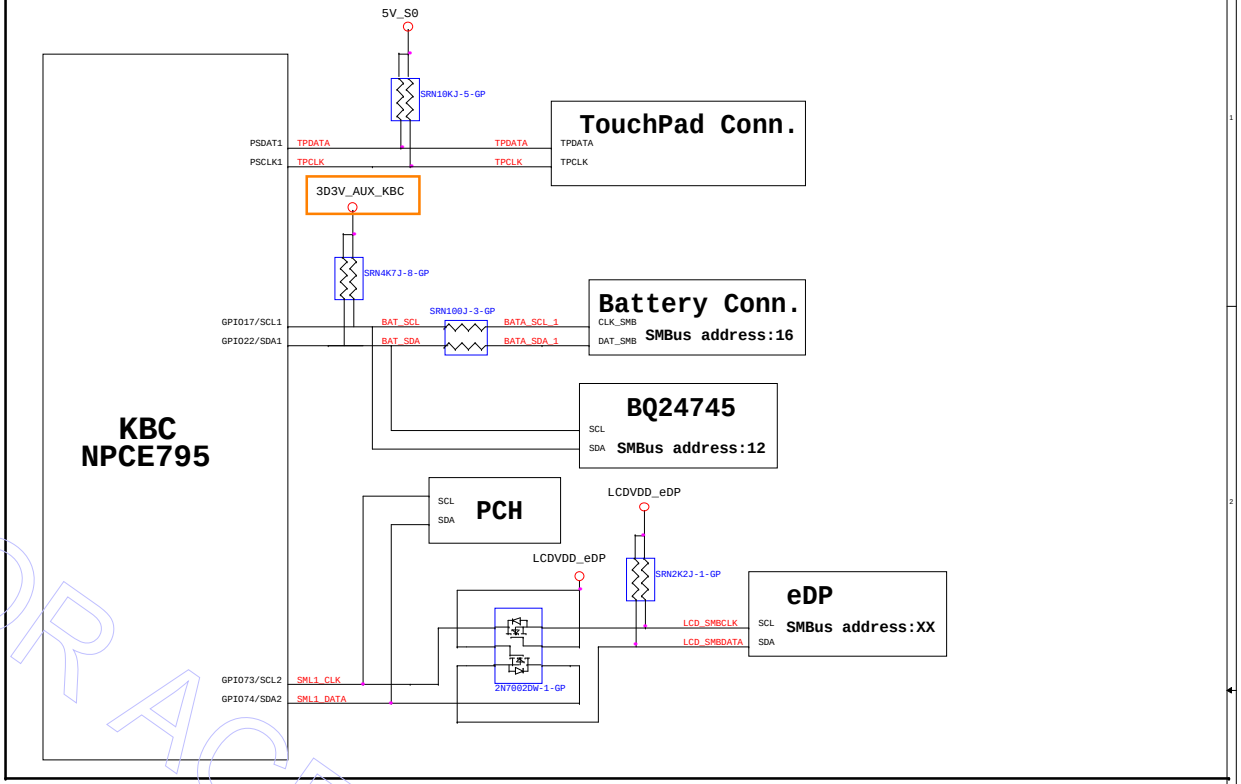
Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 100 of 103

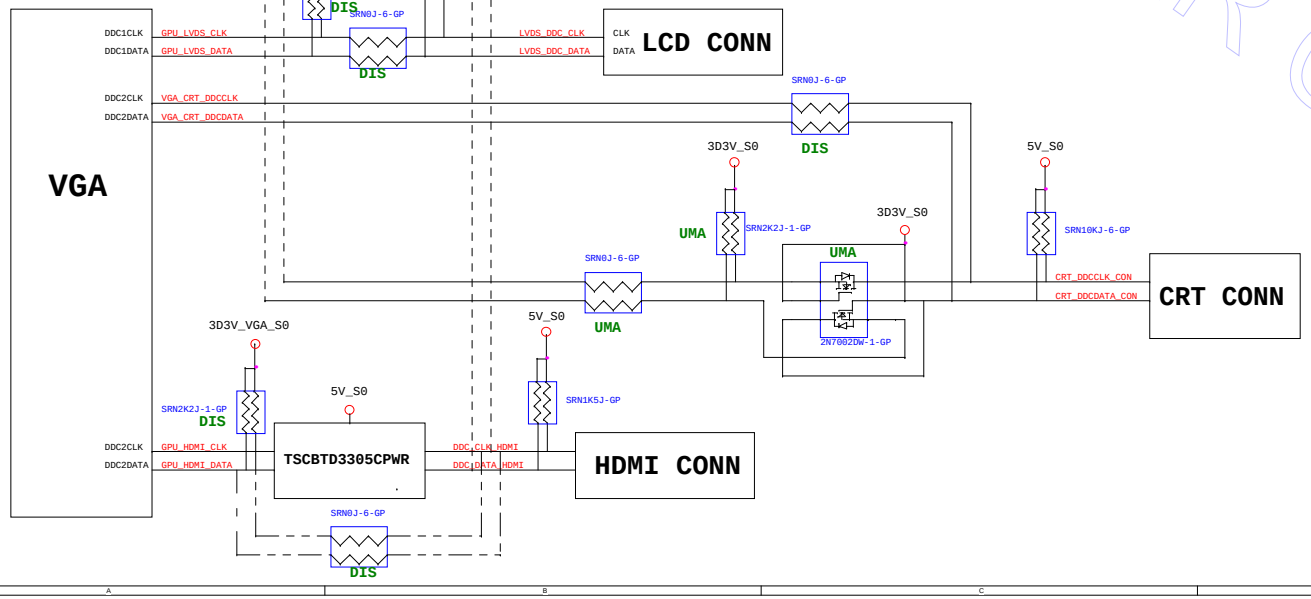
PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA



DIS IVB Touch

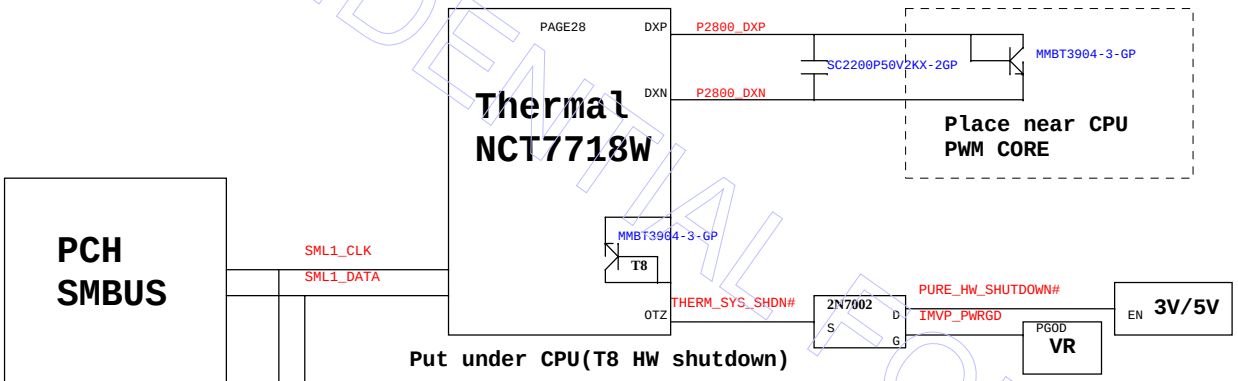
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

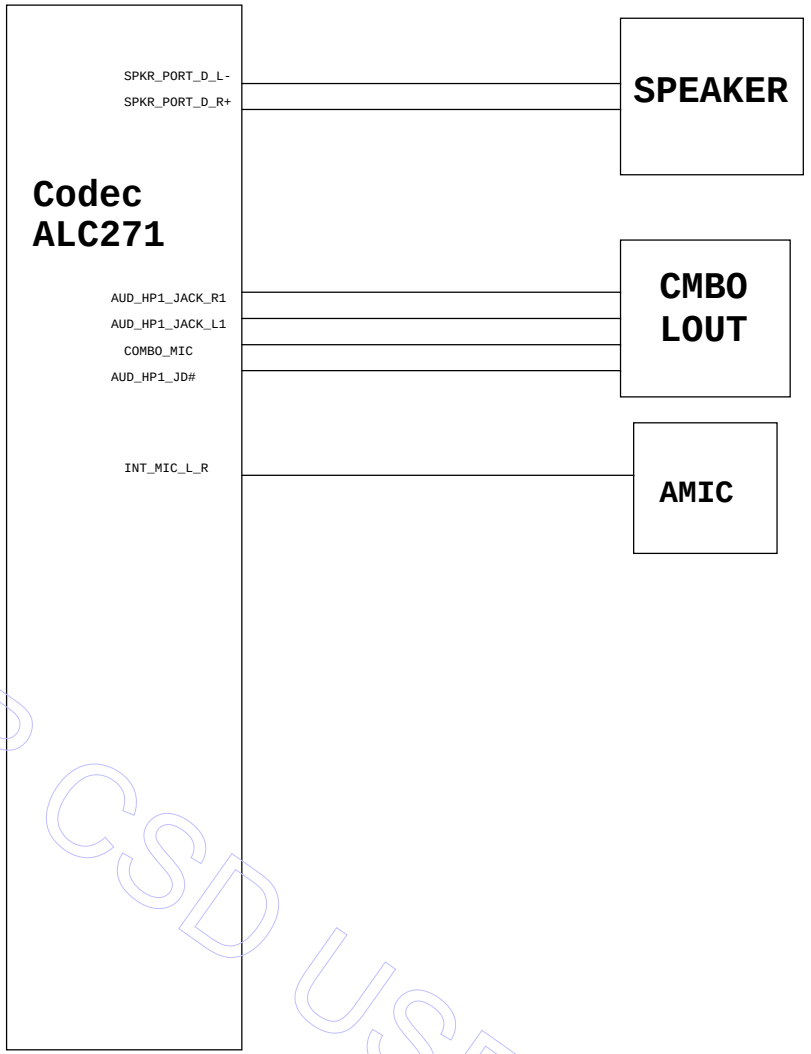
Size	Document Number	Rev
A2	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 102 of 103

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB charger**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 103 of 103