

Husk/Petra UMA/Muxless Schematics Document Ivy Bridge Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

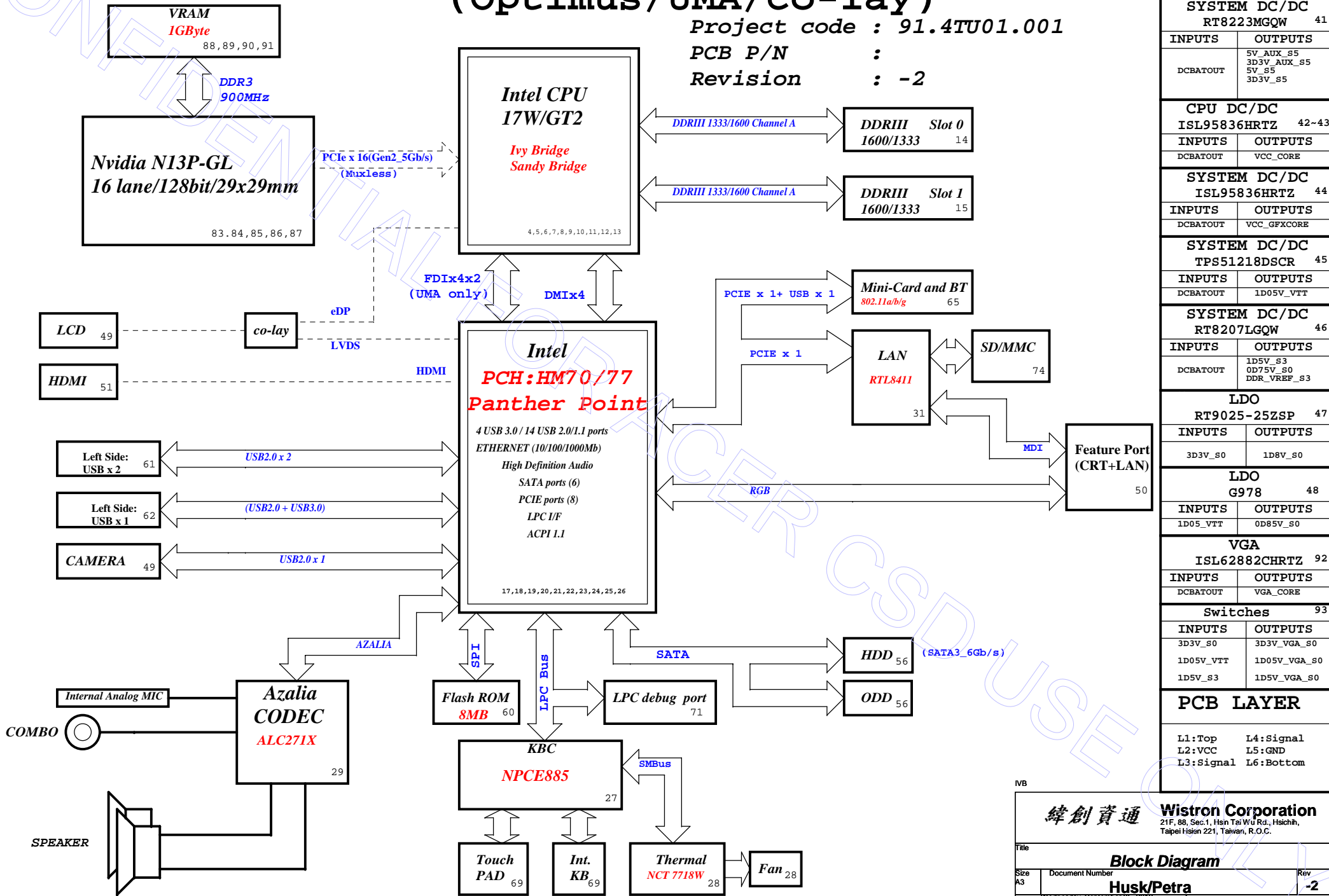
ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

IVB

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -2



CHARGER	
BQ24727	40
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT8223MGQW	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
CPU DC/DC	
ISL95836HRTZ	42~43
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
ISL95836HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218DSCR	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207LGQW	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
LDO	
RT9025-25ZSP	47
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
LDO	
G978	48
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0
VGA	
ISL62882CHRTZ	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches	
93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCC0 with 8.2-kohm weak pull-up resistor (CRB has it pulled up with 1-kohm no-stuff resistor) Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following XXRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB Bus	
Device	Address	Hex	Bus	
EC SMBus 1 Battery CHARGER	BAT_SCL/BAT_SDA		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP	SML1_CLK/SML1_DATA		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMM(A) (SPD) SO-DIMM(B) (SPD) Digital Pot G-Sensor MINI	PCH_SMBDATA/PCH_SMBCLK		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

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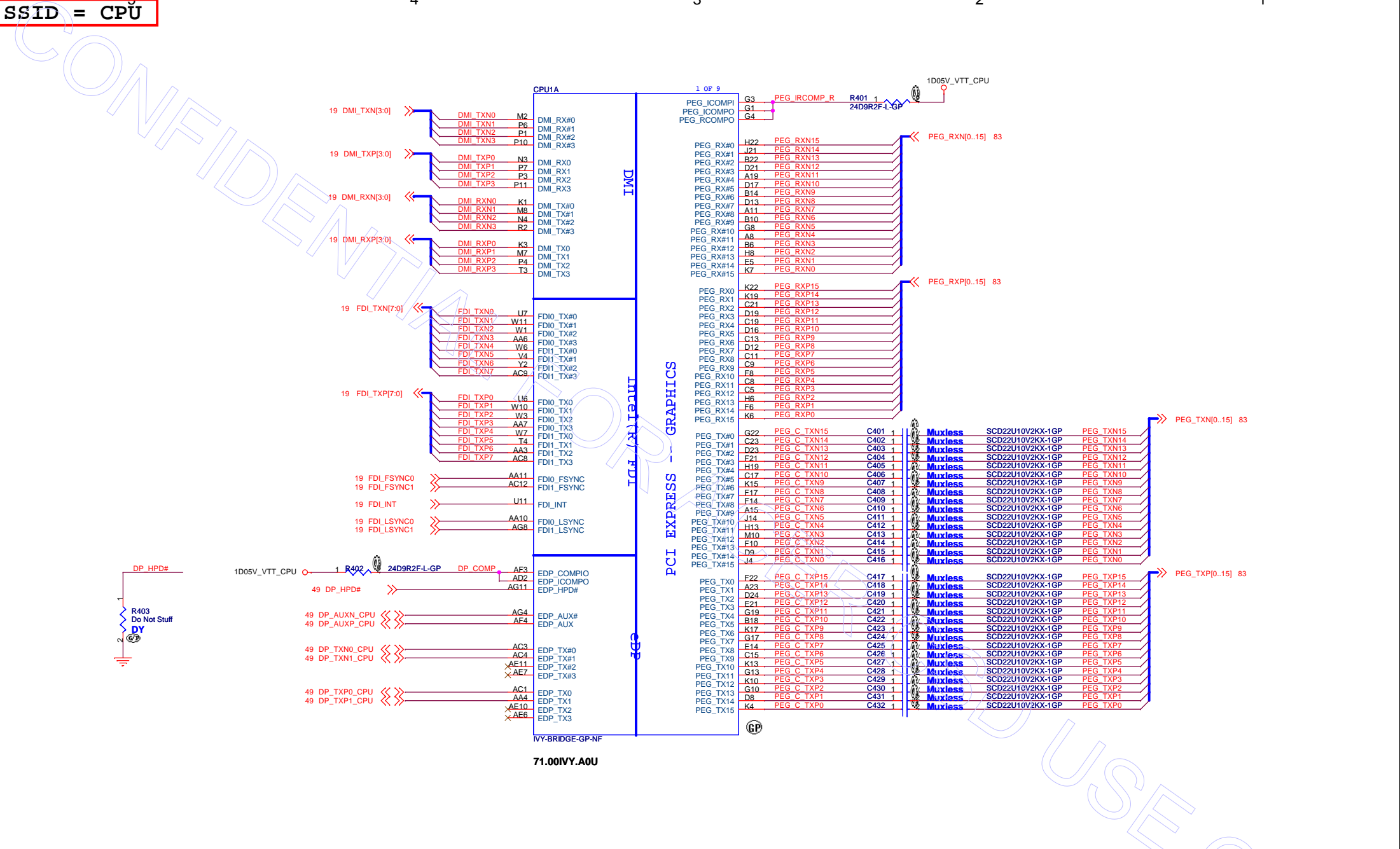
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Size A3 Document Number **Rev -2**

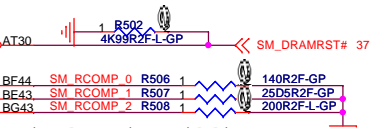
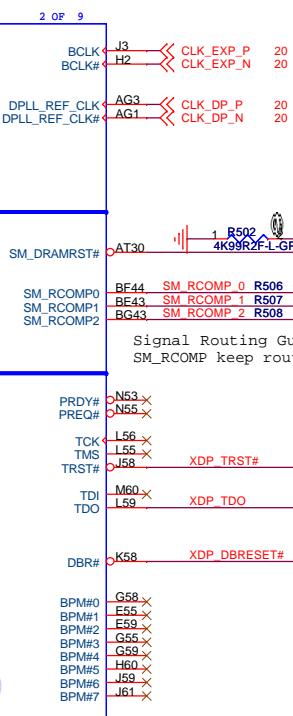
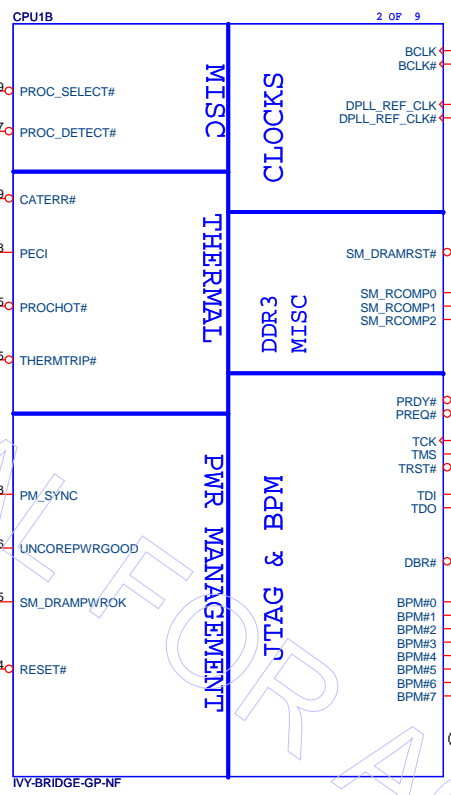
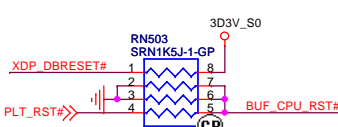
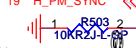
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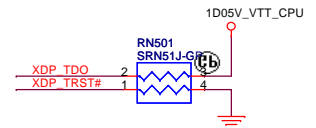


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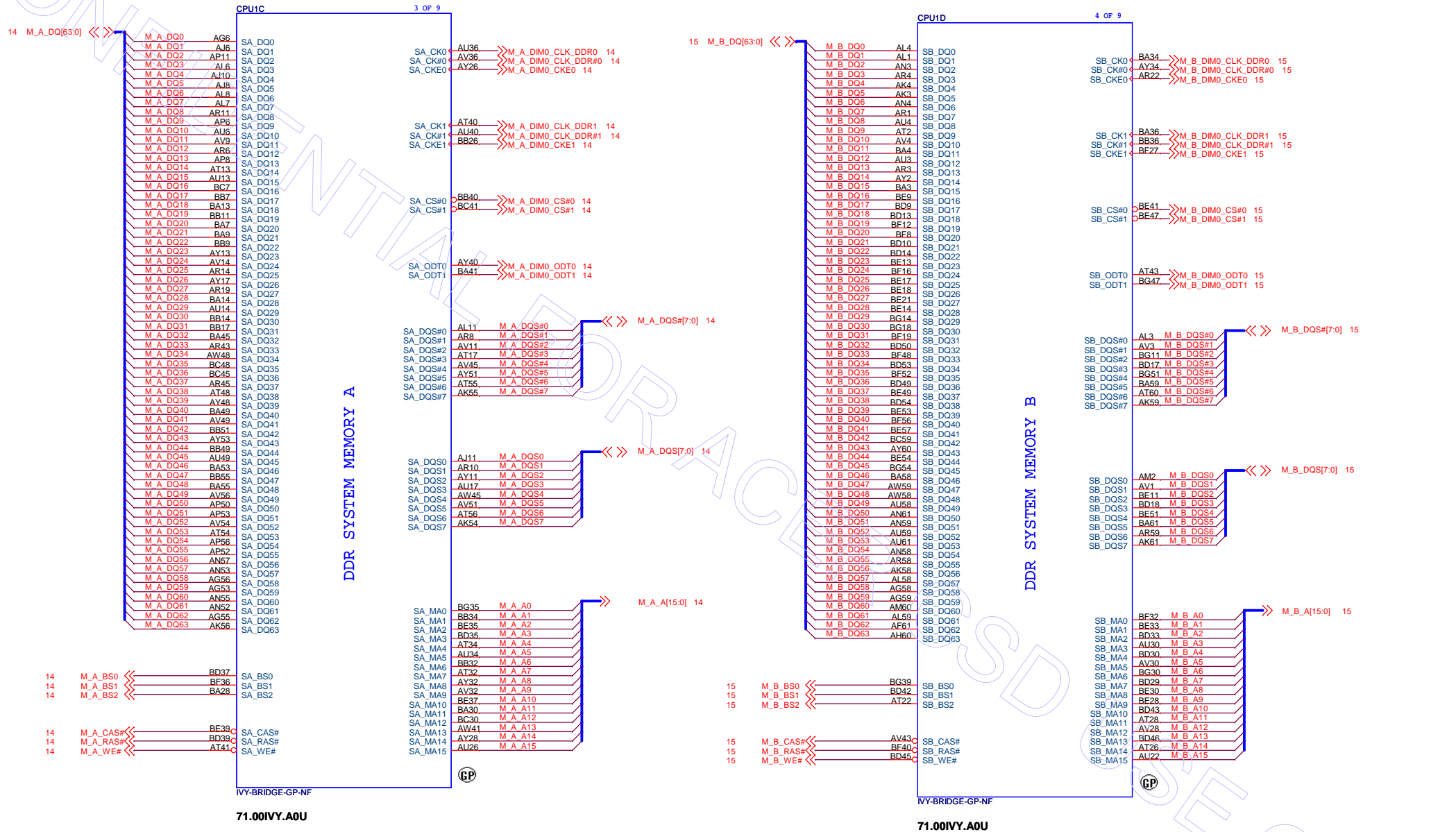


Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



IVB	
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Title CPU (THERMAL/CLOCK/PM)	
Size Custom	Document Number Husk/Petra
Date: Thursday, April 19, 2012	Rev -2
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IVY-BRIDGE-GP-NF

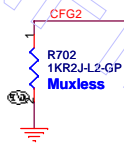
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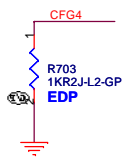
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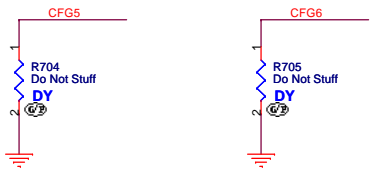
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



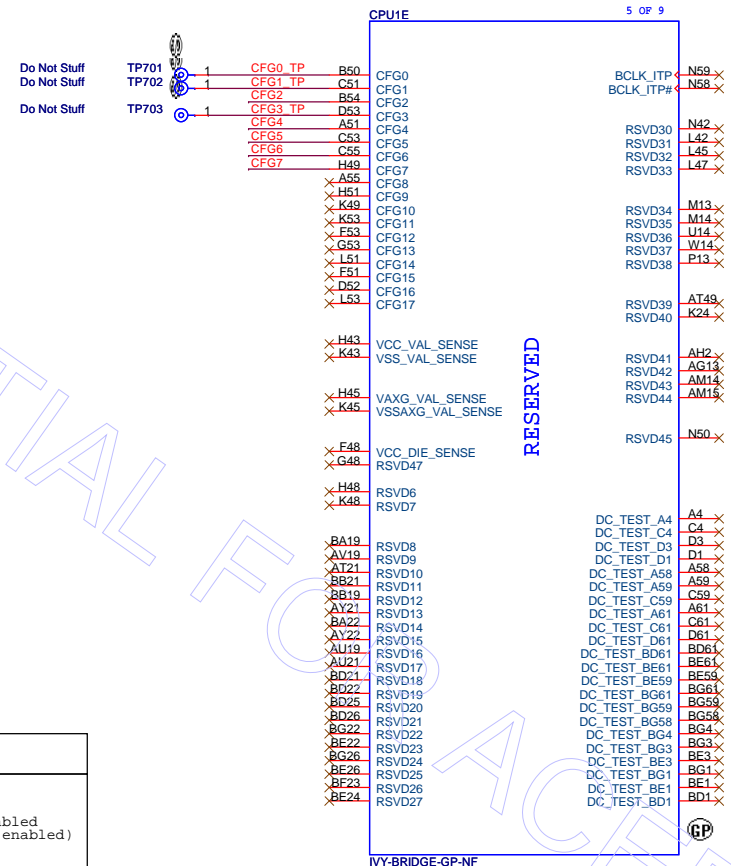
Enabl EDP function	
CFG4	1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



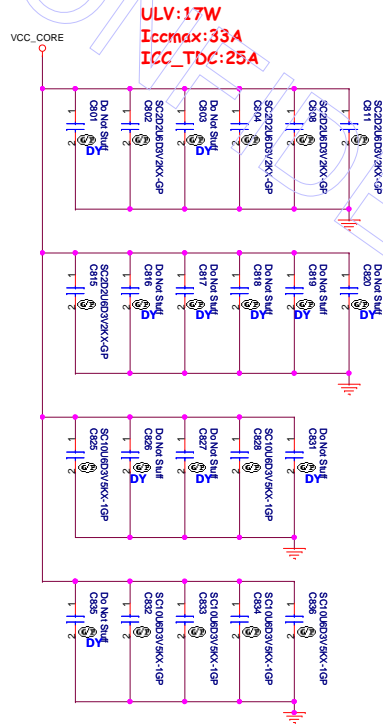
PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



71.00IVY.A0U

SSID = CPU

CPU1F 6 OF 9



- VCC_CORE
- A26 VCC1
 - A29 VCC2
 - A31 VCC3
 - A33 VCC4
 - A36 VCC5
 - A38 VCC6
 - A42 VCC7
 - A44 VCC8
 - C26 VCC9
 - C27 VCC10
 - C30 VCC11
 - C34 VCC12
 - C37 VCC13
 - C39 VCC14
 - C42 VCC15
 - D27 VCC16
 - D32 VCC17
 - D34 VCC18
 - D37 VCC19
 - D39 VCC20
 - D42 VCC21
 - E26 VCC22
 - E32 VCC23
 - E34 VCC24
 - F34 VCC25
 - F37 VCC26
 - F39 VCC27
 - F26 VCC28
 - F28 VCC29
 - F32 VCC30
 - F34 VCC31
 - F37 VCC32
 - F38 VCC33
 - G42 VCC34
 - G45 VCC35
 - H26 VCC36
 - H28 VCC37
 - H29 VCC38
 - H32 VCC39
 - H34 VCC40
 - H35 VCC41
 - H37 VCC42
 - H38 VCC43
 - H40 VCC44
 - J26 VCC45
 - J28 VCC46
 - J29 VCC47
 - J29 VCC48
 - J34 VCC49
 - J35 VCC50
 - J37 VCC51
 - J38 VCC52
 - K34 VCC53
 - K35 VCC54
 - K37 VCC55
 - K39 VCC56
 - K42 VCC57
 - K26 VCC58
 - K27 VCC59
 - K29 VCC60
 - K32 VCC61
 - K32 VCC62
 - K34 VCC63
 - K37 VCC64
 - K39 VCC65
 - K42 VCC66
 - L26 VCC67
 - L28 VCC68
 - L29 VCC69
 - L36 VCC70
 - L40 VCC71
 - N26 VCC72
 - N30 VCC73
 - N34 VCC74
 - N36 VCC75
 - N38 VCC76

POWER

CORE SUPPLY

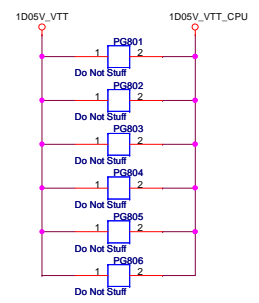
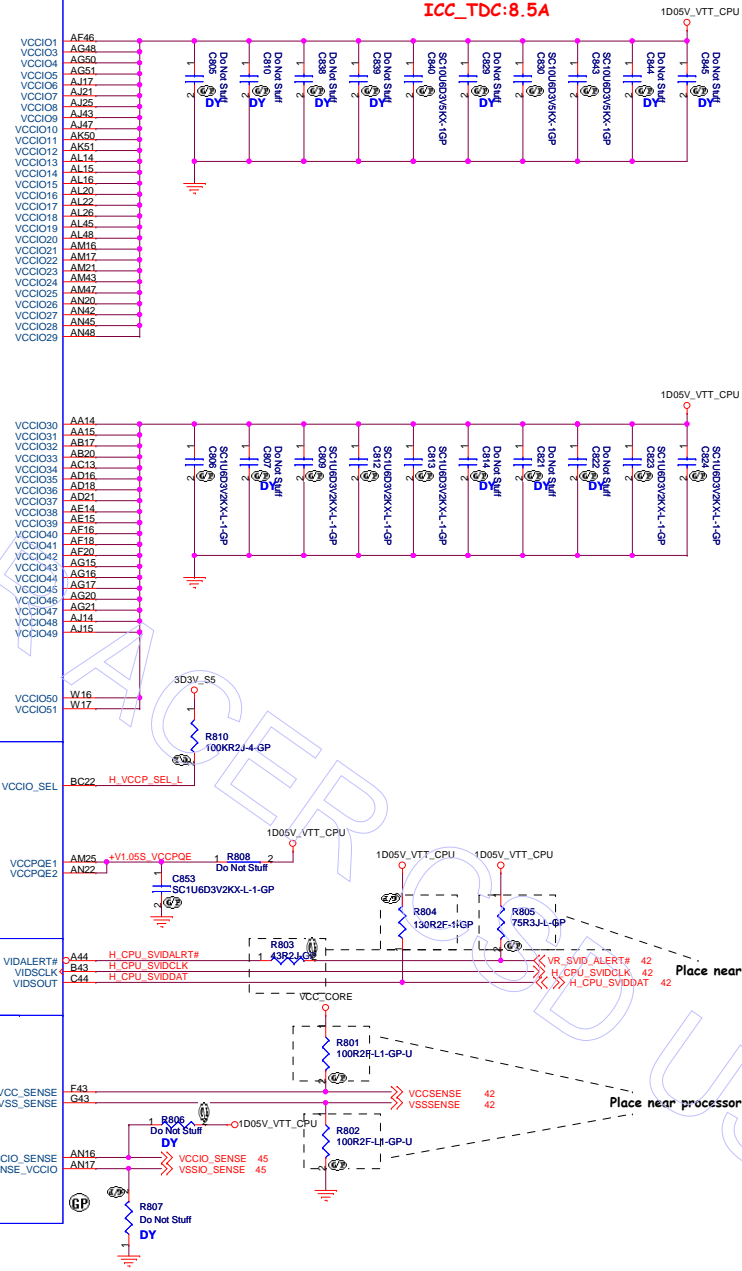
PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

RY-BRIDGE-GP-NF
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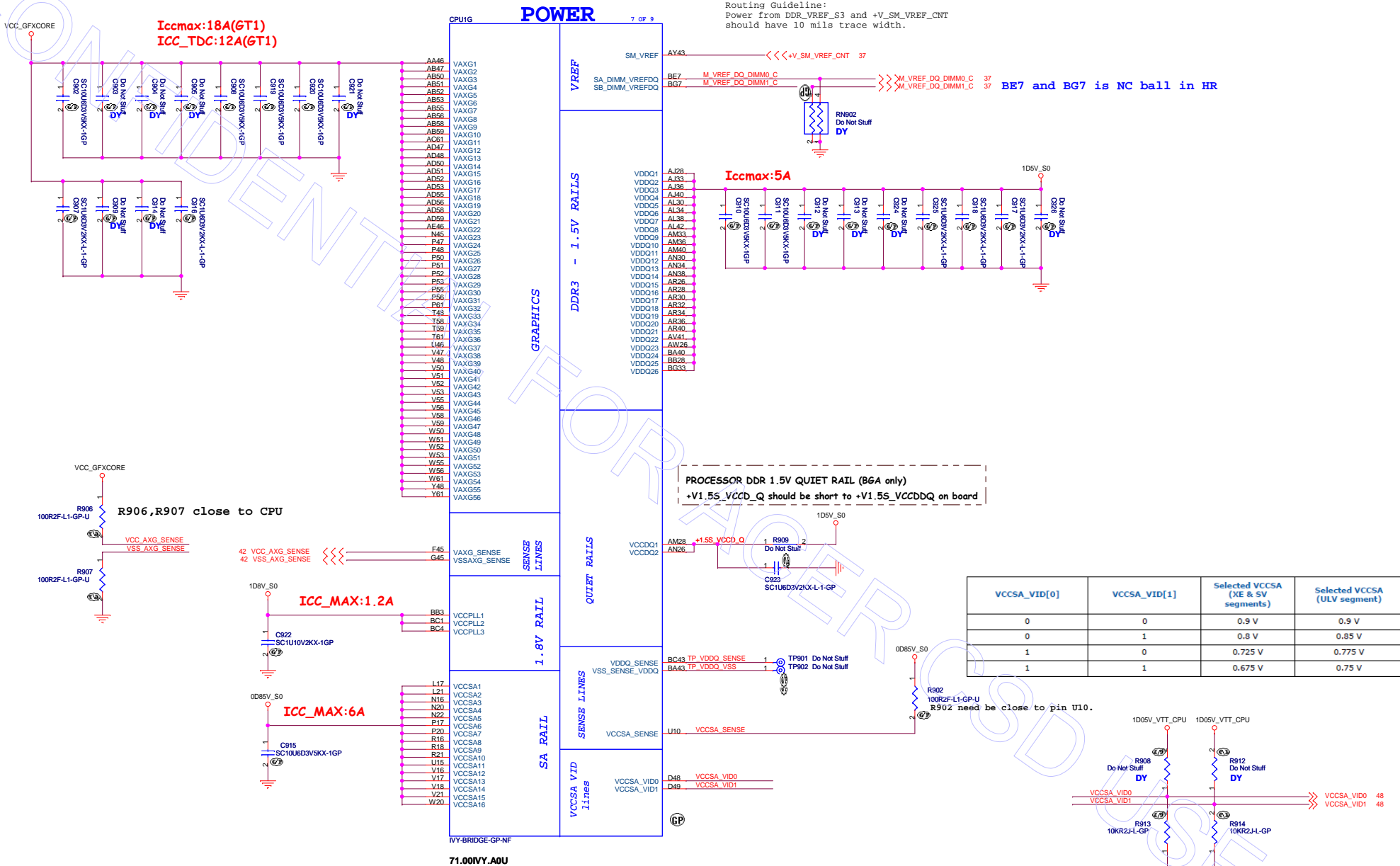
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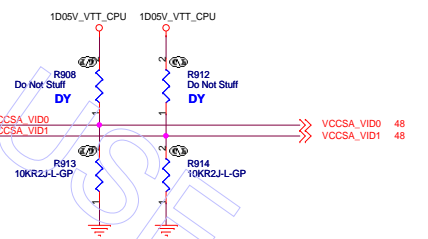
File: CPU (VCC CORE)
Size: Custom
Date: 1080909, October 09, 2012

Document Number: Husk/Petra
Rev: -4M
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Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.



VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V



SSID = CPU

CPU1H 8 OF 9

A13	VSS1	VSS91	AM38
A17	VSS2	VSS92	AM4
A27	VSS3	VSS93	AM42
A25	VSS4	VSS94	AM45
A28	VSS5	VSS95	AM48
A33	VSS6	VSS96	AM58
A37	VSS7	VSS97	AN1
A40	VSS8	VSS98	AN2
A45	VSS9	VSS99	AN25
A49	VSS10	VSS100	AN28
A53	VSS11	VSS101	AN33
A9	VSS12	VSS102	AN36
AA1	VSS13	VSS103	AN40
AA13	VSS14	VSS104	AN43
AA50	VSS15	VSS105	AN47
AA51	VSS16	VSS106	AN50
AA52	VSS17	VSS107	AN54
AA53	VSS18	VSS108	AP10
AA55	VSS19	VSS109	AP51
AA56	VSS20	VSS110	AP55
AA8	VSS21	VSS111	AP7
AB18	VSS22	VSS112	AR13
AB18	VSS23	VSS113	AR17
AB21	VSS24	VSS114	AR21
AB48	VSS25	VSS115	AR41
AB61	VSS26	VSS116	AR48
AC10	VSS27	VSS117	AR61
AC14	VSS28	VSS118	AR7
AC48	VSS29	VSS119	AT14
AC6	VSS30	VSS120	AT19
AD17	VSS31	VSS121	AT36
AD20	VSS32	VSS122	AT4
AD4	VSS33	VSS123	AT45
AD61	VSS34	VSS124	AT52
AE13	VSS35	VSS125	AT58
AE8	VSS36	VSS126	AU1
AF1	VSS37	VSS127	AU11
AF17	VSS38	VSS128	AU28
AF21	VSS39	VSS129	AU32
AF47	VSS40	VSS130	AU51
AF48	VSS41	VSS131	AU7
AF50	VSS42	VSS132	AV17
AF51	VSS43	VSS133	AV21
AF52	VSS44	VSS134	AV22
AF53	VSS45	VSS135	AV34
AF55	VSS46	VSS136	AV40
AF56	VSS47	VSS137	AV48
AF58	VSS48	VSS138	AV55
AF59	VSS49	VSS139	AW13
AG10	VSS50	VSS140	AW43
AG14	VSS51	VSS141	AW61
AG18	VSS52	VSS142	AW7
AG47	VSS53	VSS143	AY14
AG52	VSS54	VSS144	AY19
AG61	VSS55	VSS145	AY30
AG7	VSS56	VSS146	AY36
AH4	VSS57	VSS147	AY4
AH58	VSS58	VSS148	AY41
AJ13	VSS59	VSS149	AY45
AJ16	VSS60	VSS150	AY49
AJ20	VSS61	VSS151	AY55
AJ22	VSS62	VSS152	AY58
AJ26	VSS63	VSS153	AY9
AJ30	VSS64	VSS154	BA1
AJ34	VSS65	VSS155	BA11
AJ38	VSS66	VSS156	BA17
AJ42	VSS67	VSS157	BA21
AJ45	VSS68	VSS158	BA26
AJ48	VSS69	VSS159	BA32
AJ7	VSS70	VSS160	BA48
AK1	VSS71	VSS161	BA51
AK52	VSS72	VSS162	BB53
AL10	VSS73	VSS163	BC13
AL13	VSS74	VSS164	BC5
AL17	VSS75	VSS165	BC57
AL21	VSS76	VSS166	BD12
AL25	VSS77	VSS167	BD16
AL28	VSS78	VSS168	BD19
AL33	VSS79	VSS169	BD23
AL36	VSS80	VSS170	BD27
AL40	VSS81	VSS171	BD32
AL43	VSS82	VSS172	BD36
AL47	VSS83	VSS173	BD40
AL61	VSS84	VSS174	BD44
AM13	VSS85	VSS175	BD48
AM20	VSS86	VSS176	BD52
AM22	VSS87	VSS177	BD56
AM26	VSS88	VSS178	BD8
AM30	VSS89	VSS179	BE5
AM34	VSS90	VSS180	BG13

VSS

IVY-BRIDGE-GP-NF

71.00IVY.A0U



CPU1I 9 OF 9

BG17	VSS181	VSS250	M4
BG21	VSS182	VSS251	M58
BG24	VSS183	VSS252	M6
BG28	VSS184	VSS253	N1
BG37	VSS185	VSS254	N17
BG41	VSS186	VSS255	N21
BG45	VSS187	VSS256	N25
BG49	VSS188	VSS257	N28
BG53	VSS189	VSS258	N33
BG9	VSS190	VSS259	N36
C29	VSS191	VSS260	N40
C35	VSS192	VSS261	N43
C40	VSS193	VSS262	N47
D10	VSS194	VSS263	N48
D14	VSS195	VSS264	N51
D18	VSS196	VSS265	N52
D22	VSS197	VSS266	N56
D26	VSS198	VSS267	N61
D29	VSS199	VSS268	P14
D35	VSS200	VSS269	P16
D4	VSS201	VSS270	P18
D40	VSS202	VSS271	P21
D43	VSS203	VSS272	P58
D46	VSS204	VSS273	P59
D50	VSS205	VSS274	P9
D54	VSS206	VSS275	R17
D58	VSS207	VSS276	R20
D6	VSS208	VSS277	R4
E25	VSS209	VSS278	R46
E29	VSS210	VSS279	T1
E3	VSS211	VSS280	T47
F35	VSS212	VSS281	T50
F13	VSS213	VSS282	T51
F15	VSS214	VSS283	T52
F19	VSS215	VSS284	T53
F29	VSS216	VSS285	T55
F35	VSS217	VSS286	T56
F35	VSS218	VSS287	U13
F40	VSS219	VSS288	U8
G51	VSS220	VSS289	V20
G6	VSS221	VSS290	V61
G61	VSS222	VSS291	W13
H10	VSS223	VSS292	W15
H14	VSS224	VSS293	W18
H17	VSS225	VSS294	W21
H21	VSS226	VSS295	W46
H4	VSS227	VSS296	W8
H53	VSS228	VSS297	Y4
H58	VSS229	VSS298	Y47
J1	VSS230	VSS299	Y58
J49	VSS231	VSS300	Y59
J55	VSS232		
K11	VSS233		
K21	VSS234		
K51	VSS235		
K8	VSS236		
L16	VSS237		
L20	VSS238		
L22	VSS239		
L26	VSS240		
L30	VSS241		
L34	VSS242		
L38	VSS243		
L43	VSS244		
L48	VSS245		
L61	VSS246		
M11	VSS247		
M15	VSS248		
M15	VSS249		

VSS

NCTF

NCTF TEST PIN :
 A5, A57, EC61, BG5
 BG57, C3, E1, E61
 VSS_NCTF_1#A5
 VSS_NCTF_2#A57
 VSS_NCTF_3#BC61
 VSS_NCTF_8#BG5
 VSS_NCTF_9#BG57
 VSS_NCTF_10#C3
 VSS_NCTF_13#E1
 VSS_NCTF_14#E61
 VSS_NCTF_4
 VSS_NCTF_5
 VSS_NCTF_6
 VSS_NCTF_7
 VSS_NCTF_11
 VSS_NCTF_12

IVY-BRIDGE-GP-NF

71.00IVY.A0U



IVB

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CPU (VSS)			
Size A3	Document Number Husk/Petra	Rev -2	
Date: Thursday, April 19, 2012	Sheet 10	of 103	

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
XDP			
Size	Document Number	Rev	
A3	Husk/Petra	-2	
Date:	Thursday, April 19, 2012	Sheet	11 of 103

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Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012 Sheet 12 of 103

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Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
------------	--------------------------------------	------------------

SSID = MEMORY

M_A_A[15:0] 6

M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS[7:0] 6
M_A_DQS[7:0] 6

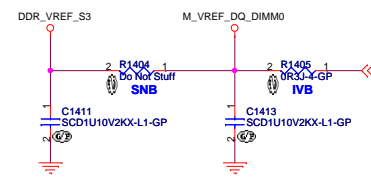
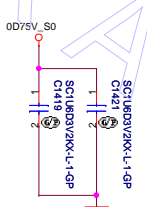
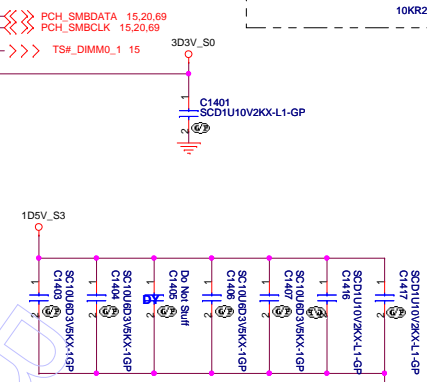
M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6

DDR_VREF_S3
M_VREF_DQ_DIMM0
15.37 DDR3_DRAMRST#

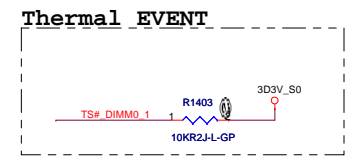
M_A A0	98	A0
M_A A1	97	A1
M_A A2	96	A2
M_A A3	95	A3
M_A A4	92	A4
M_A A5	91	A5
M_A A6	90	A6
M_A A7	86	A7
M_A A8	89	A8
M_A A9	88	A9
M_A A10	107	A10/AP
M_A A11	84	A11
M_A A12	83	A12
M_A A13	118	A13
M_A A14	80	A14
M_A A15	78	A15
M_A A16/BA2	79	A16/BA2
M_A BA0	109	BA0
M_A BA1	108	BA1
M_A DQ0	5	DQ0
M_A DQ1	7	DQ1
M_A DQ2	15	DQ2
M_A DQ3	17	DQ3
M_A DQ4	4	DQ4
M_A DQ5	6	DQ5
M_A DQ6	16	DQ6
M_A DQ7	18	DQ7
M_A DQ8	21	DQ8
M_A DQ9	23	DQ9
M_A DQ10	33	DQ10
M_A DQ11	35	DQ11
M_A DQ12	22	DQ12
M_A DQ13	24	DQ13
M_A DQ14	34	DQ14
M_A DQ15	36	DQ15
M_A DQ16	39	DQ16
M_A DQ17	41	DQ17
M_A DQ18	51	DQ18
M_A DQ19	53	DQ19
M_A DQ20	42	DQ20
M_A DQ21	40	DQ21
M_A DQ22	50	DQ22
M_A DQ23	52	DQ23
M_A DQ24	67	DQ24
M_A DQ25	59	DQ25
M_A DQ26	67	DQ26
M_A DQ27	69	DQ27
M_A DQ28	66	DQ28
M_A DQ29	58	DQ29
M_A DQ30	68	DQ30
M_A DQ31	70	DQ31
M_A DQ32	129	DQ32
M_A DQ33	131	DQ33
M_A DQ34	141	DQ34
M_A DQ35	143	DQ35
M_A DQ36	130	DQ36
M_A DQ37	132	DQ37
M_A DQ38	140	DQ38
M_A DQ39	142	DQ39
M_A DQ40	147	DQ40
M_A DQ41	149	DQ41
M_A DQ42	157	DQ42
M_A DQ43	159	DQ43
M_A DQ44	146	DQ44
M_A DQ45	148	DQ45
M_A DQ46	158	DQ46
M_A DQ47	160	DQ47
M_A DQ48	163	DQ48
M_A DQ49	165	DQ49
M_A DQ50	175	DQ50
M_A DQ51	177	DQ51
M_A DQ52	164	DQ52
M_A DQ53	166	DQ53
M_A DQ54	174	DQ54
M_A DQ55	176	DQ55
M_A DQ56	181	DQ56
M_A DQ57	183	DQ57
M_A DQ58	191	DQ58
M_A DQ59	193	DQ59
M_A DQ60	180	DQ60
M_A DQ61	182	DQ61
M_A DQ62	192	DQ62
M_A DQ63	194	DQ63
M_A DQS#0	10	DQS#0
M_A DQS#1	27	DQS#1
M_A DQS#2	45	DQS#2
M_A DQS#3	62	DQS#3
M_A DQS#4	135	DQS#4
M_A DQS#5	152	DQS#5
M_A DQS#6	169	DQS#6
M_A DQS#7	186	DQS#7
M_A DQS0	12	DQS0
M_A DQS1	29	DQS1
M_A DQS2	47	DQS2
M_A DQS3	64	DQS3
M_A DQS4	137	DQS4
M_A DQS5	154	DQS5
M_A DQS6	171	DQS6
M_A DQS7	188	DQS7
M_A DIM0_ODT0	116	ODT0
M_A DIM0_ODT1	120	ODT1
DDR_VREF_S3	126	VREF_CA
M_VREF_DQ_DIMM0	1	VREF_DQ
RESET#	30	RESET#
VTT1	203	VTT1
VTT2	204	VTT2

NP1	NP1
NP2	NP2
RAS#	110
WE#	113
CAS#	115
CS0#	114
CS1#	121
CKE0	73
CKE1	74
CK0	101
CK0	103
CK1	102
CK1#	104
DM0	11
DM1	28
DM2	46
DM3	63
DM4	136
DM5	153
DM6	170
DM7	187
SDA	200
SCL	202
EVENT#	198
VDDSPD	199
SA0	197
SA1	201
NC#1	77
NC#	122
NC#/TEST	125
VDD1	75
VDD2	76
VDD3	81
VDD4	82
VDD5	87
VDD6	88
VDD7	93
VDD8	94
VDD9	99
VDD10	100
VDD11	105
VDD12	106
VDD13	111
VDD14	112
VDD15	117
VDD16	118
VDD17	123
VDD18	124
VDD19	128
VDD20	129
VDD21	130
VDD22	131
VDD23	132
VDD24	133
VDD25	134
VDD26	135
VDD27	136
VDD28	137
VDD29	138
VDD30	139
VDD31	140
VDD32	141
VDD33	142
VDD34	143
VDD35	144
VDD36	145
VDD37	146
VDD38	147
VDD39	148
VDD40	149
VDD41	150
VDD42	151
VDD43	152
VDD44	153
VDD45	154
VDD46	155
VDD47	156
VDD48	157
VDD49	158
VDD50	159
VDD51	160
VDD52	161
VDD53	162
VDD54	163
VDD55	164
VDD56	165
VDD57	166
VDD58	167
VDD59	168
VDD60	169
VDD61	170
VDD62	171
VDD63	172
VDD64	173
VDD65	174
VDD66	175
VDD67	176
VDD68	177
VDD69	178
VDD70	179
VDD71	180
VDD72	181
VDD73	182
VDD74	183
VDD75	184
VDD76	185
VDD77	186
VDD78	187
VDD79	188
VDD80	189
VDD81	190
VDD82	191
VDD83	192
VDD84	193
VDD85	194
VDD86	195
VDD87	196
VDD88	197
VDD89	198
VDD90	199
VDD91	200
VDD92	201
VDD93	202
VDD94	203
VDD95	204
VDD96	205
VDD97	206

DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.M51
3rd = 62.10024.G21



Tracew should be at least 20 mils wide



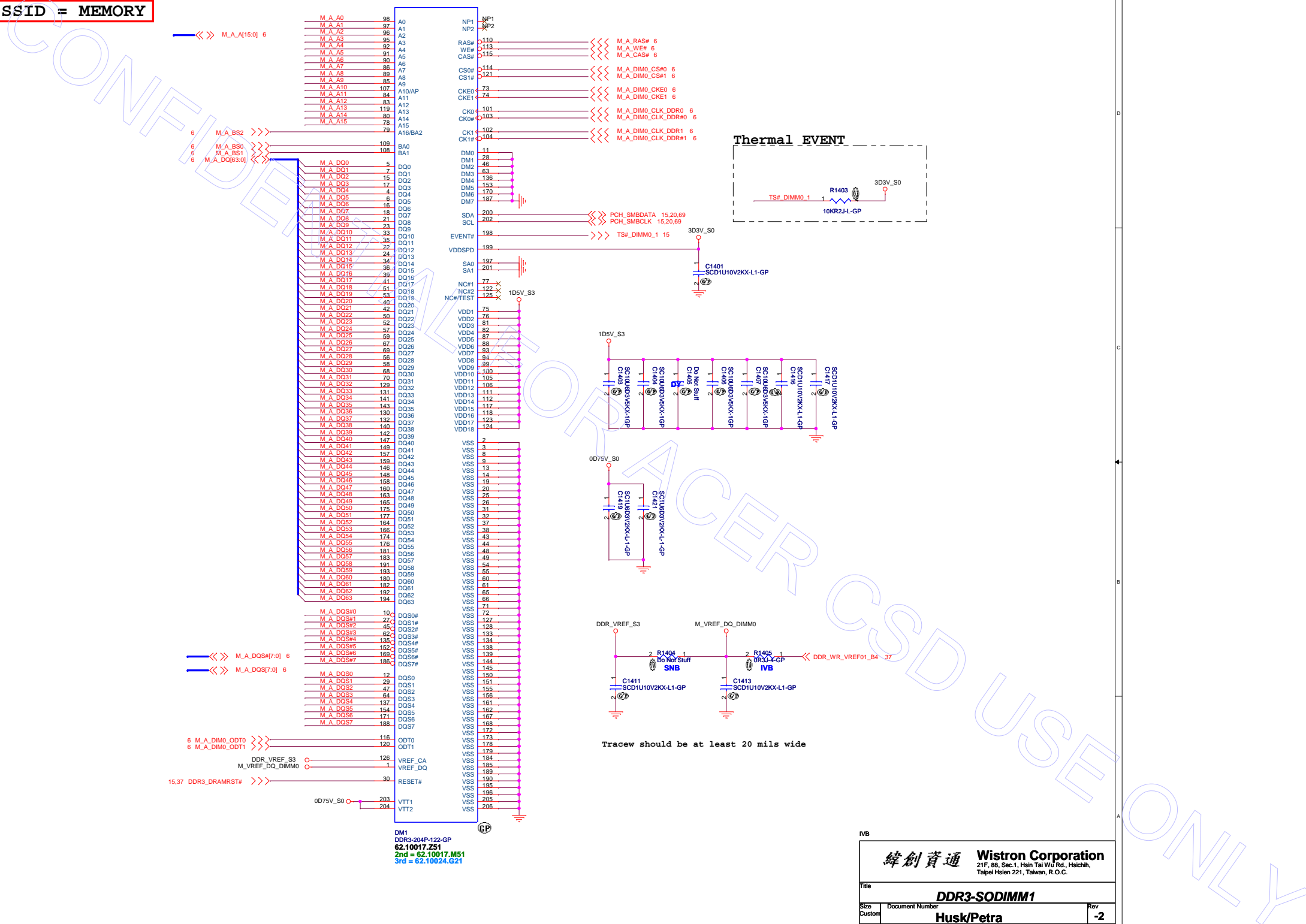
Wistron Corporation
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Title: **DDR3-SODIMM1**

Document Number: **Husk/Petra**

Rev: **-2**

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SSID = MEMORY

6 M_B_A[15:0] 6

6 M_B_BS2

6 M_B_BS0

6 M_B_BS1

6 M_B_DQ[63:0]

6 M_B_DQS#[7:0] 6

6 M_B_DQS#[7:0] 6

6 M_B_DIM0_ODT0

6 M_B_DIM0_ODT1

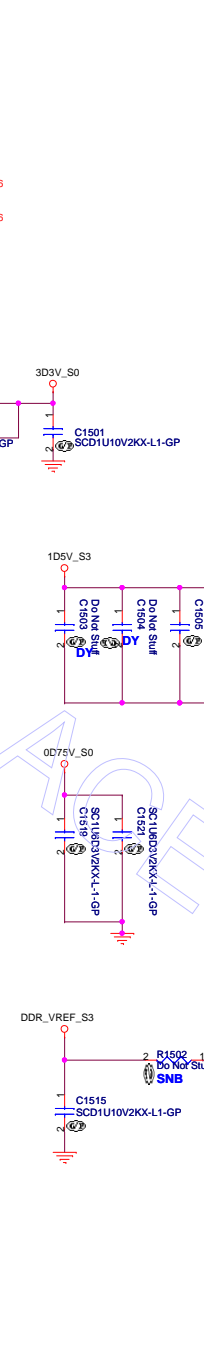
DDR_VREF_S3

M_VREF_DQ_DIMM1

14.37 DDR3_DRAMRST#

M_B A0	36
M_B A1	37
M_B A2	96
M_B A3	95
M_B A4	92
M_B A5	91
M_B A6	90
M_B A7	86
M_B A8	89
M_B A9	85
M_B A10	107
M_B A11	84
M_B A12	83
M_B A13	119
M_B A14	80
M_B A15	78
A16/BA2	79
BA0	109
BA1	108
M_B DQ0	5
M_B DQ1	7
M_B DQ2	15
M_B DQ3	17
M_B DQ4	4
M_B DQ5	6
M_B DQ6	16
M_B DQ7	18
M_B DQ8	21
M_B DQ9	23
M_B DQ10	33
M_B DQ11	35
M_B DQ12	22
M_B DQ13	24
M_B DQ14	34
M_B DQ15	36
M_B DQ16	39
M_B DQ17	41
M_B DQ18	51
M_B DQ19	53
M_B DQ20	40
M_B DQ21	42
M_B DQ22	50
M_B DQ23	52
M_B DQ24	47
M_B DQ25	59
M_B DQ26	67
M_B DQ27	69
M_B DQ28	56
M_B DQ29	58
M_B DQ30	60
M_B DQ31	70
M_B DQ32	129
M_B DQ33	131
M_B DQ34	141
M_B DQ35	143
M_B DQ36	130
M_B DQ37	132
M_B DQ38	140
M_B DQ39	142
M_B DQ40	147
M_B DQ41	149
M_B DQ42	157
M_B DQ43	159
M_B DQ44	146
M_B DQ45	148
M_B DQ46	158
M_B DQ47	160
M_B DQ48	163
M_B DQ49	165
M_B DQ50	175
M_B DQ51	177
M_B DQ52	164
M_B DQ53	166
M_B DQ54	174
M_B DQ55	176
M_B DQ56	181
M_B DQ57	183
M_B DQ58	191
M_B DQ59	193
M_B DQ60	180
M_B DQ61	182
M_B DQ62	192
M_B DQ63	194
M_B DQS#0	10C
M_B DQS#1	12C
M_B DQS#2	45C
M_B DQS#3	62C
M_B DQS#4	135C
M_B DQS#5	152C
M_B DQS#6	169C
M_B DQS#7	186C
M_B DQS#0	12
M_B DQS#1	29
M_B DQS#2	47
M_B DQS#3	64
M_B DQS#4	137
M_B DQS#5	154
M_B DQS#6	171
M_B DQS#7	188
M_B DIM0_ODT0	116
M_B DIM0_ODT1	120
DDR_VREF_S3	126
M_VREF_DQ_DIMM1	1
14.37 DDR3_DRAMRST#	30
OD75V_S0	203
	204

NP1	110
NP2	113
RAS#	115
WE#	114
CAS#	121
CS0#	73
CS1#	74
CKE0	101
CKE1	103
CK0	102
CK0#	104
CK1	11
CK1#	28
DM0	46
DM1	63
DM2	136
DM3	153
DM4	170
DM5	187
DM6	170
DM7	187
SDA	200
SCL	202
EVENT#	198
VDDSPD	199
SA0	197
SA1	201
NC#1	77 X
NC#2	122 X
NC#/TEST	125 X
VDD1	75
VDD2	76
VDD3	81
VDD4	82
VDD5	87
VDD6	88
VDD7	93
VDD8	94
VDD9	99
VDD10	100
VDD11	105
VDD12	106
VDD13	111
VDD14	112
VDD15	117
VDD16	118
VDD17	123
VDD18	124
VSS	2
VSS	3
VSS	8
VSS	9
VSS	13
VSS	14
VSS	19
VSS	20
VSS	25
VSS	26
VSS	31
VSS	32
VSS	37
VSS	38
VSS	43
VSS	48
VSS	49
VSS	54
VSS	55
VSS	60
VSS	61
VSS	65
VSS	66
VSS	71
VSS	72
VSS	127
VSS	128
VSS	133
VSS	134
VSS	138
VSS	139
VSS	144
VSS	145
VSS	150
VSS	151
VSS	155
VSS	162
VSS	167
VSS	168
VSS	172
VSS	173
VSS	178
VSS	179
VSS	184
VSS	185
VSS	189
VSS	190
VSS	195
VSS	196
VSS	205
VSS	206
M_B_RAS#	6
M_B_WE#	6
M_B_CAS#	6
M_B_DIM0_CS#0	6
M_B_DIM0_CS#1	6
M_B_DIM0_CKE0	6
M_B_DIM0_CKE1	6
M_B_DIM0_CLK_DDR0	6
M_B_DIM0_CLK_DDR#0	6
M_B_DIM0_CLK_DDR1	6
M_B_DIM0_CLK_DDR#1	6
PCH_SMBDATA	14.20.69
PCH_SMBCLK	14.20.69
TS#_DIMM0_1	14
R1501	Y0KR24L-GP
R1502	SMB
R1503	IVB



DM2
DDR3-204P-122-GP
62.10017.251
2nd = 62.10017.M51
3rd = 62.10024.G21

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
DDR3-SODIMM2		
Title	Document Number	Rev
	Husk/Petra	-2
Date: Thursday, April 19, 2012	Sheet 15 of 102	

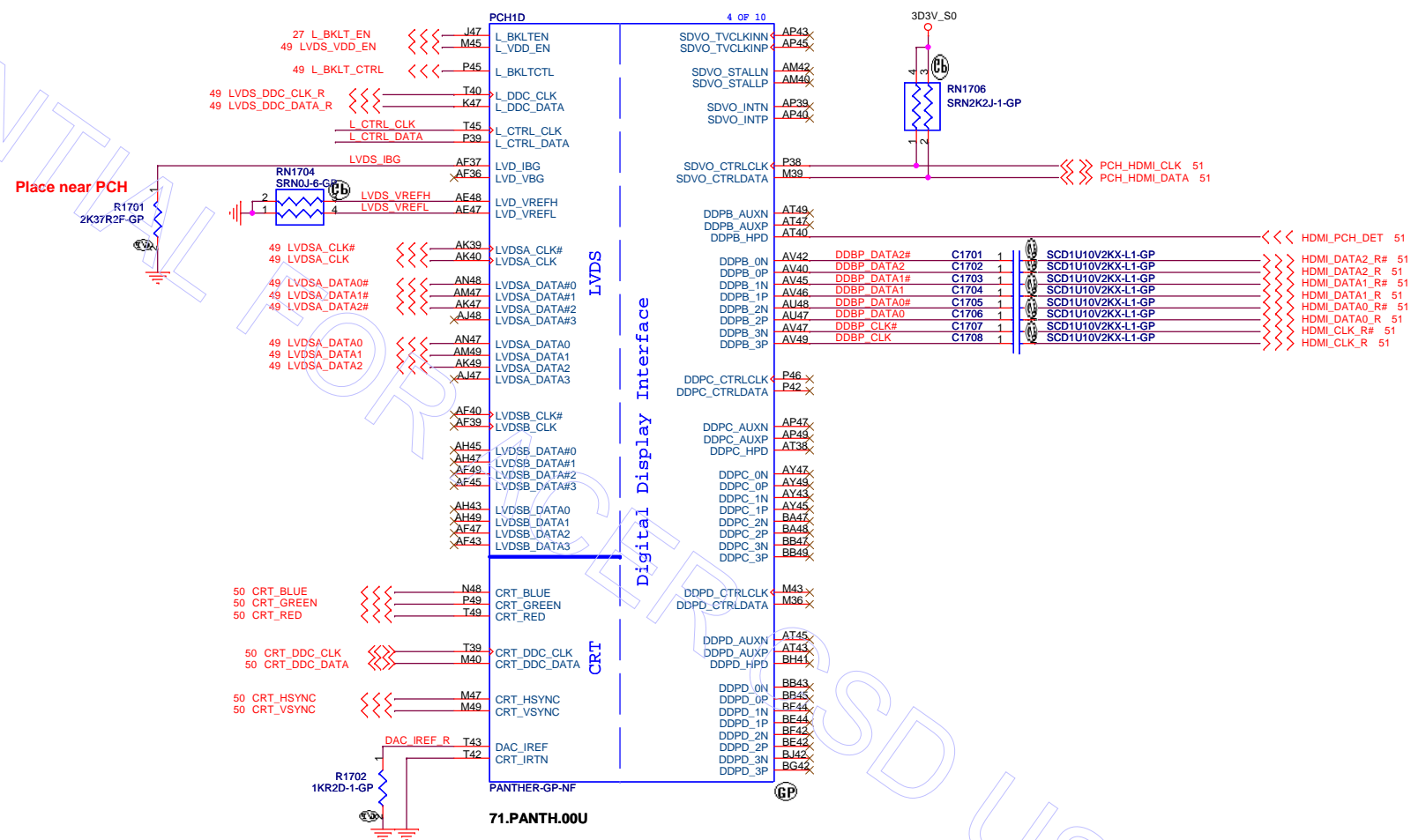
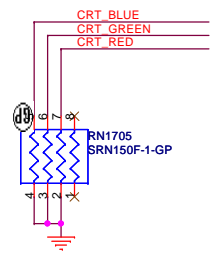
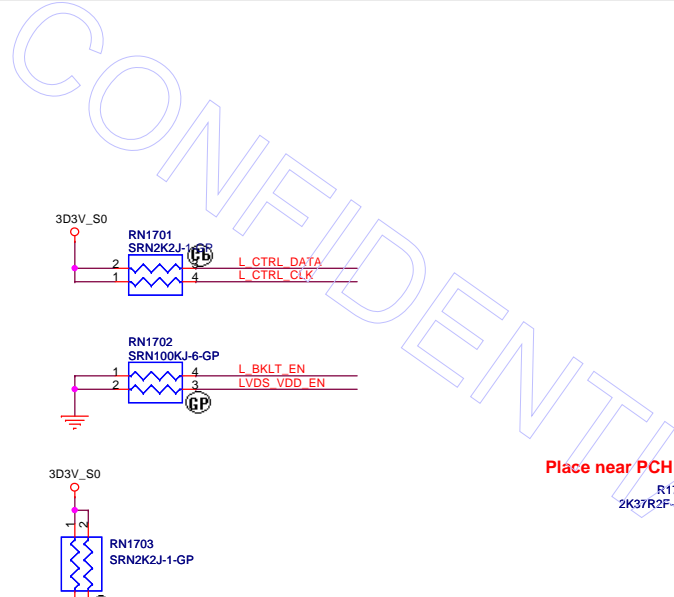
CONFIDENTIAL USE ONLY

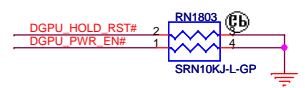
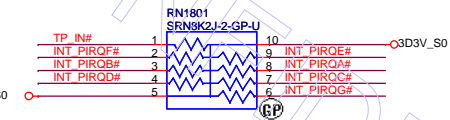
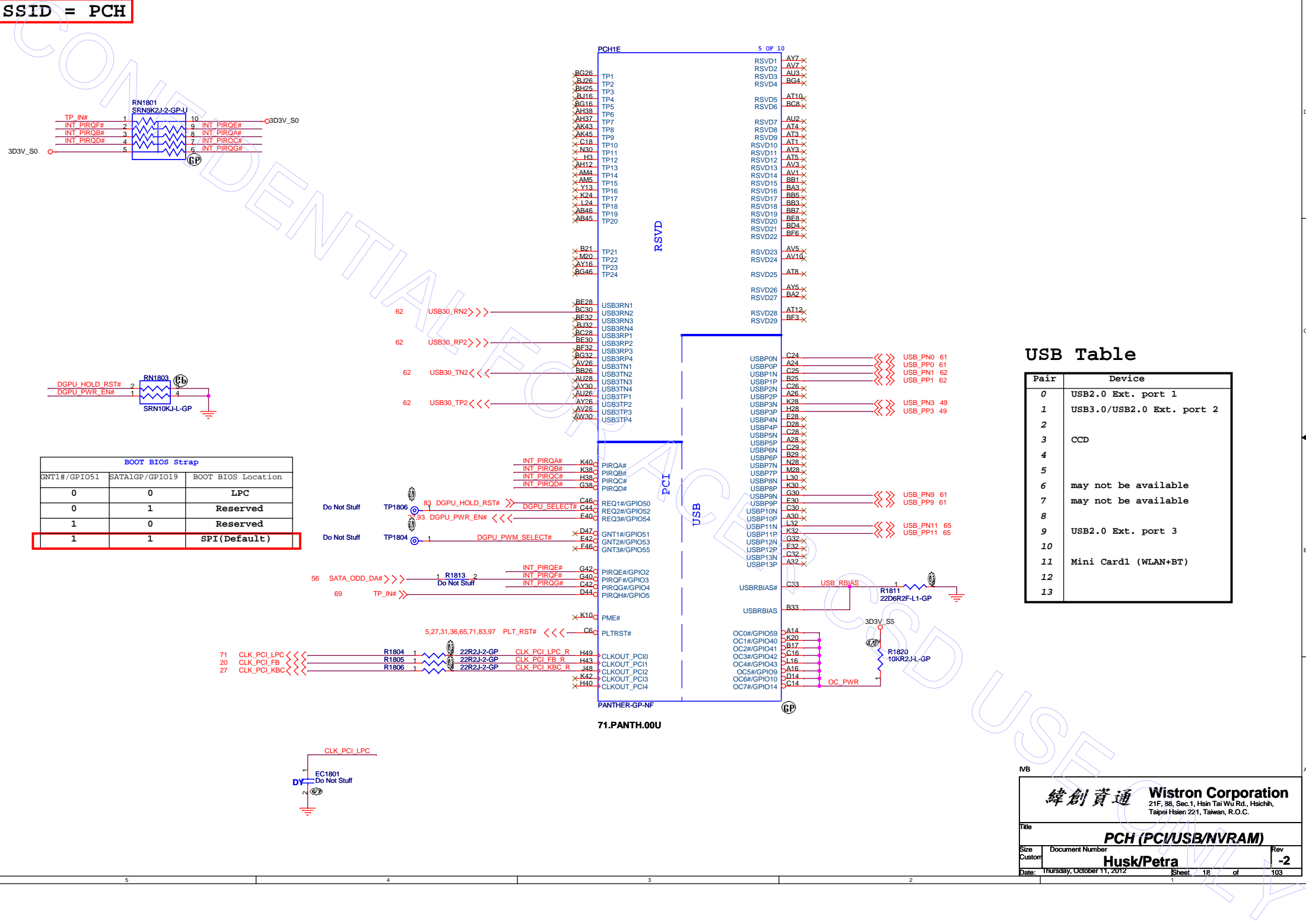
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IVB

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Title			
DDR3-SODIMM2			
Size	Document Number		Rev
A4	Husk/Petra		-2
Date: Thursday, April 19, 2012		Sheet 16	of 103





BOOT BIOS Strap		
SNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

Do Not Stuff TP1806

Do Not Stuff TP1804

Do Not Stuff

Do Not Stuff

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	
3	CCD
4	
5	may not be available
6	may not be available
7	
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

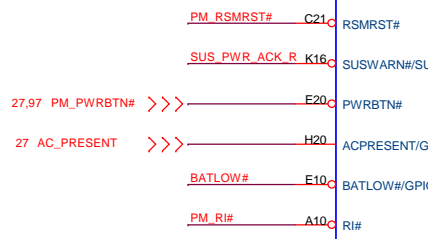
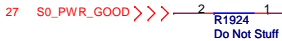
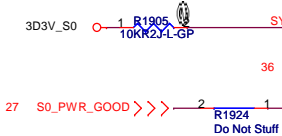
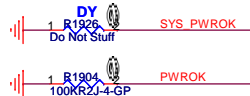
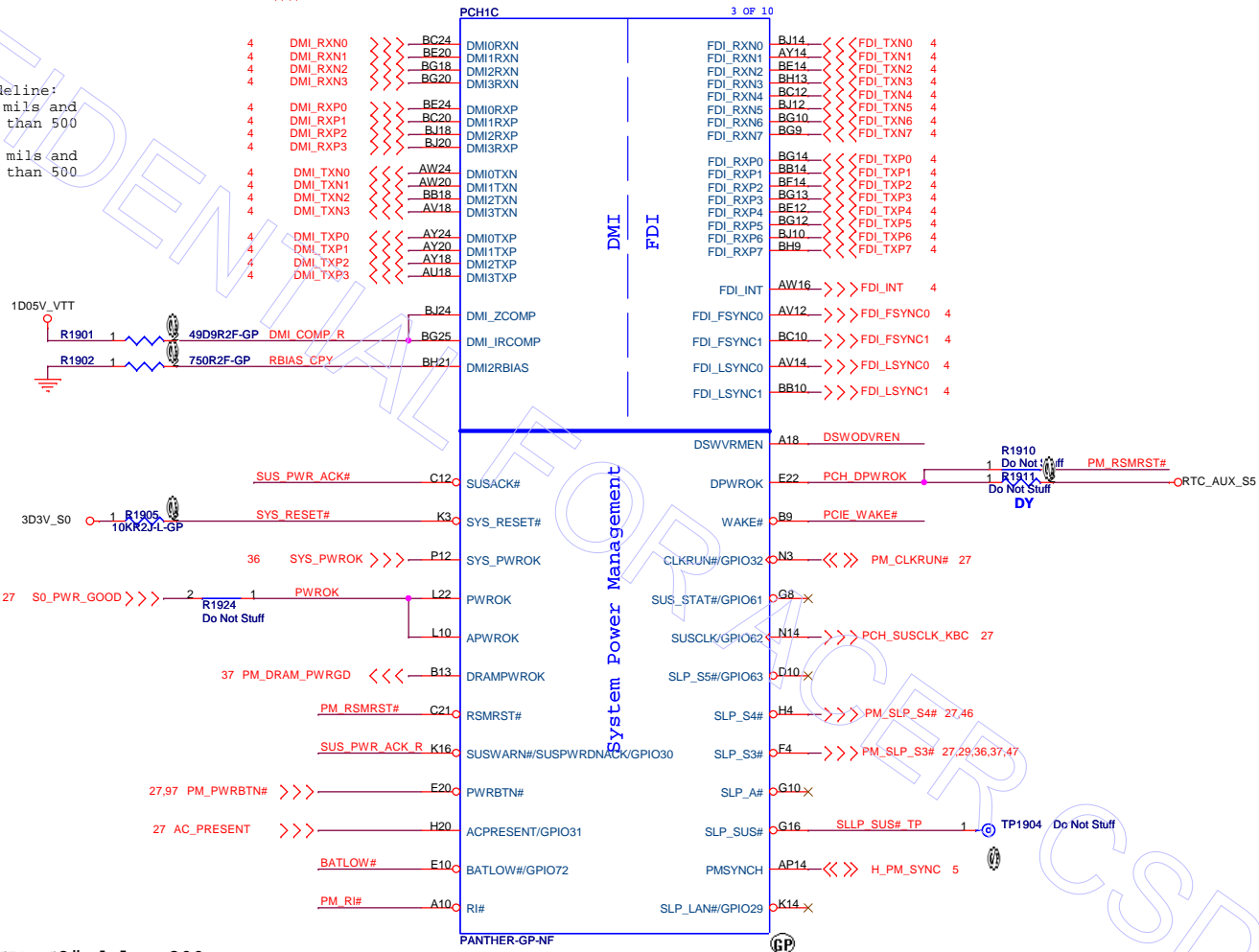
Title PCH (PCI/USB/NVRAM)
Size Custom
Document Number Husk/Petra
Date Thursday, October 11, 2012

Rev -2
 Sheet 18 of 103

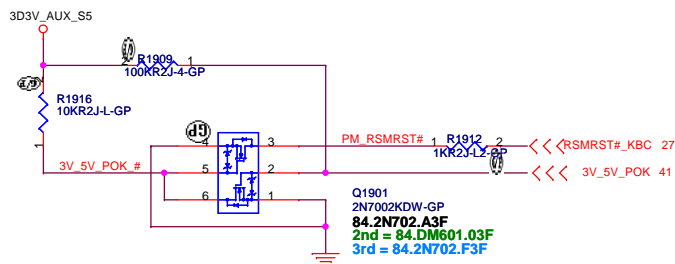
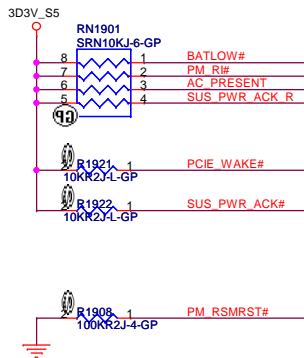
SSID = PCH



Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

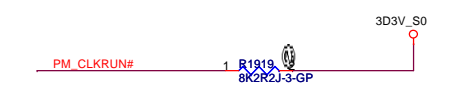


S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

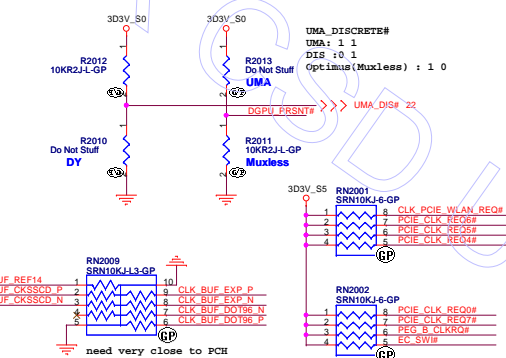
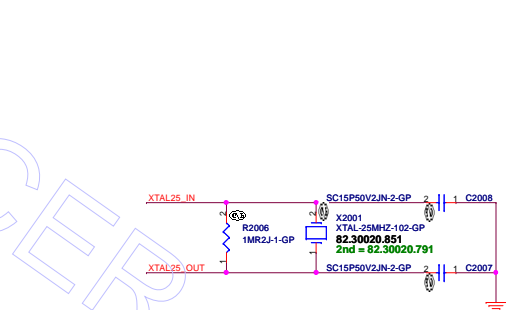
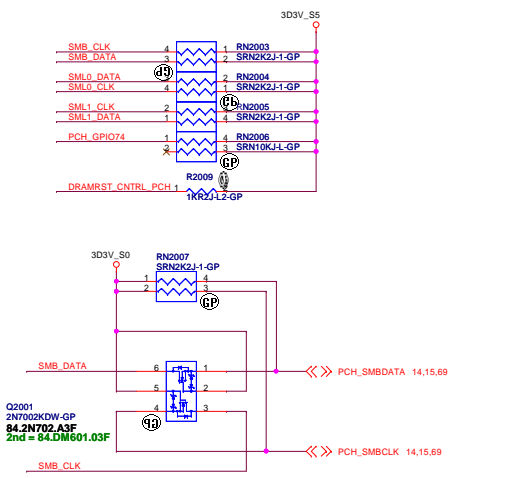
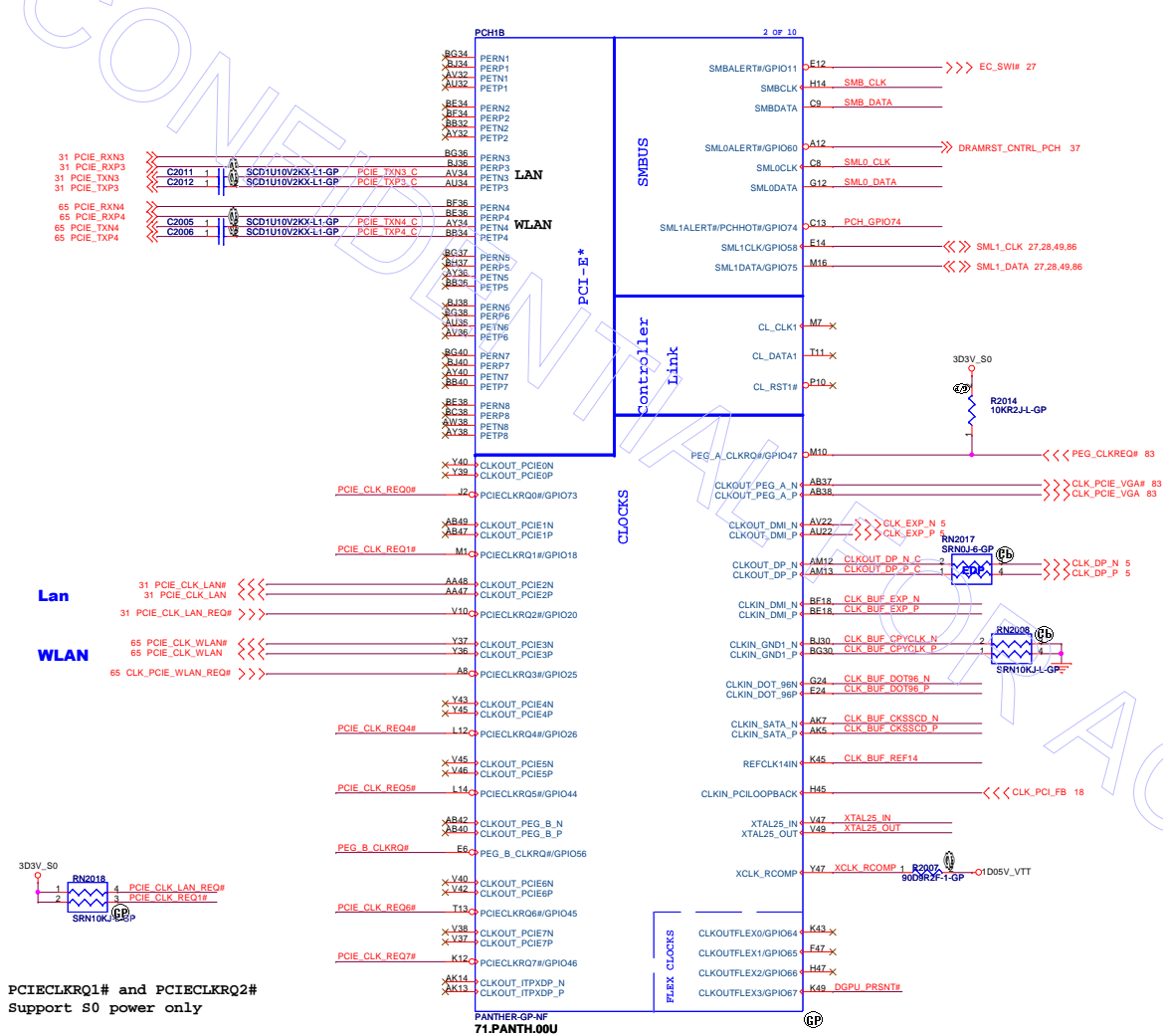


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled



SSID = PCH



PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

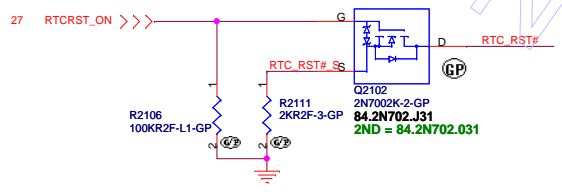
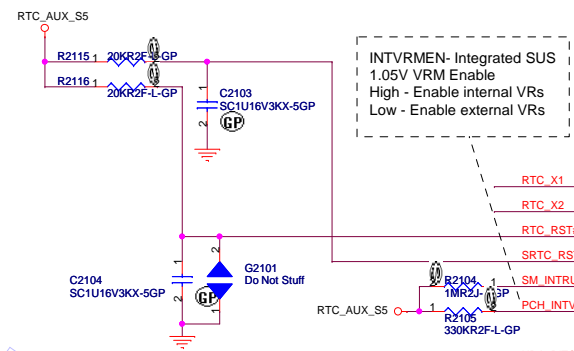
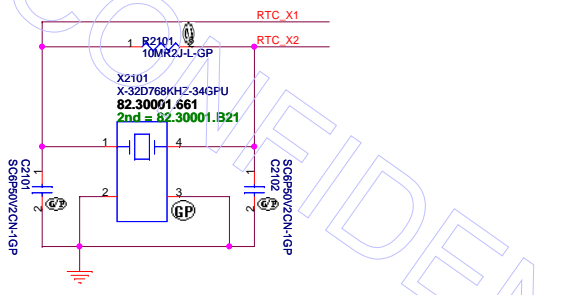
PCH (PCI-E/SMBUS/CLOCK/CL)

Customer: **Husk/Petra**

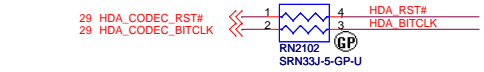
Date: 1/25/2012, October 05, 2012

Sheet 20 of 103

SSID = PCH

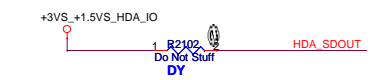


RTC Reset



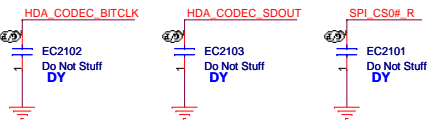
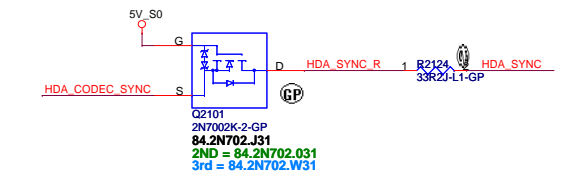
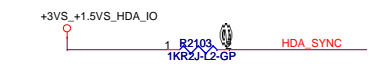
Flash Descriptor Security Override

HDA_SDOUT	Low = Default High = Enable
-----------	--------------------------------

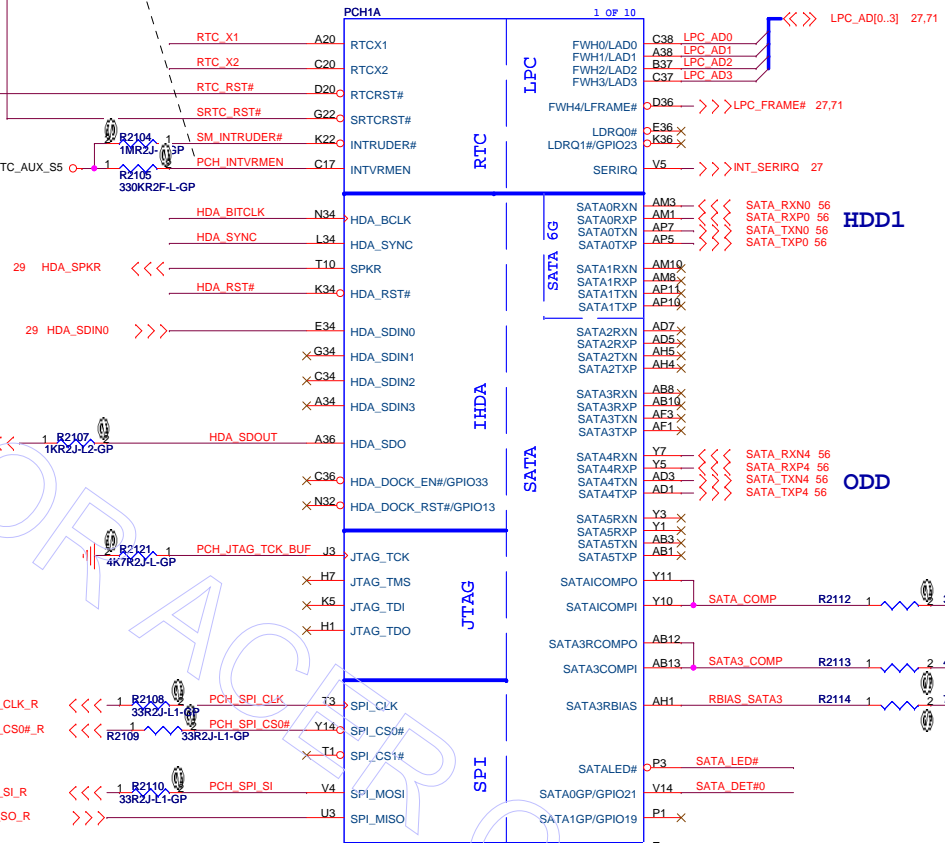


PLL ODVR VOLTAGE

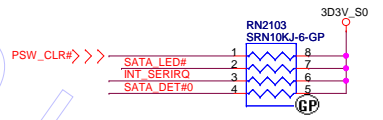
HDA_SYNC	Low = 1.8V (Default) High = 1.5V
----------	-------------------------------------



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



71.PANTH.00U

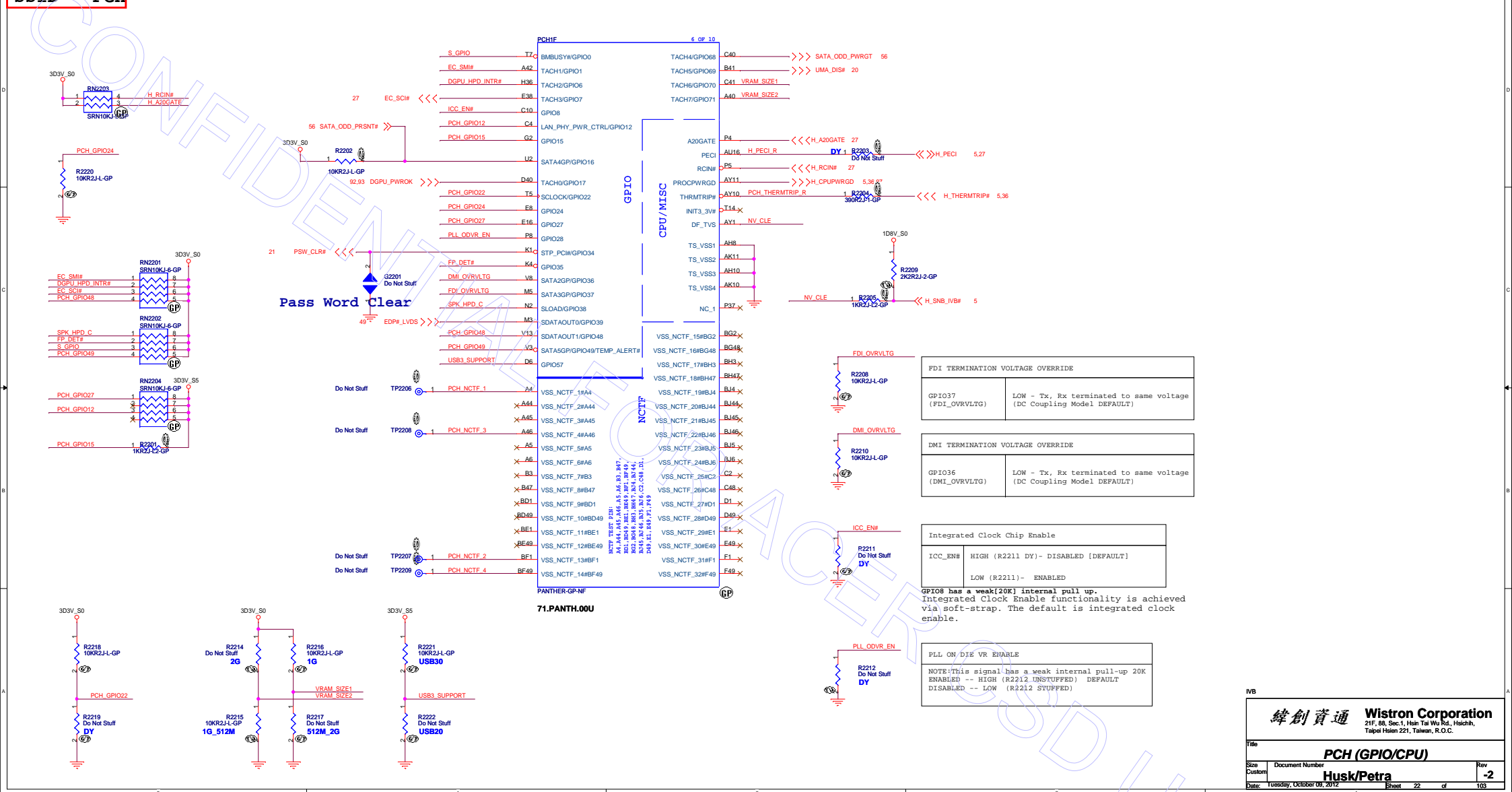


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PCH (SPI/RTC/LPC/SATA/IHDA)

Size: Custom Document Number
Date: Tuesday, October 09, 2012 Sheet 21 of 103

SSID = PCH



FDI OVRVLTG	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI OVRVLTG	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICG_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

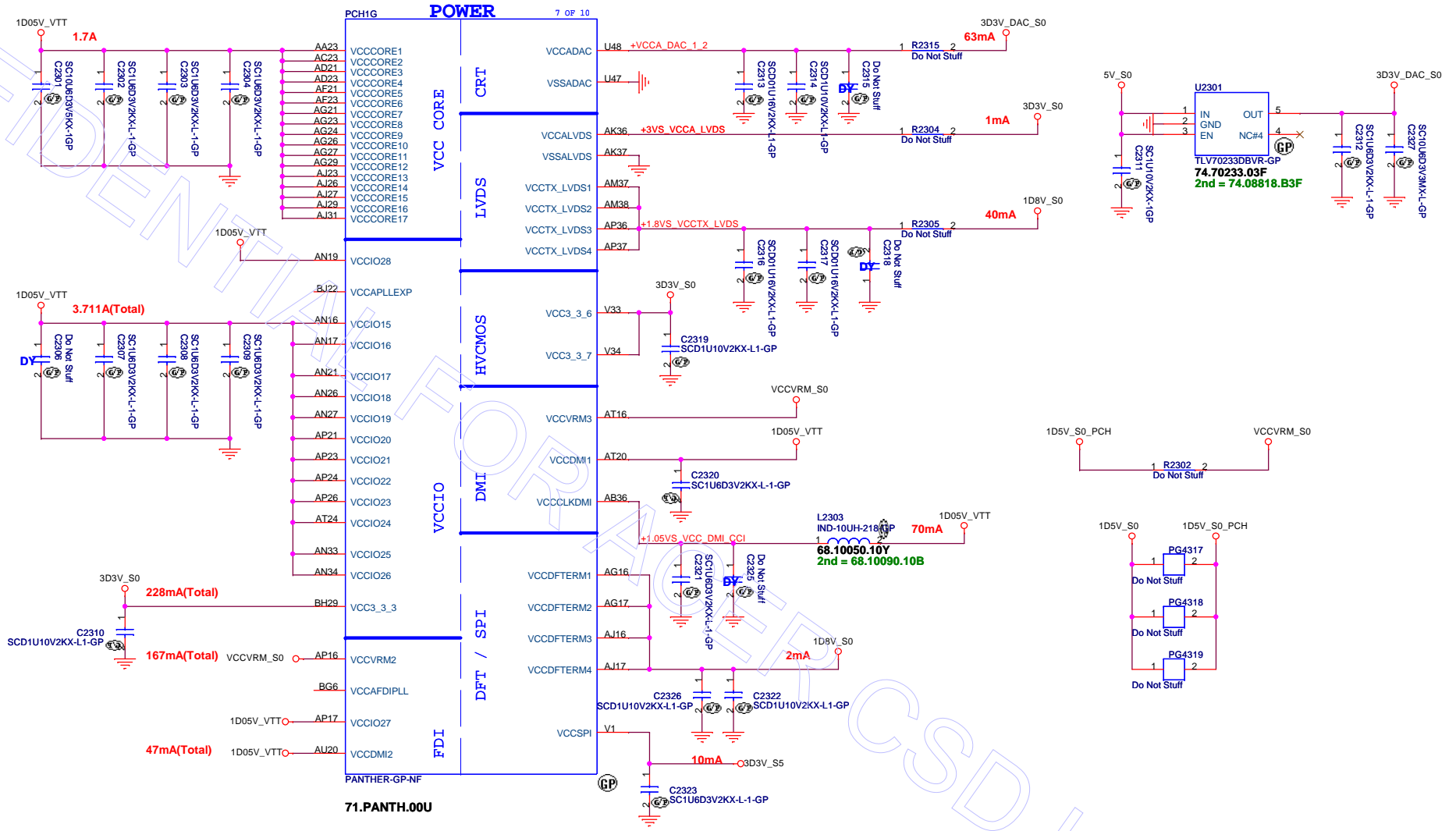
PLL ON DJE VR ENARLE	
	NOTE: This signal has a weak internal pull-up 20K
	ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
	DISABLED -- LOW (R2212 STUFFED)

IVB

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Title		
PCH (GPIO/CPU)		
Size Custom	Document Number	Rev
	Husk/Petra	-2
Date: 10/09/2012	Sheet 22	of 103

FOR INTERNAL USE ONLY



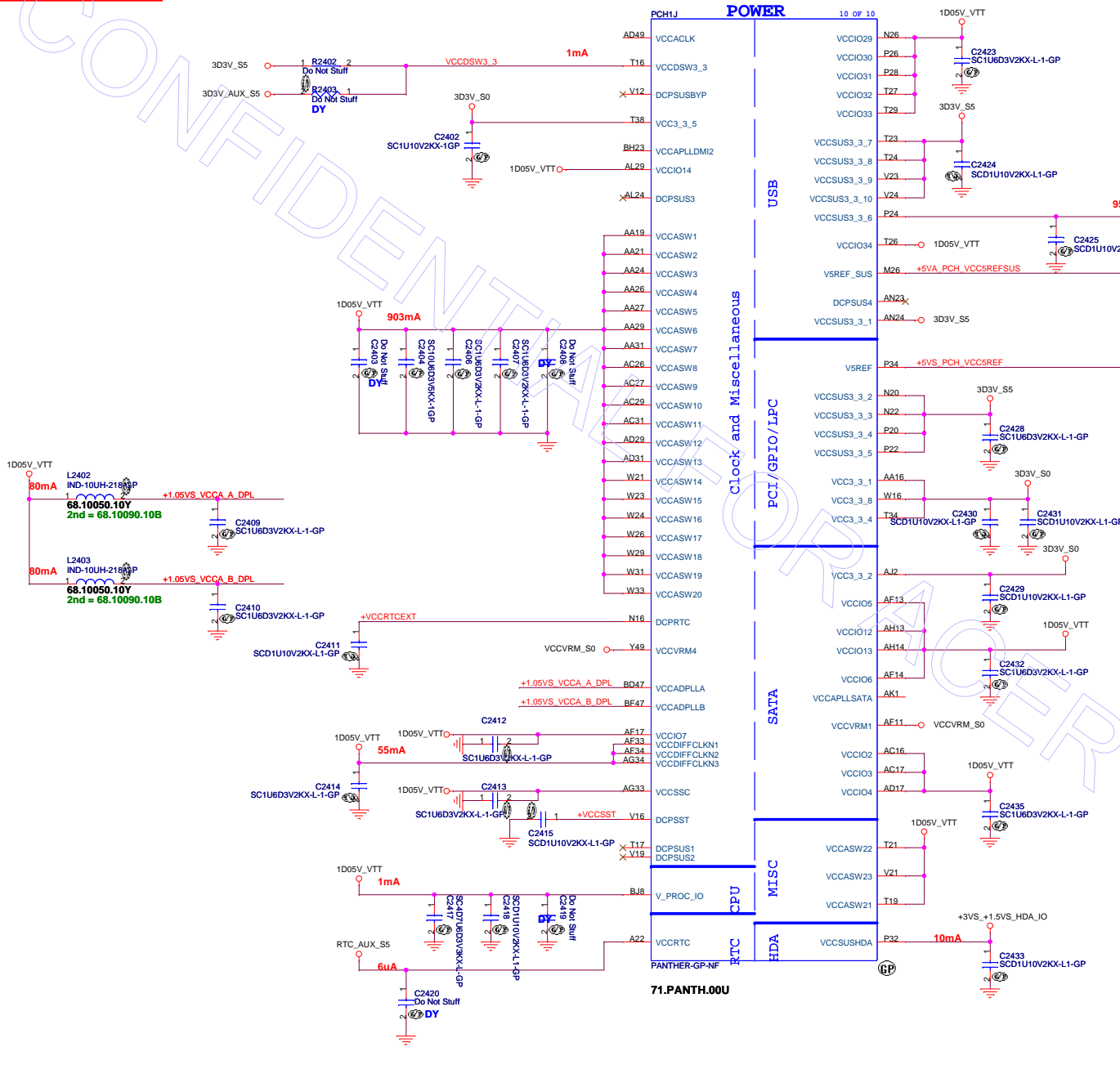
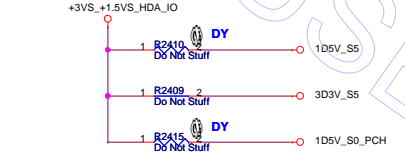
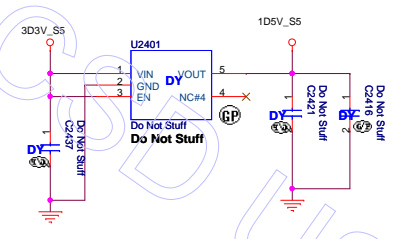


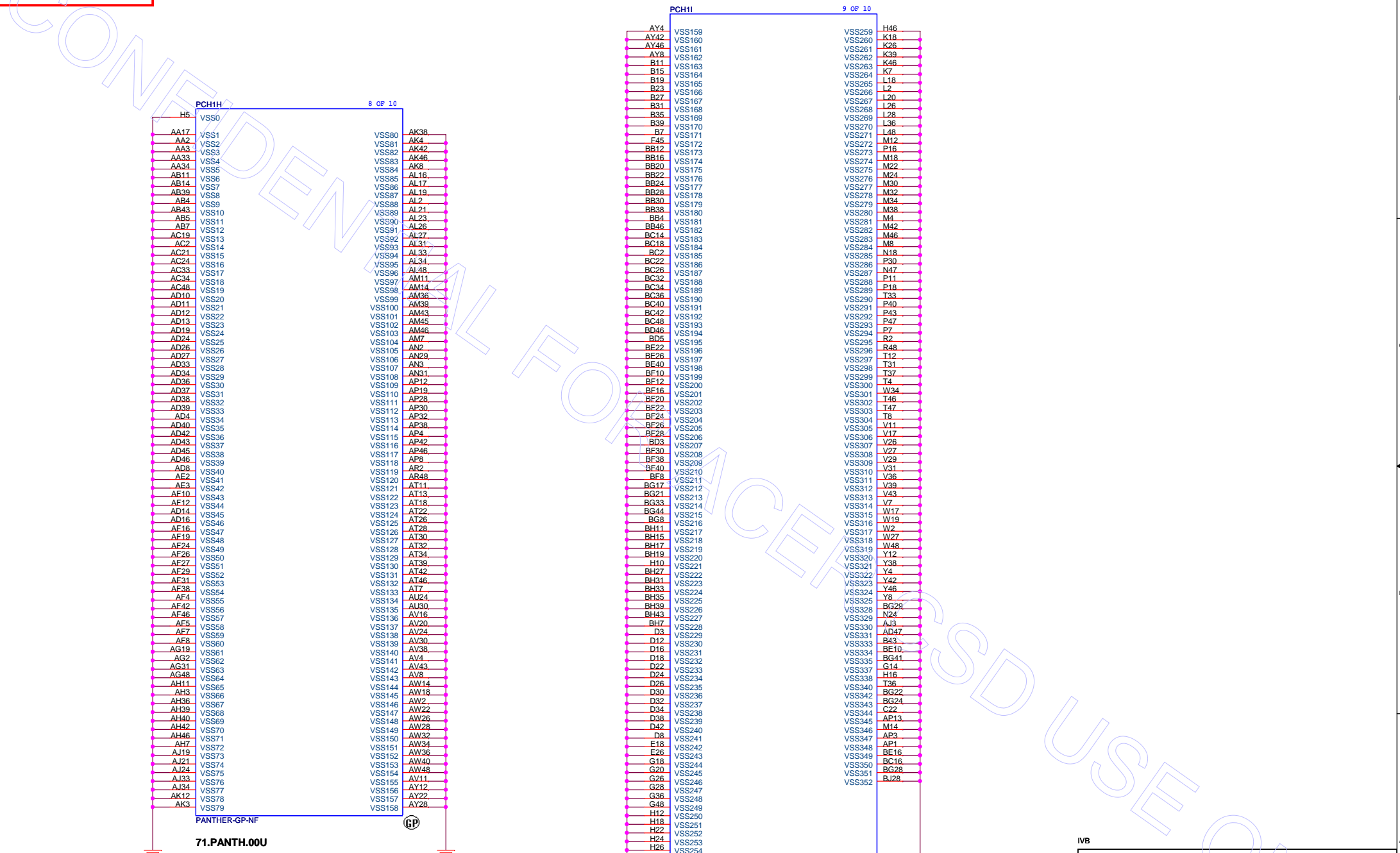
Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
V\$REF_SUS	VCC\$US3_3	a) VCC\$REF_SUS must be powered-up before VCC\$US3_3 or after VCC\$US3_3 within 0.7 V. b) If VCC\$REF_SUS is more than VCC\$US3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V\$REF_SUS must be powered down after VCC\$US3_3 or before VCC\$US3_3 within 0.7 V.
V\$REF	VCC3_3	a) V\$REF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC\$REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V\$REF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



SSID = PCH



<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title: PCH (VSS)</p>	
<p>Size A3</p>	<p>Document Number: Husk/Petra</p>
<p>Date: Thursday, April 19, 2012</p>	<p>Rev: -2</p>
<p>Sheet 25 of 103</p>	

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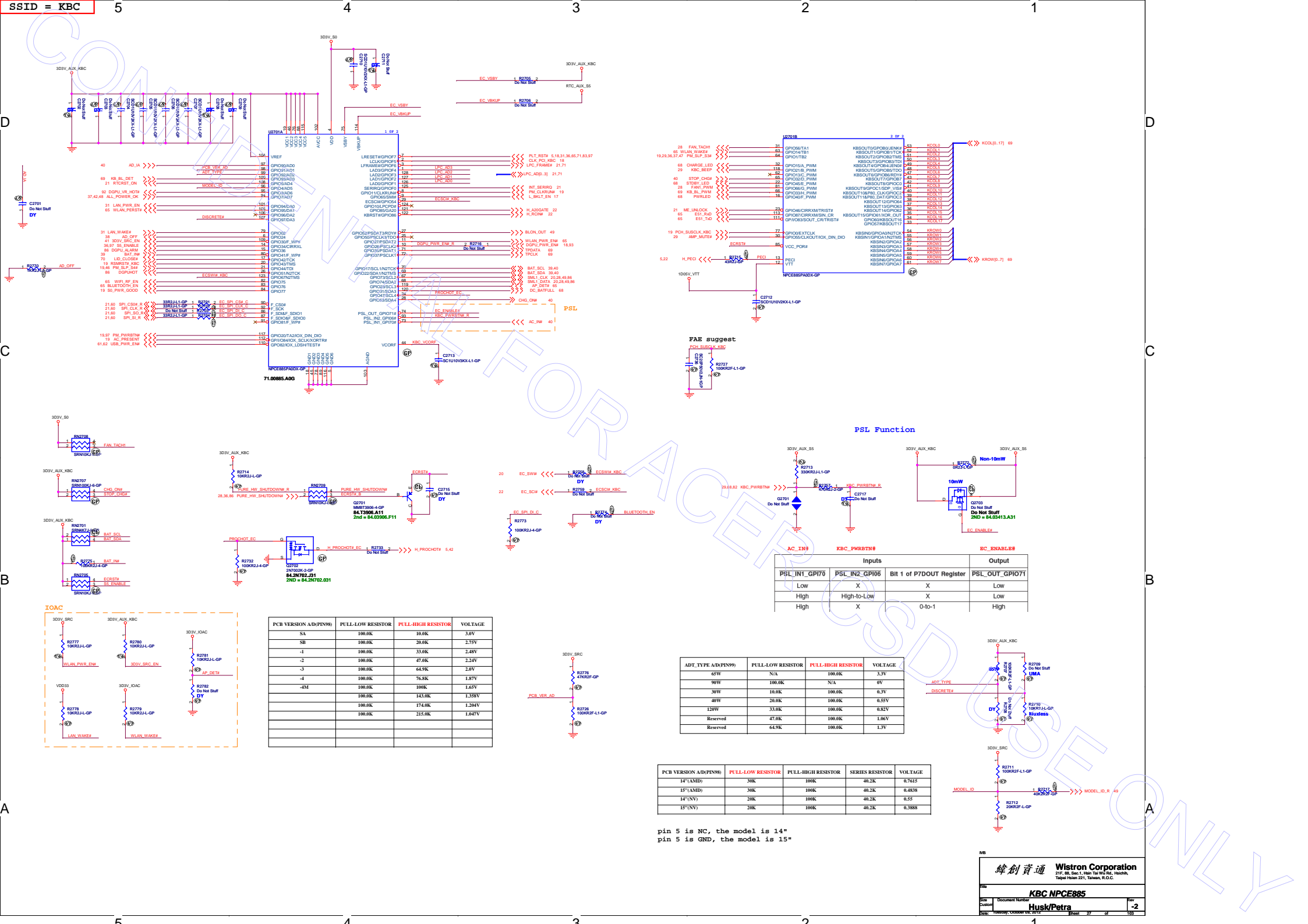
IVB

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Clock(colay)**

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012 Sheet 26 of 103



SSID = KBC

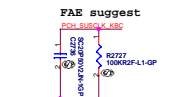
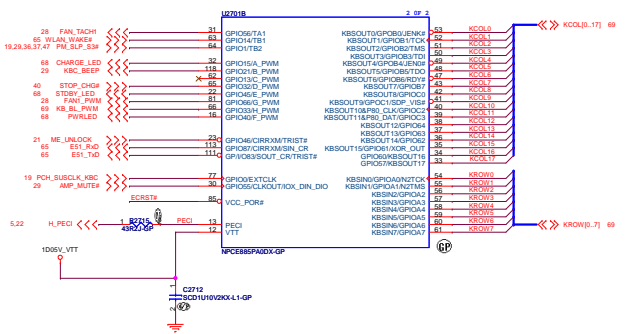
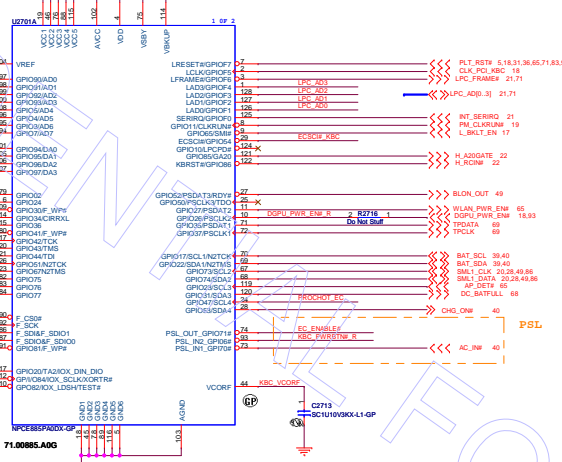
D

C

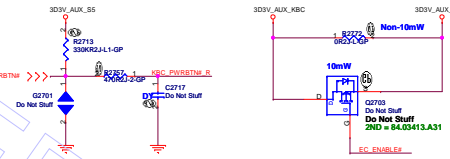
B

A

5



PSL Function



Inputs	Output
PSL_IN1_GPI70	PSL_OUT_GPI071
Low	Low
High	High-to-Low
High	0-to-1

PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
NB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.48V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V

ADT_TYPE A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65V	N/A	100.0K	3.3V
90V	100.0K	N/A	0V
30V	100.0K	100.0K	0.3V
40V	20.0K	100.0K	0.55V
120V	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	SERIES RESISTOR	VOLTAGE
14*(AMD)	30K	100K	40.2K	0.7615
15*(AMD)	30K	100K	40.2K	0.4838
14*(NV)	20K	100K	40.2K	0.55
15*(NV)	20K	100K	40.2K	0.3888

pin 5 is NC, the model is 14*
pin 5 is GND, the model is 15*

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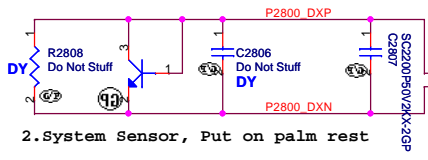
Doc No	KBC NPCE885	
Doc Name	Document Number	
Doc Date	2018/05/22	
Doc Rev	1	

SSID = Thermal

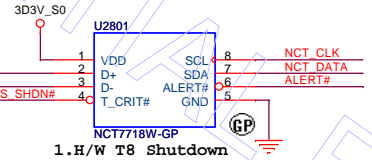
Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Q2801
PMBS3904-1-GP
84.03904.L06



2. System Sensor, Put on palm rest



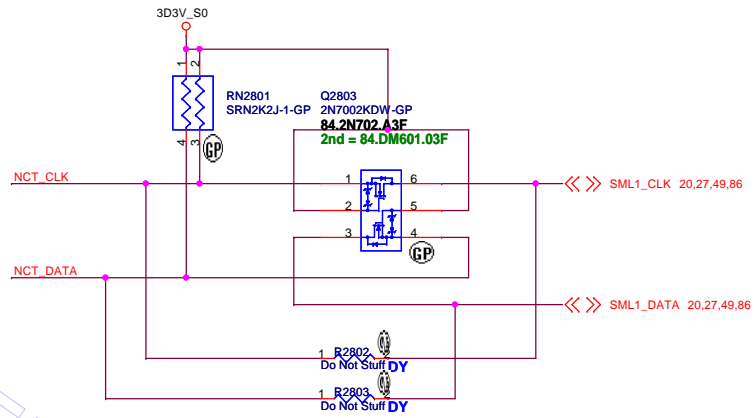
1.H/W T8 Shutdown

ALERT# /T CRIT#
Pull-up Resistor

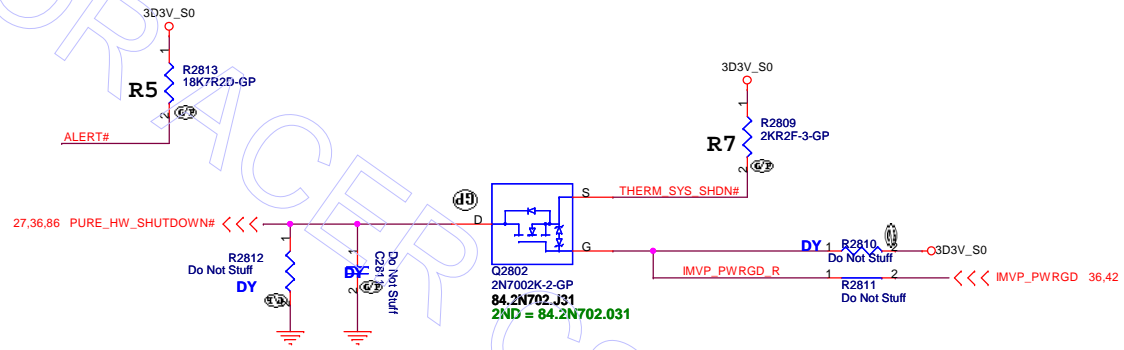
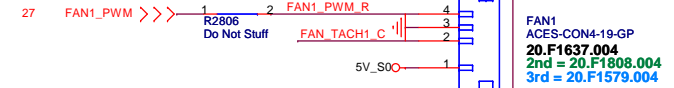
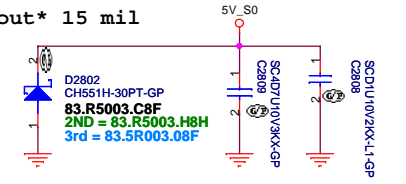
	R7					
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm	
R5	2Kohm	77°C	87°C	97°C	107°C	117°C
	7.5Kohm	79°C	89°C	99°C	109°C	119°C
	10.5Kohm	81°C	91°C	101°C	111°C	121°C
	14Kohm	83°C	93°C	103°C	113°C	123°C
	18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

SB T8=85 degree



Layout 15 mil



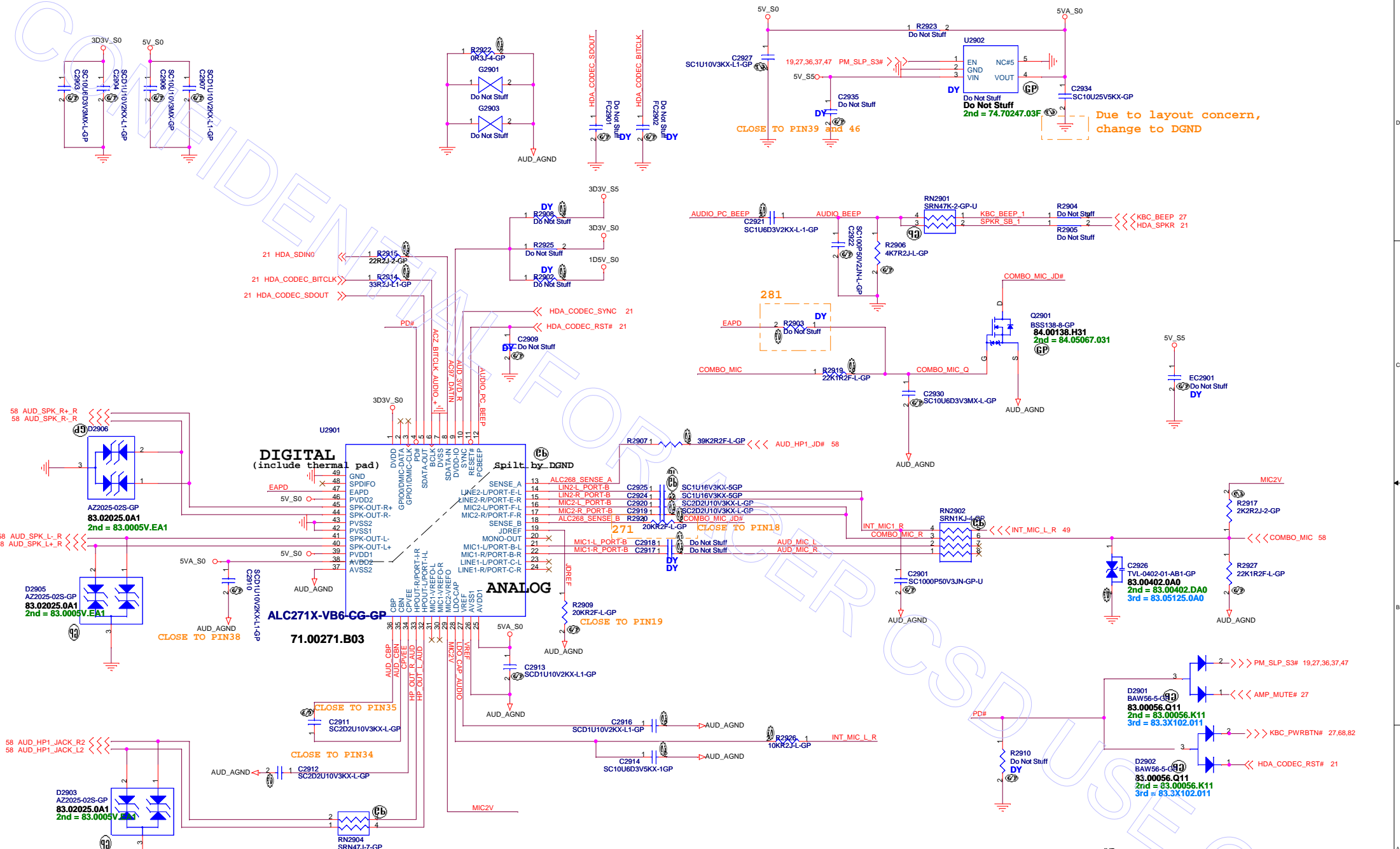
IVB

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Title: **Thermal NCT7718**

Size	Document Number	Rev
Custom	Husk/Petra	-2

Date: Tuesday, October 09, 2012 Sheet 28 of 103

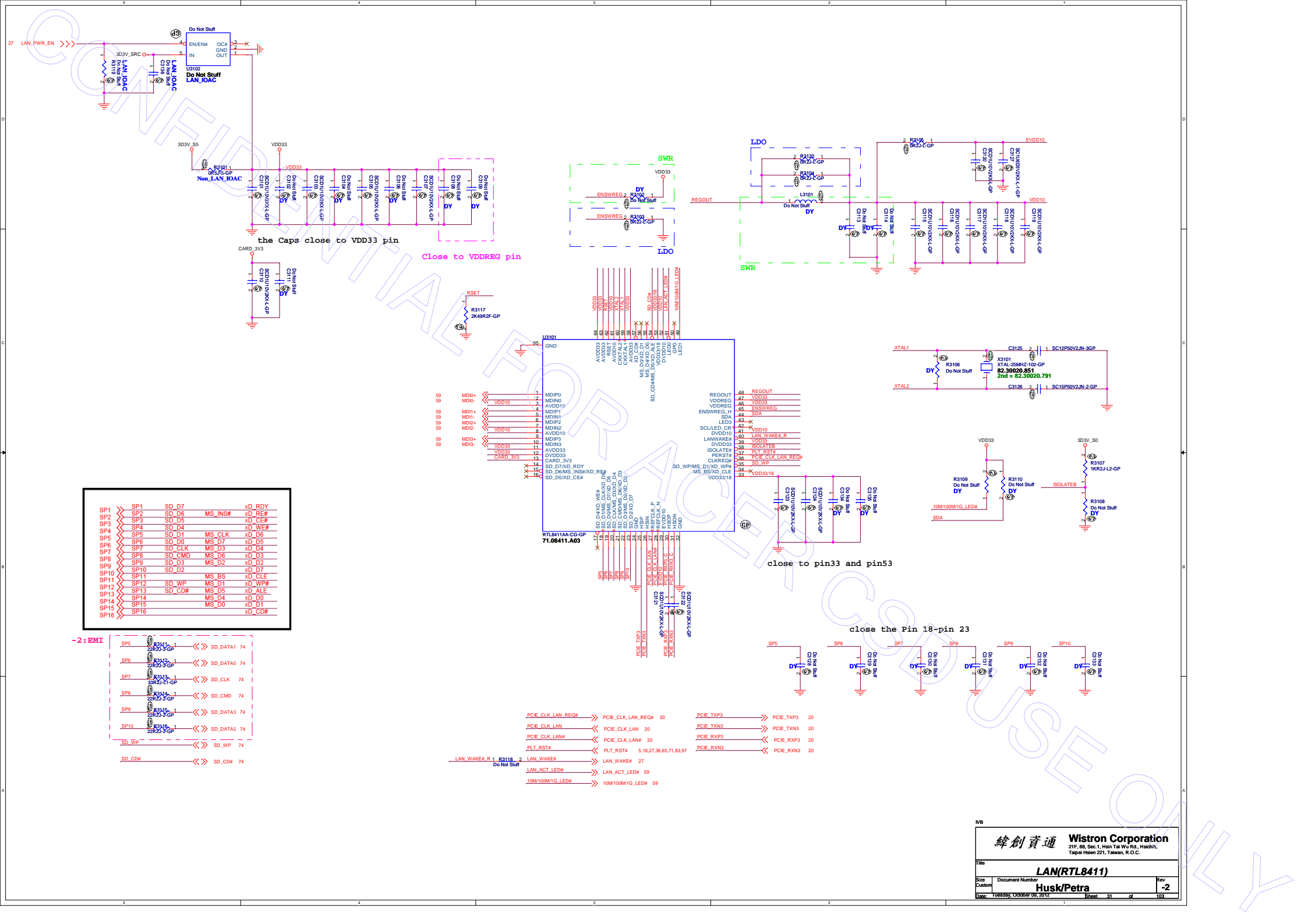


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Audio Codec		
Title	Husk/Petra	
Size	Document Number	Rev
Custom	-2	
Date:	Thursday, October 11, 2012	Sheet 29 of 103

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IVB

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Audio AMP			
Size A3	Document Number Husk/Petra	Rev -2	
Date: Thursday, April 19, 2012	Sheet 30	of 103	



the Caps close to VDD33 pin

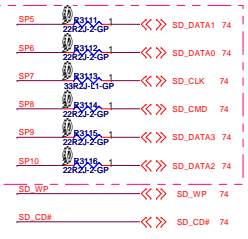
Close to VDDREG pin

close to pin33 and pin53

close the Pin 18-pin 23

SP1	SP1	SD D7	MS_INS#	xD_RDY
SP2	SP2	SD D6	MS_RE#	xD_RE#
SP3	SP3	SD D5	MS_CE#	xD_CE#
SP4	SP4	SD D4	MS_CLK	xD_WIE#
SP5	SP5	SD D3	MS_D6	xD_D6
SP6	SP6	SD D0	MS_D7	xD_D5
SP7	SP7	SD CLK	MS_D3	xD_D4
SP8	SP8	SD CMD	MS_D6	xD_D3
SP9	SP9	SD D3	MS_D2	xD_D2
SP10	SP10	SD D2	MS_D7	xD_D7
SP11	SP11	MS_BS	MS_CD#	xD_CD#
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D0	xD_D0
SP15	SP15	MS_D0	xD_D1	xD_D1
SP16	SP16	xD_CD#	xD_CD#	xD_CD#

-2: EMI



PCIE_CLK_LAN_REQ#	PCIE_CLK_LAN_REQ#	20	PCIE_TXP3	PCIE_TXP3	20
PCIE_CLK_LAN	PCIE_CLK_LAN	20	PCIE_TXN3	PCIE_TXN3	20
PCIE_CLK_LAN#	PCIE_CLK_LAN#	20	PCIE_RXP3	PCIE_RXP3	20
PLT_RST#	PLT_RST#	518,27,36,65,71,83,97	PCIE_RXN3	PCIE_RXN3	20
LAN_WAKE#	LAN_WAKE#	27			
LAN_ACT_LED#	LAN_ACT_LED#	59			
10M/100M/1G_LED#	10M/100M/1G_LED#	59			

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IVB	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RTS5159 (CARD READER)	
Size	Document Number
Custom	Husk/Petra
Date	Revision
Thursday, April 19, 2012	-2
Sheet	of
32	103

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IVB

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
Reserved		

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012	Sheet 33 of 103
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(Blanking)

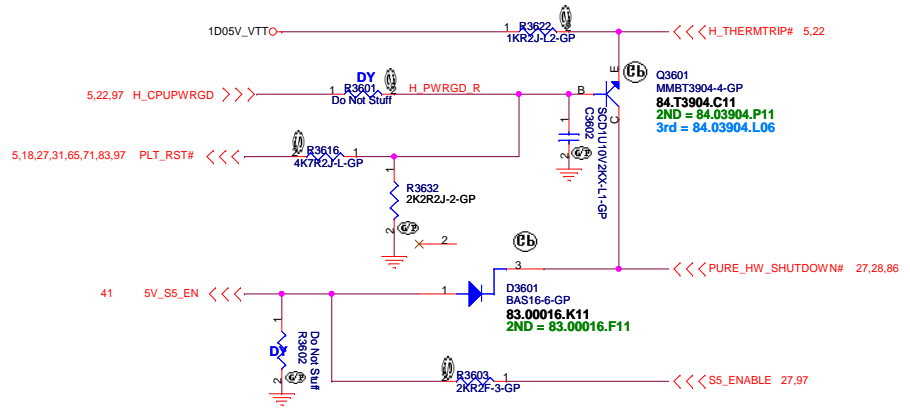
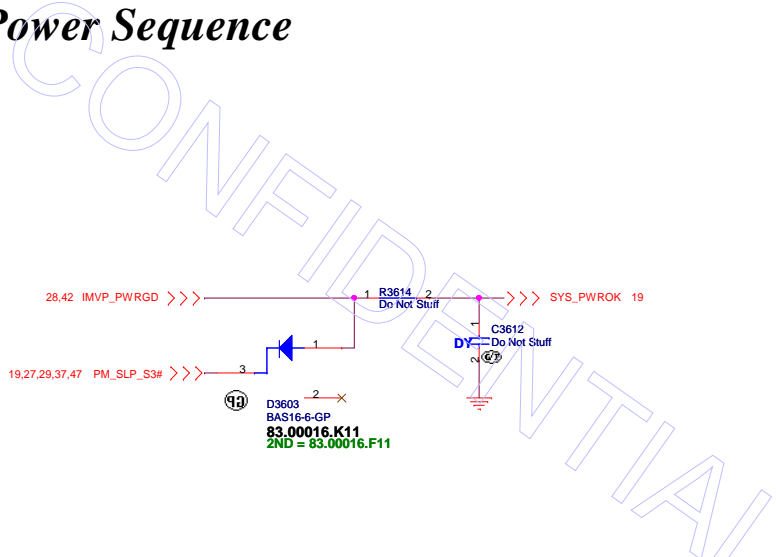
IVB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Reserved		
Size A4	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012		Sheet 34 of 103

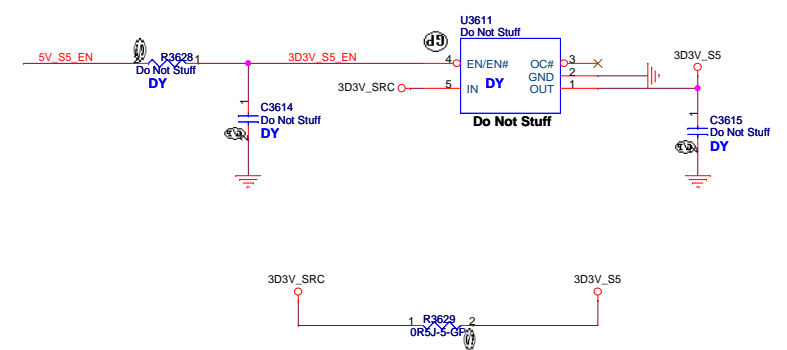
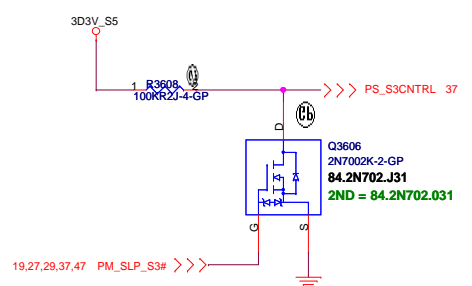
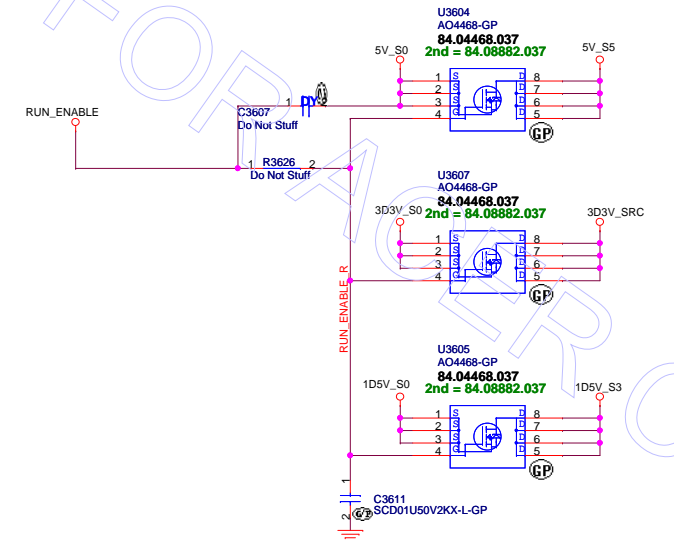
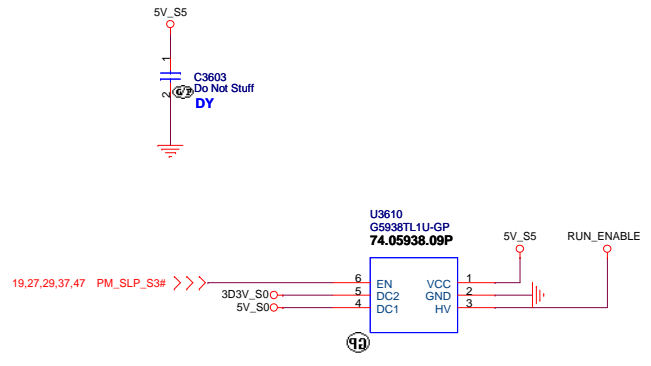
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IVB	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB 3.0 Controller	
Size	Document Number	Rev
Custom	Husk/Petra	-2
Date:	Thursday, April 19, 2012	Sheet 35 of 103

Power Sequence



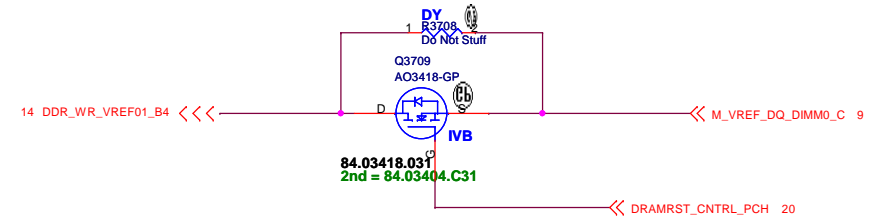
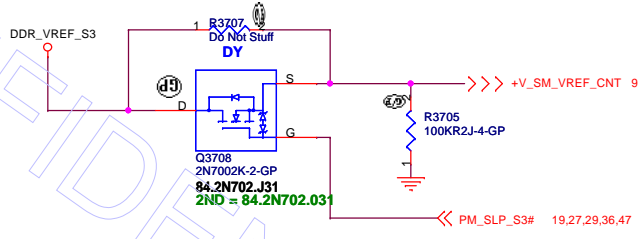
ANNIE Run Power



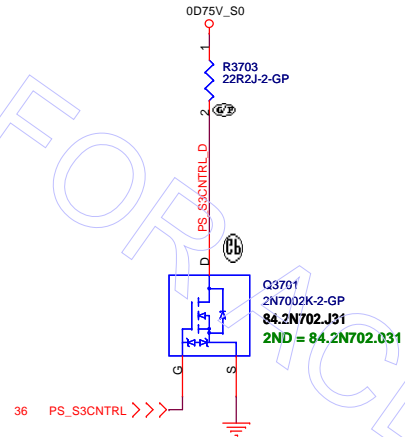
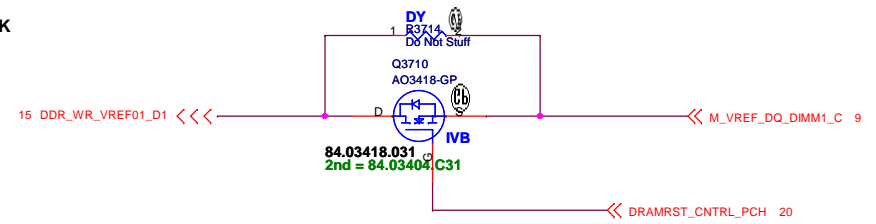
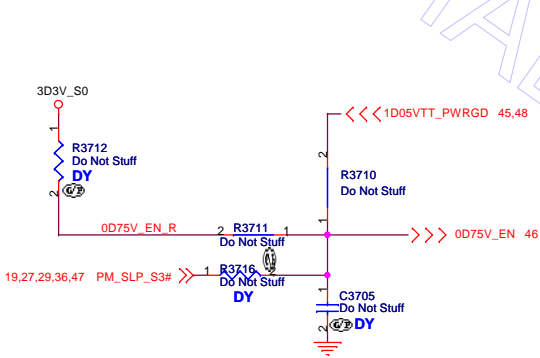
IVB

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power Plane Enable	
Size Custom	Document Number Husk/Petra
Date: Tuesday, October 09, 2012	Rev -2
Sheet 36 of 103	

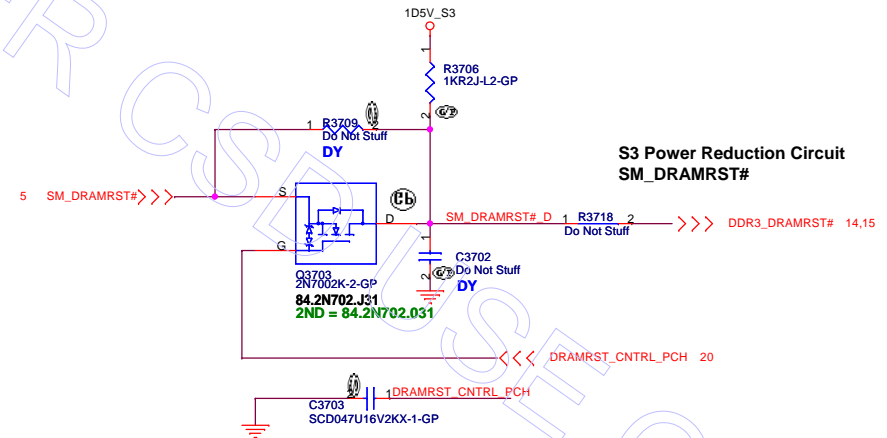
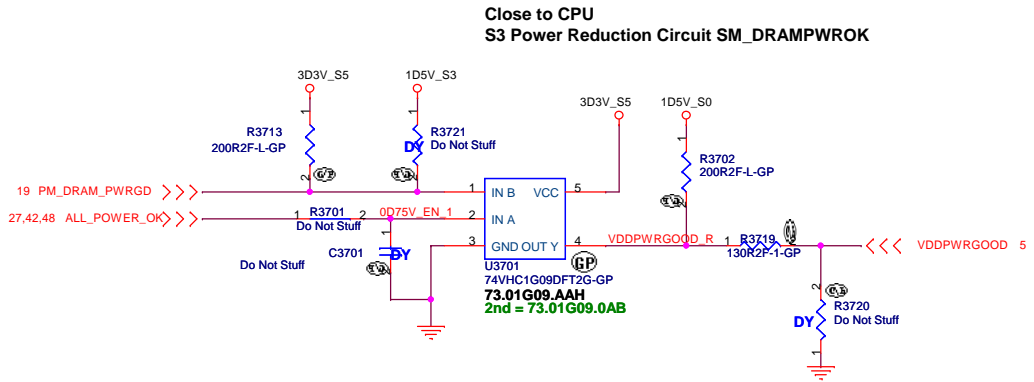
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



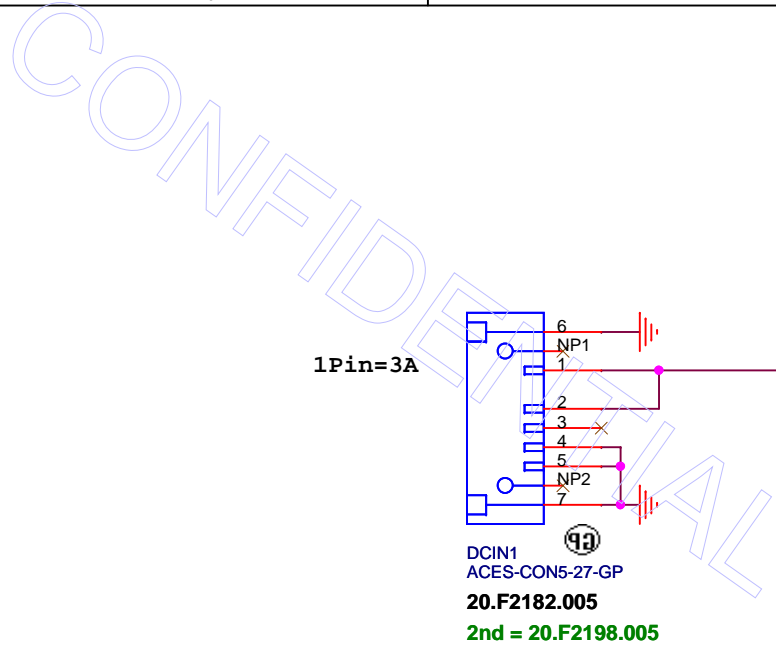
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ADAPTER	
Title Husk/Petra	Document Number -2
Date: Tuesday, October 09, 2012	Sheet 37 of 103



1Pin=3A

DCIN1
ACES-CON5-27-GP
20.F2182.005
2nd = 20.F2198.005

PC3801
SCD1U50V3KX-GP

D3801
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

PC3802
SC1U50V5ZY-1-GP

AD_JK

AD+

27

AD_OFF >>>

PQ3801
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR_ADJK_EN

PQ3802
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

PR3807
200KR2F-L-GP

PC3805
SC1U50V5ZY-1-GP

PR3808
100KR2J-4-GP

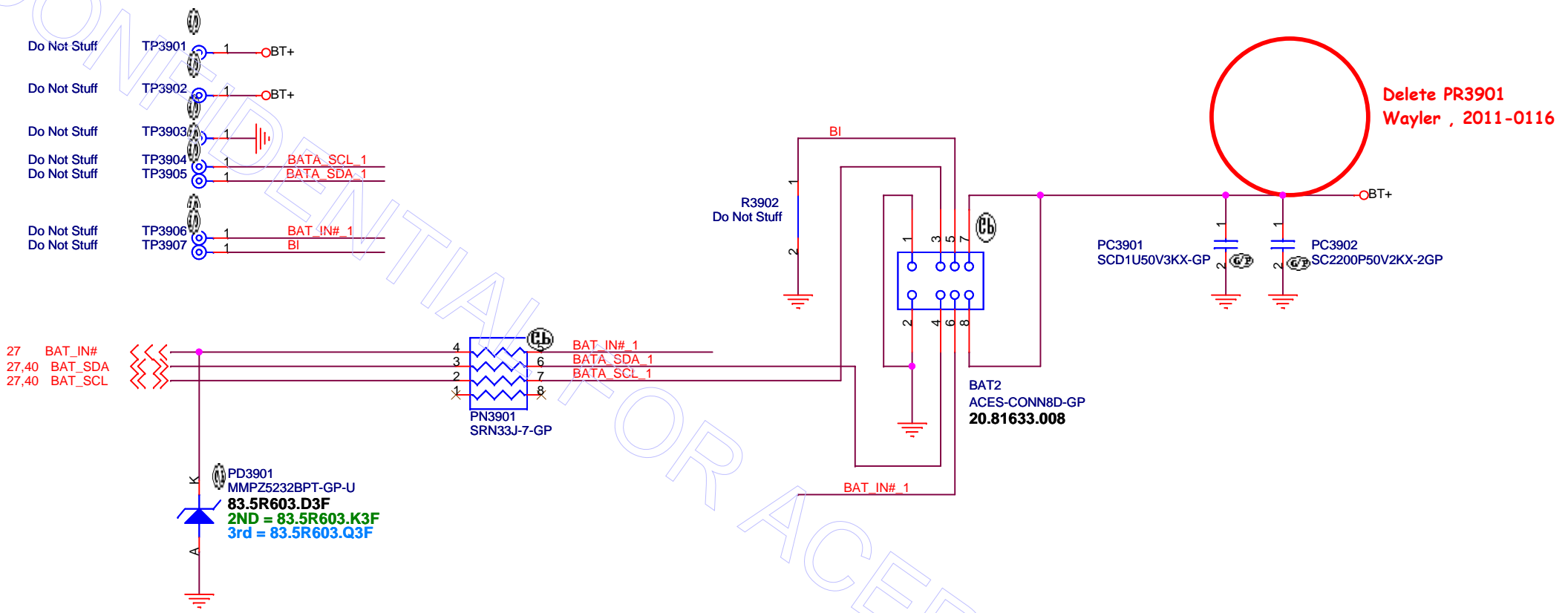
PU3802
P1403EV8-GP
84.P1403.B37
2nd = 84.04407.F37
3rd = 84.03005.037

PWR_AD+_2

IVB

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DCIN JACK			
Size A4	Document Number Husk/Petra		Rev -2
Date: Thursday, June 14, 2012	Sheet 38	of	103

BATTERY CONNECTOR

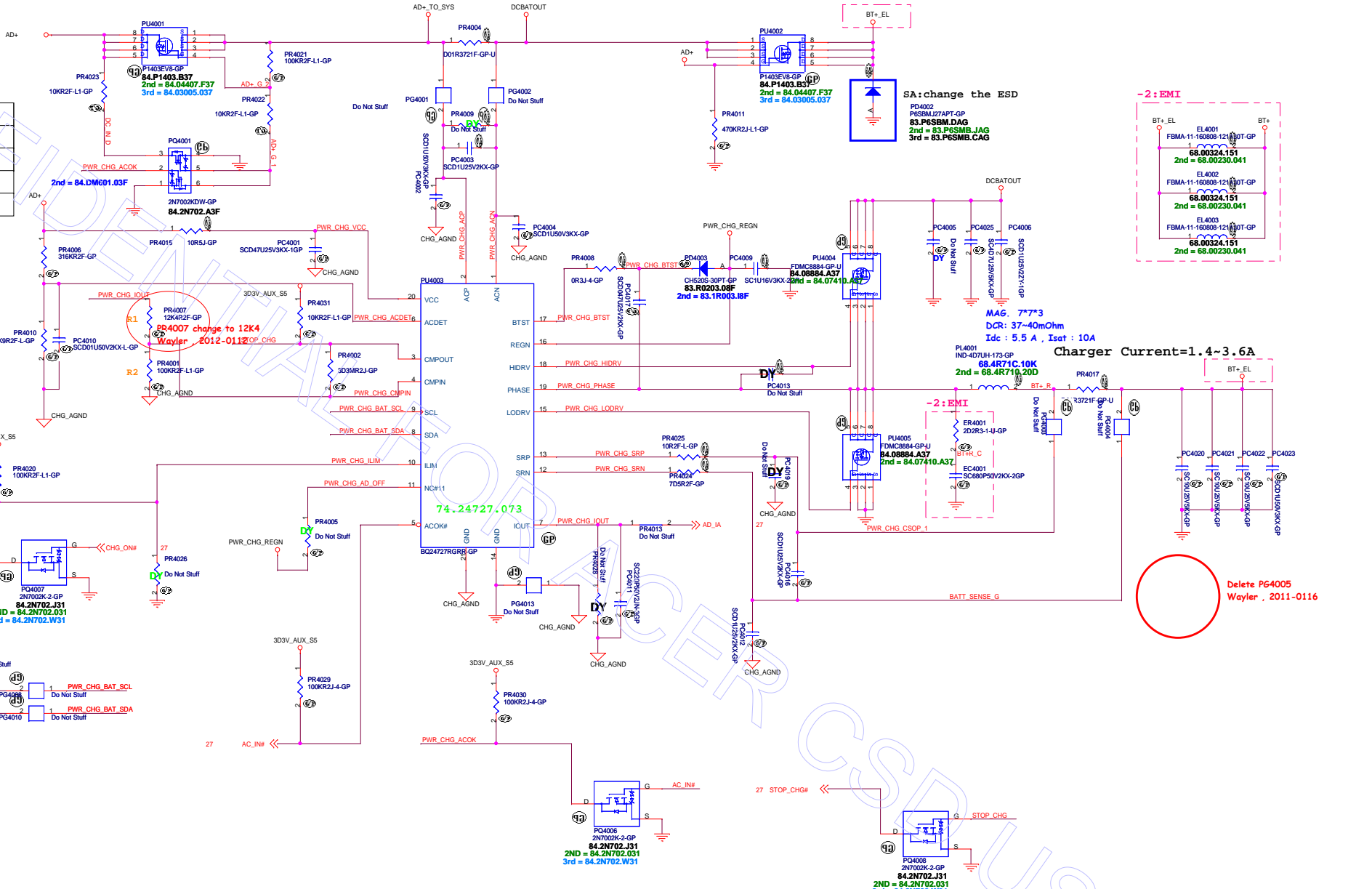


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BATT CONN			
Size A4	Document Number Husk/Petra		Rev -2
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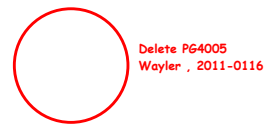
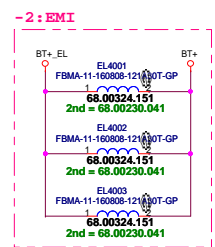
SSID = Charger

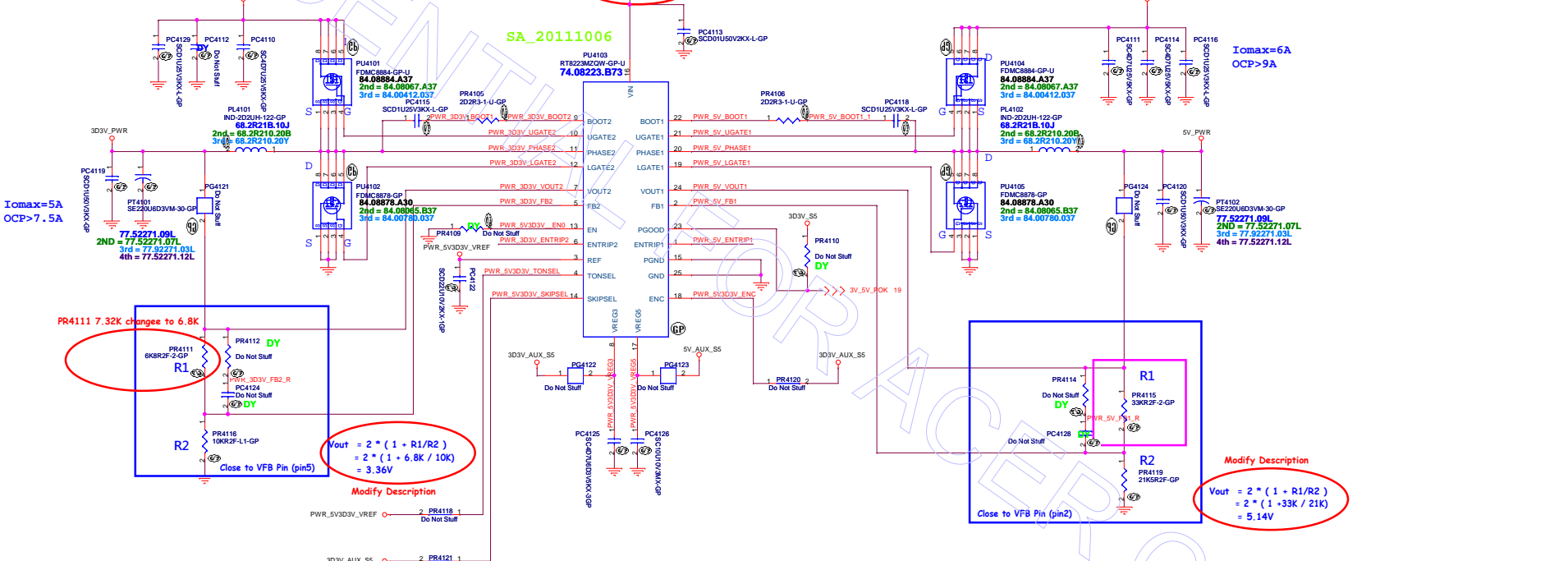
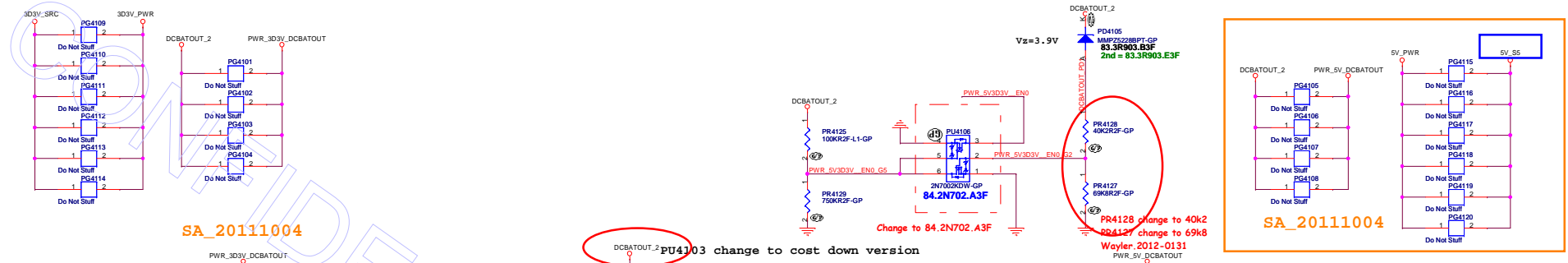
A8 (ANNIE/ASTRO)
PR4014, PR4016

AD+ total power	R1	R2
65w	1.2.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	1.18k	100K



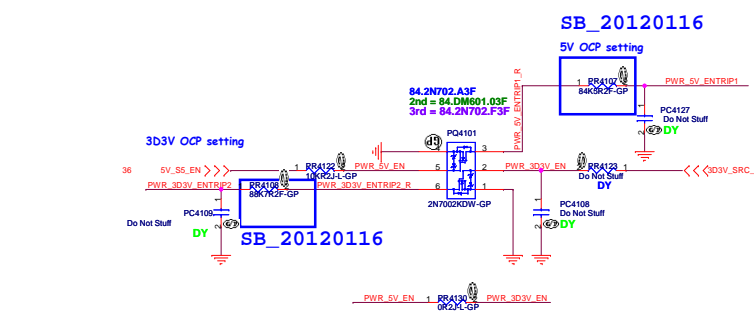
MAG: 777*3
DCR: 37-40mOhm
I_{dc}: 5.5 A, I_{sat}: 10A
Charger Current = 1.4~3.6A



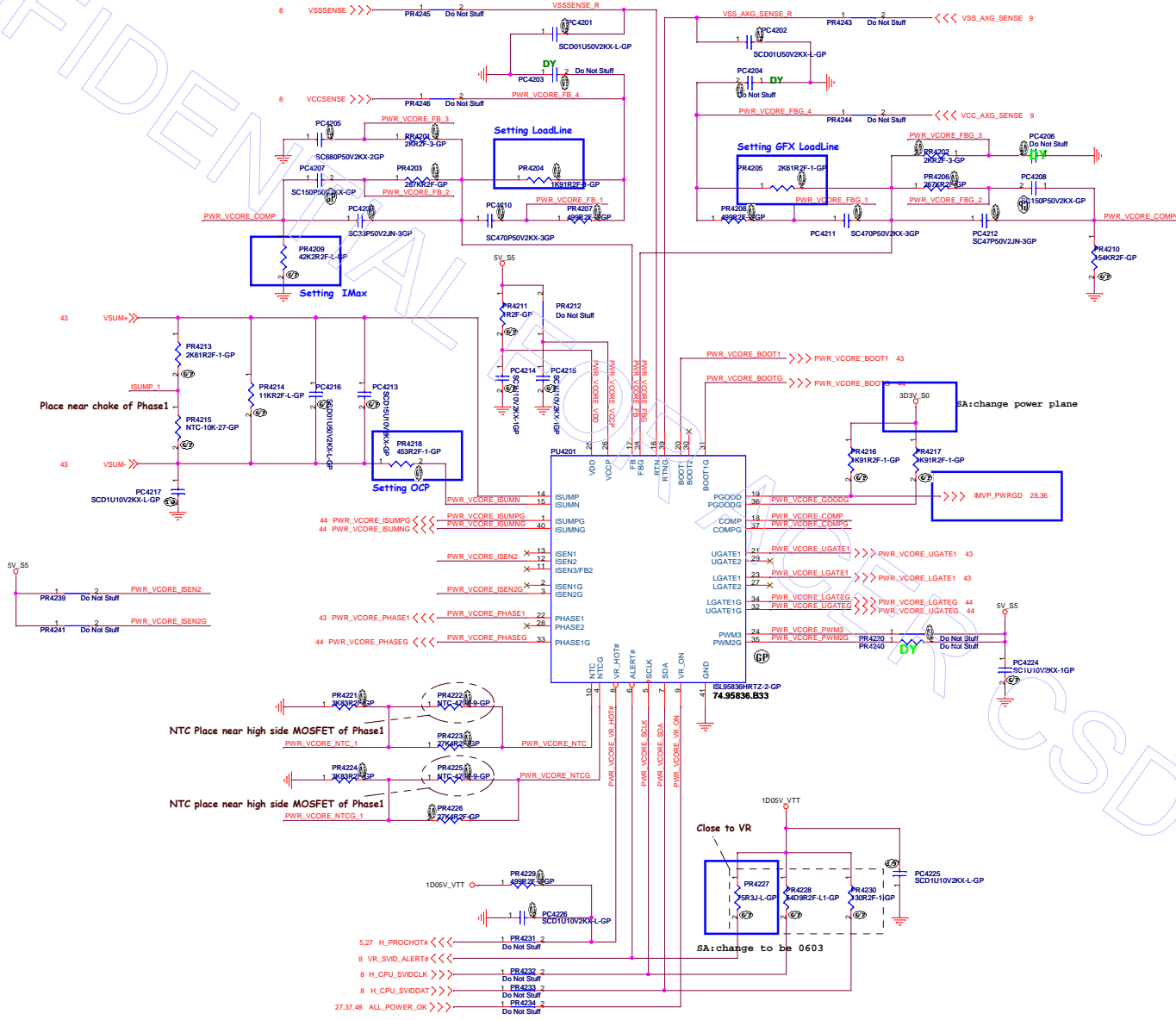


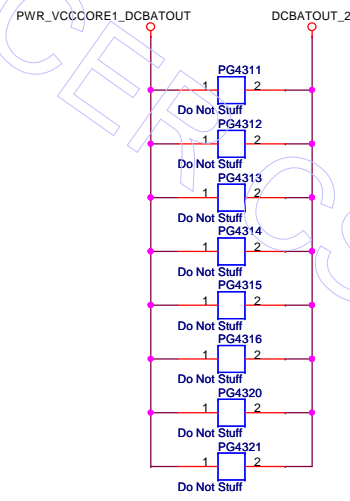
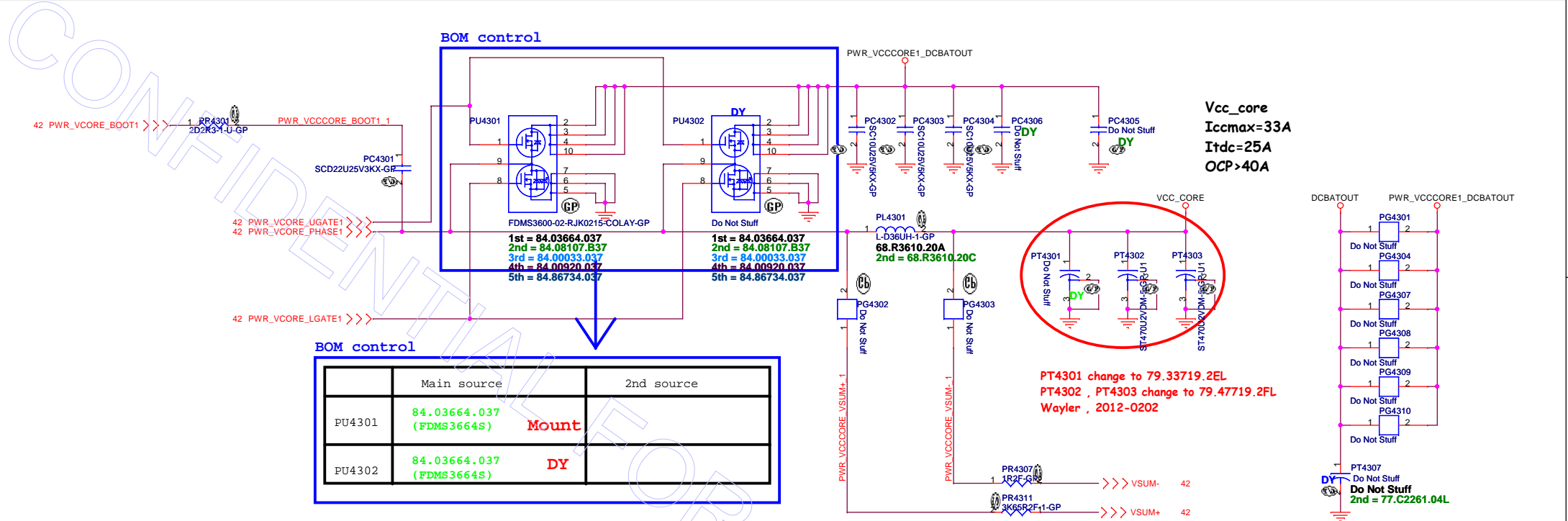
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VRBG3 or VRBG5	400kHz	500kHz

SKIPSEL	VRBG3 or VRBG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

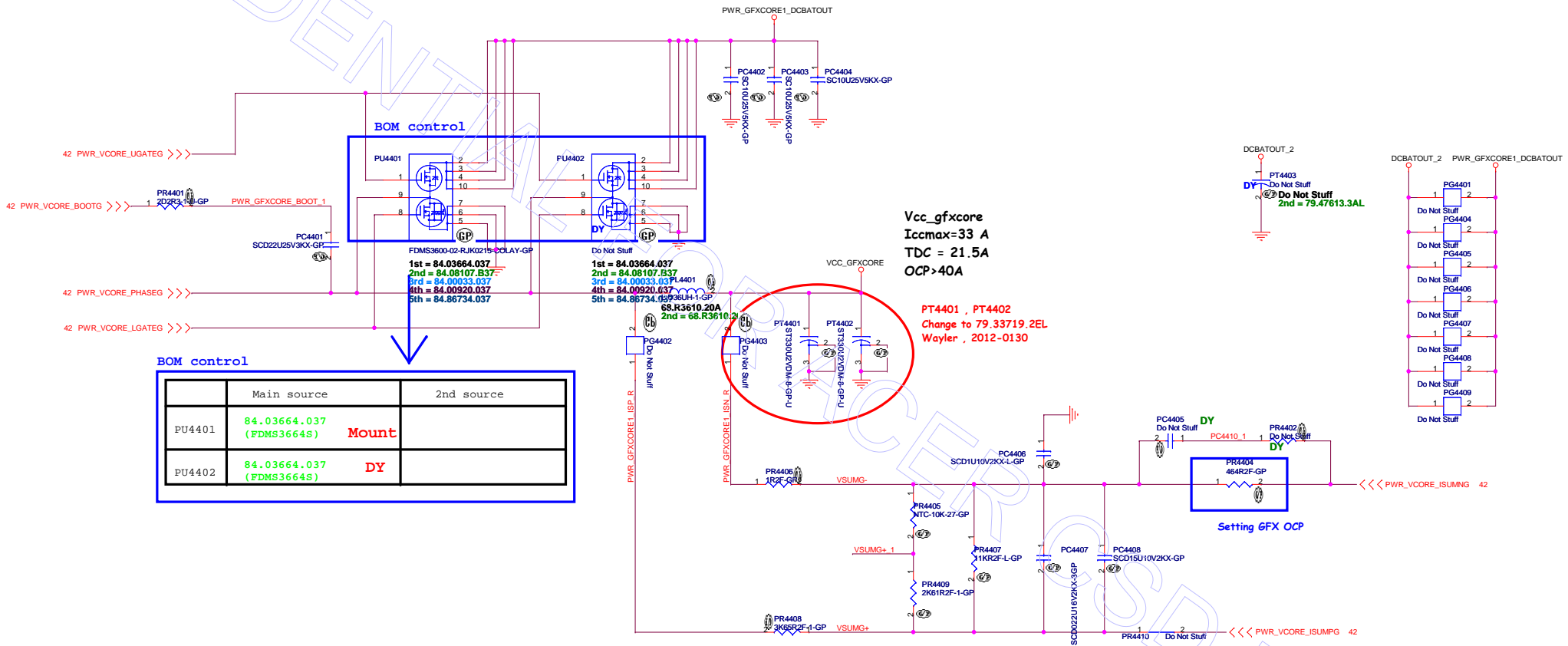


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Vcc_gfxcore
 Iccmax=33 A
 TDC = 21.5A
 OCP>40A

PT4401 , PT4402
 Change to 79.33719.2EL
 Wayler , 2012-0130

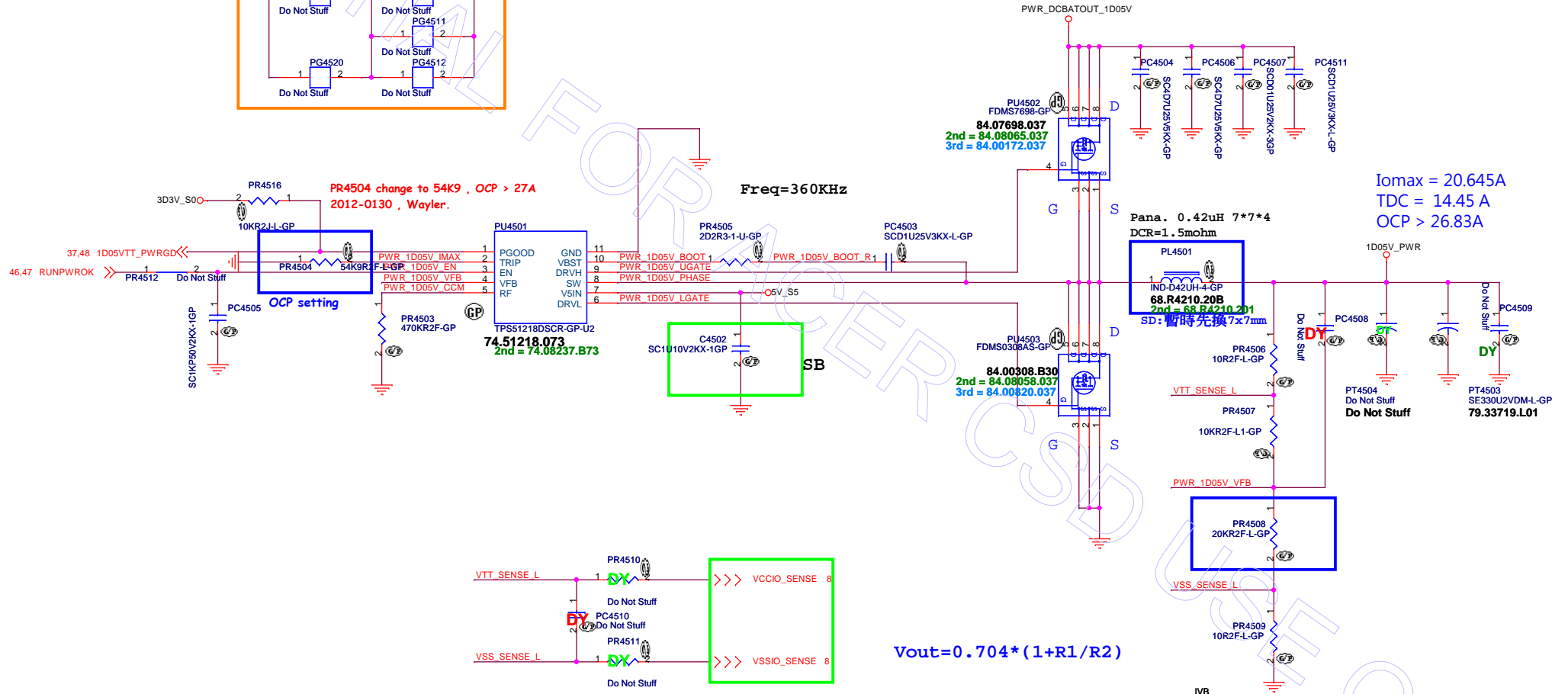
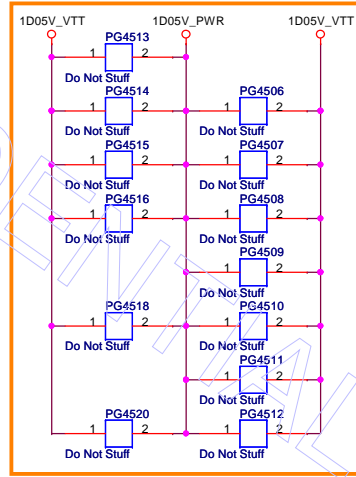
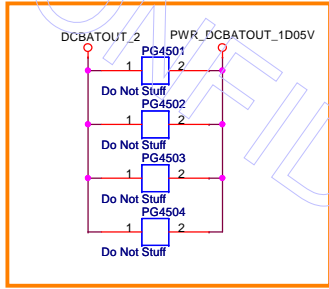
BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S)	Mount
PU4402	84.03664.037 (FDMS3664S)	DY

SA_20111004

SA_20111013

TPS51218D for 1D05V



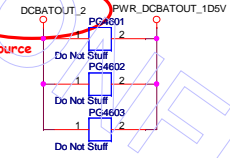
PR4504 change to 54K9 , OCP > 27A
2012-0130 , Wayer.

OCP setting

$$V_{out} = 0.704 * (1 + R1/R2)$$

SSID = PWR.Plane.Regulator_lp5v0p75v

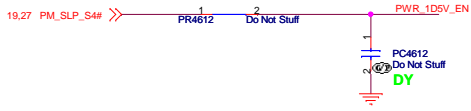
Change power source



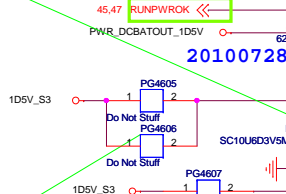
SA 20111004

SC:delete PT4601

RT8207L for 1D5V



Close to pin23



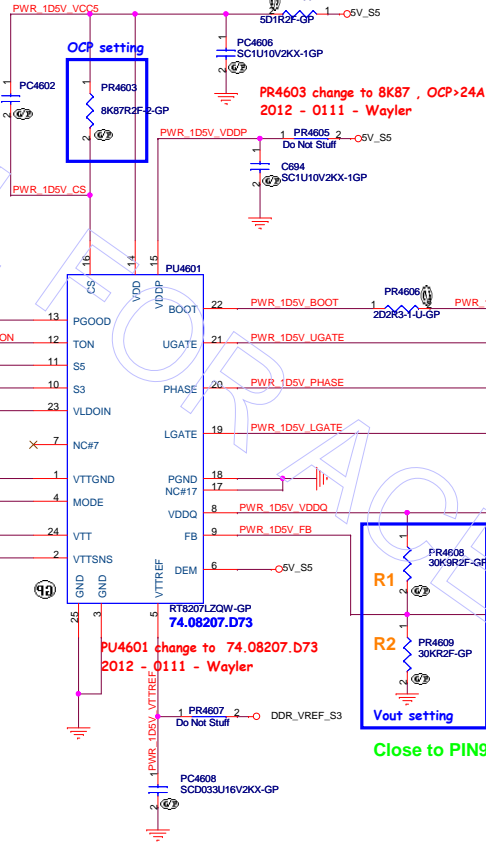
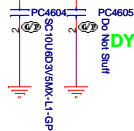
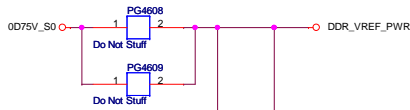
20100728

Close to pin23

I_{omax}=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

+0.75VS
I_{omax}: 1.2A



OCP setting

PR4603 change to 8K87, OCP>24A
2012 - 0111 - Waylor

Close to pin9

Close to pin9

Vout setting

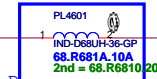
PR4608 change to 30.9K
2012 - 0111 - Waylor

PWR_DCBATOUT_1D5V



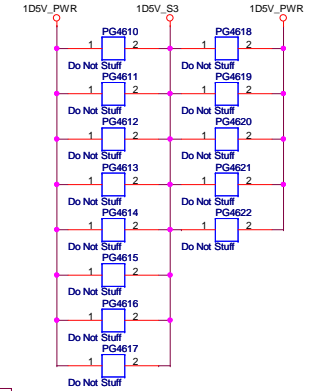
CYNTREC. 0.68uH 7*7*3
DCR= 5 - 5.5 mohm
I_{dc}=15.5A, I_{sat}=25A

I_{ccMAX} = 18.38A
I_{ccTDC} = 12.86A
OCP > 23.89A



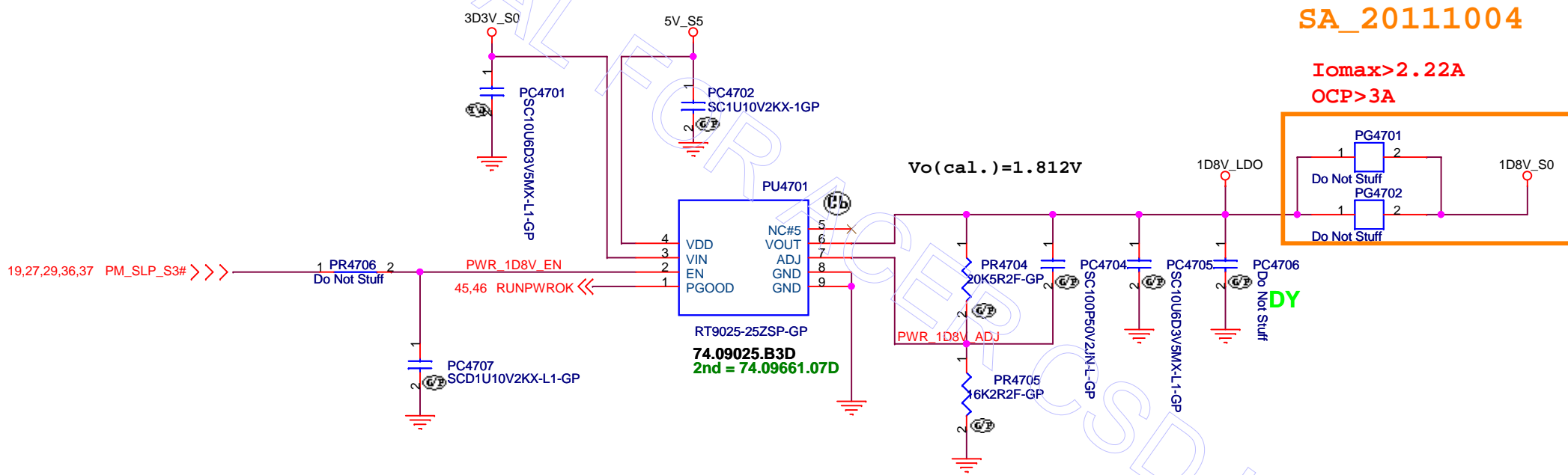
SD: 暫時先換 7x7mm
PL4603 IND-D30U4336-GP
84.00308.B30
2nd = 84.08058.037
3rd = 84.00820.037

$V_{out} = 0.75 * (1 + R1/R2)$



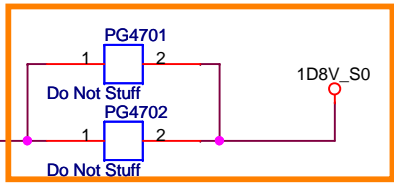
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



SA_20111004

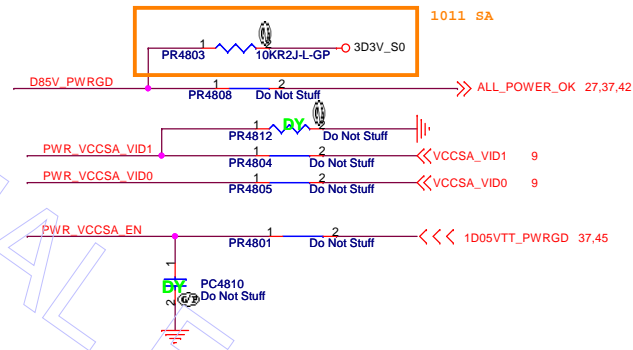
Iomax > 2.22A
OCP > 3A



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Title			
LDO 1D8V(RT9025)			
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LDO G978 for VCCSA



D0, D1 V₀ Selection Table

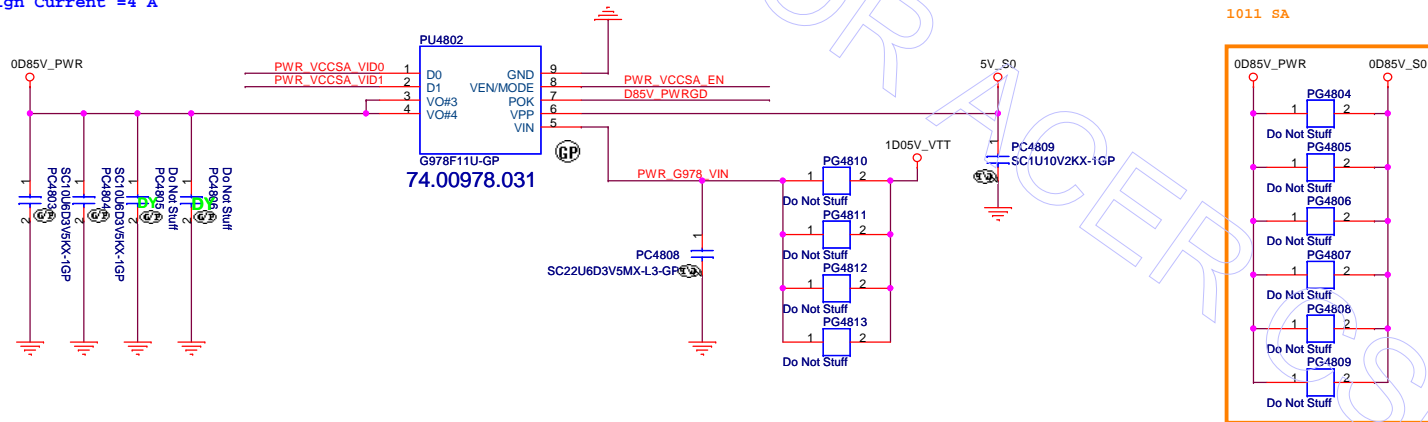
D0	D1	V ₀ MODE=0	V ₀ MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

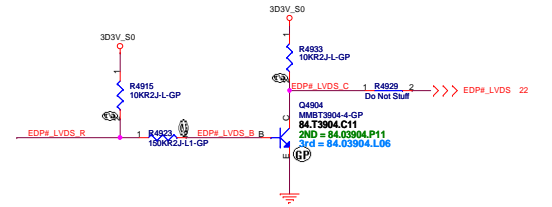
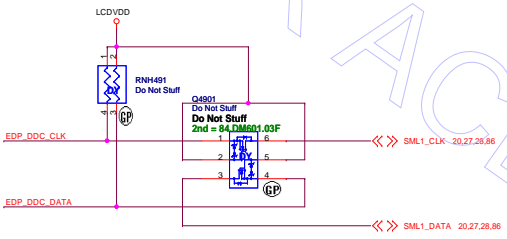
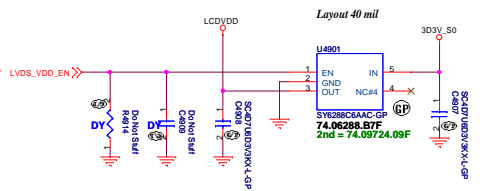
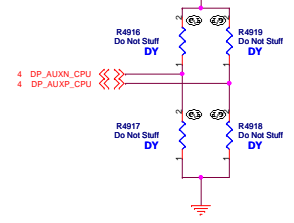
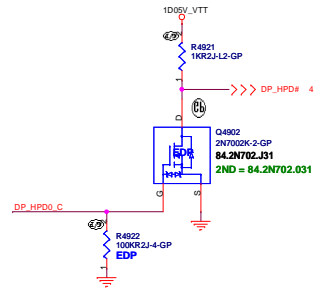
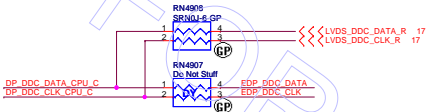
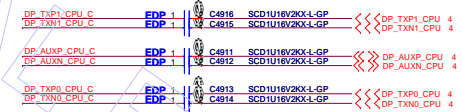
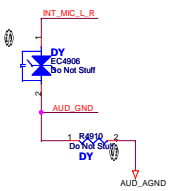
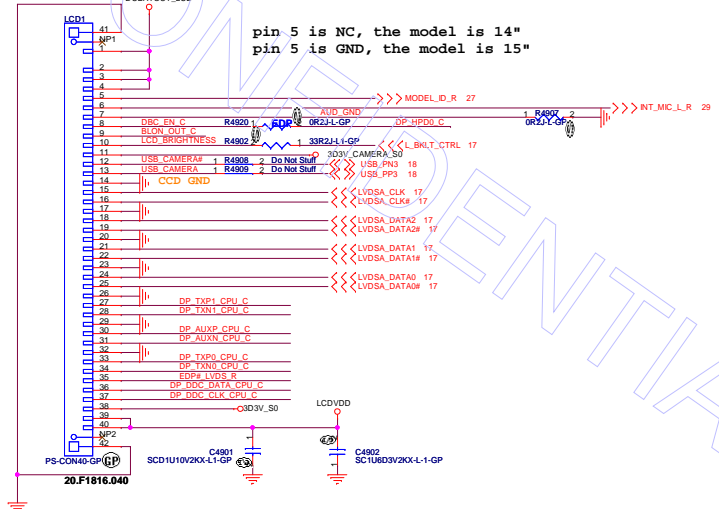
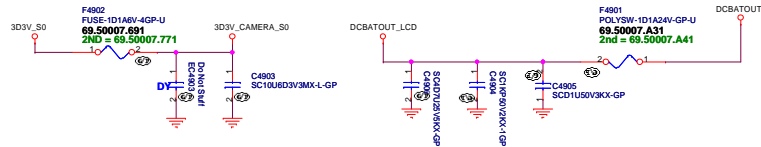
Design Current = 4 A



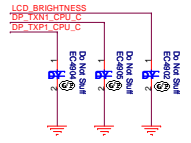
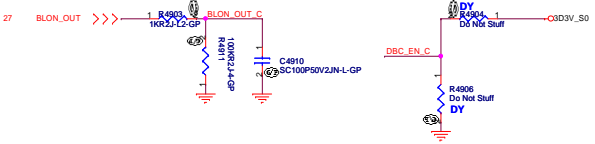
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Title VCCSA LDO G978			
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pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"

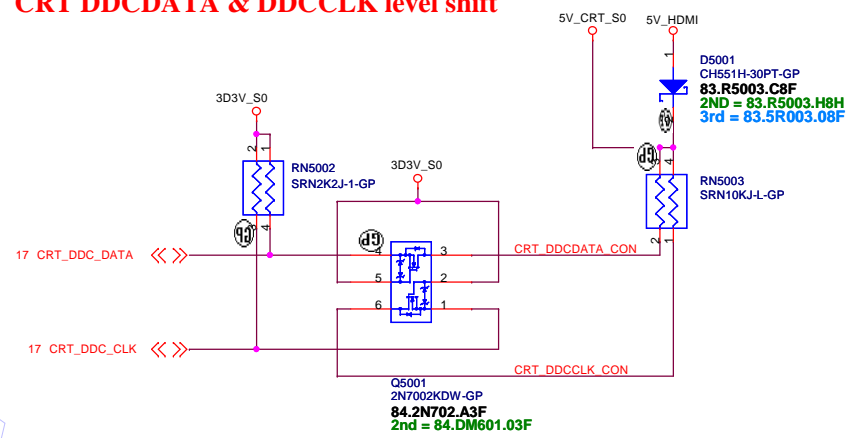
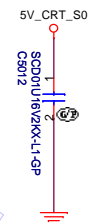


EDP: pin35 NC
LVDS: pin35 GND

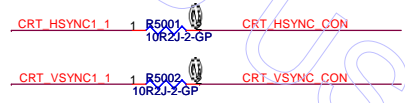
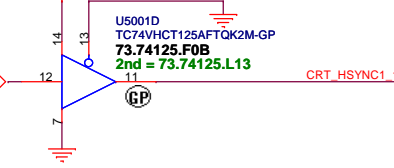
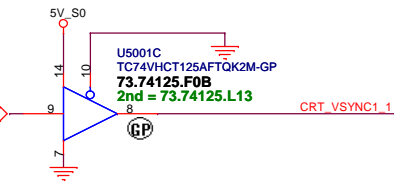
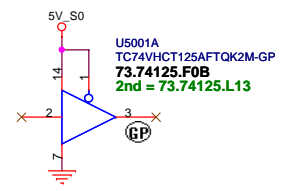
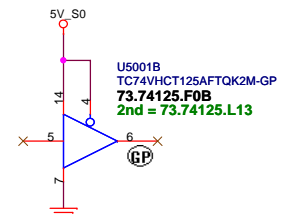
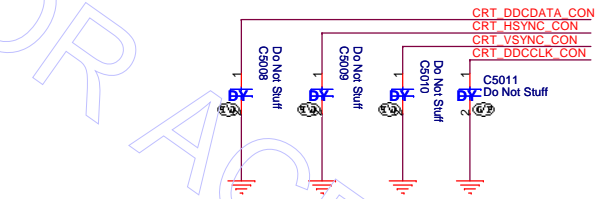
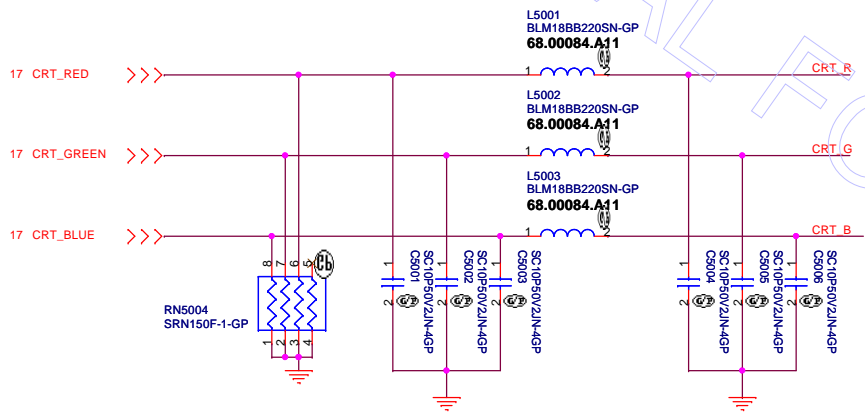


CRT DDCDATA & DDCLK level shift

- CRT_DDCDATA_CON >>> CRT_DDCDATA_CON 59
- CRT_DDCLK_CON >>> CRT_DDCLK_CON 59
- CRT_R >>> CRT_R 59
- CRT_G >>> CRT_G 59
- CRT_B >>> CRT_B 59
- CRT_HSYNC_CON >>> CRT_HSYNC_CON 59
- CRT_VSYNC_CON >>> CRT_VSYNC_CON 59



- D5001 CH551H-30PT-GP
- 83.R5003.C8F
- 2ND = 83.R5003.H8H
- 3rd = 83.SR003.08F



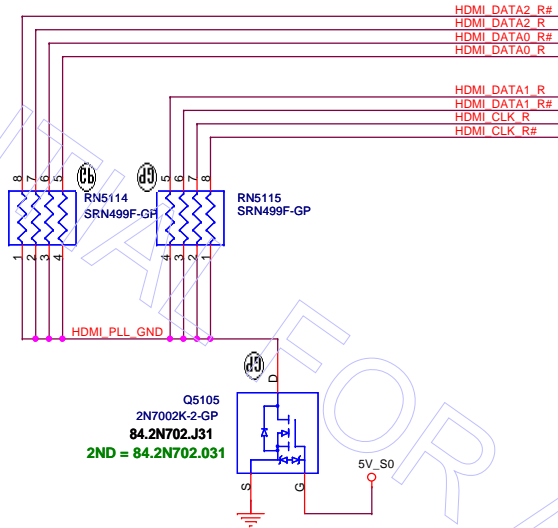
SSID = VIDEO HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

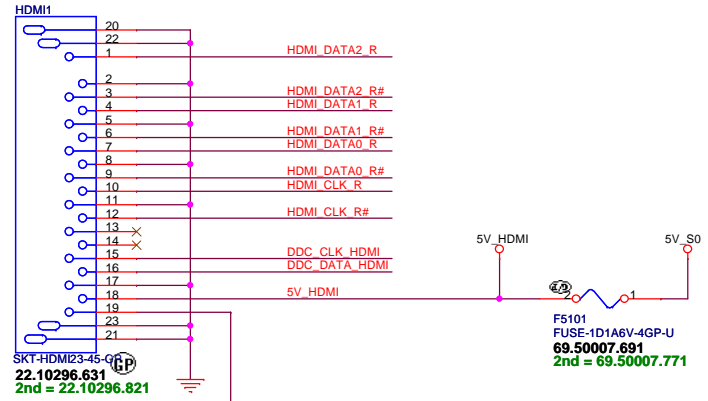
change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

17 HDMI_CLK_R# >>>
17 HDMI_CLK_R >>>
17 HDMI_DATA0_R# >>>
17 HDMI_DATA0_R >>>

17 HDMI_DATA1_R# >>>
17 HDMI_DATA1_R >>>
17 HDMI_DATA2_R# >>>
17 HDMI_DATA2_R >>>

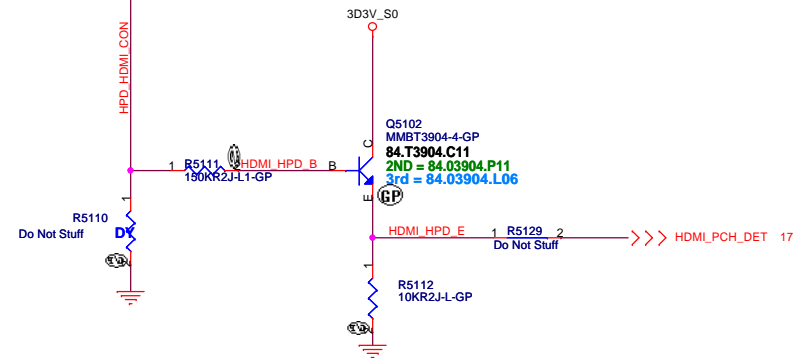


Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031



SKT-HDMI23-45-GP
22.10296.631
2nd = 22.10296.821

F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771



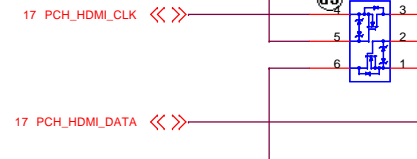
R5110
Do Not Stuff

Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06

R5112
10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F



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Title		eDP	
Size A3	Document Number	Rev	
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Taipei Hsien 221, Taiwan, R.O.C.

Title **S-VIDEO**

Size A4 Document Number **Husk/Petra** Rev **-2**

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Taipei Hsien 221, Taiwan, R.O.C.

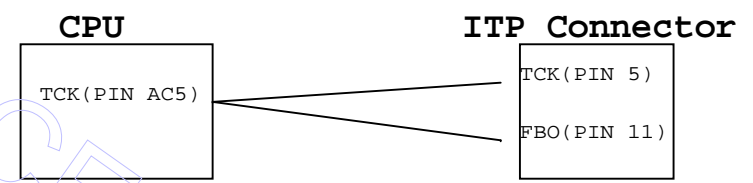
Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

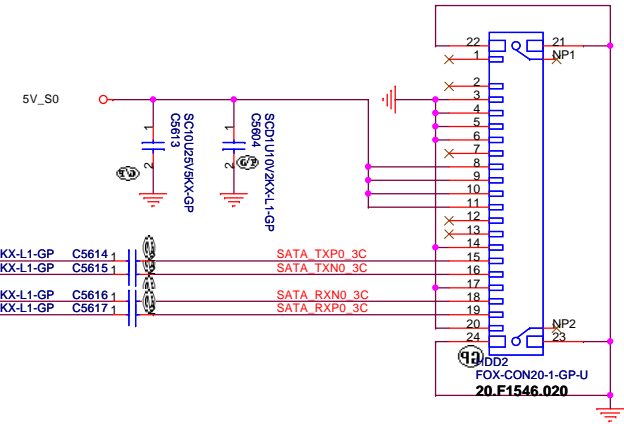
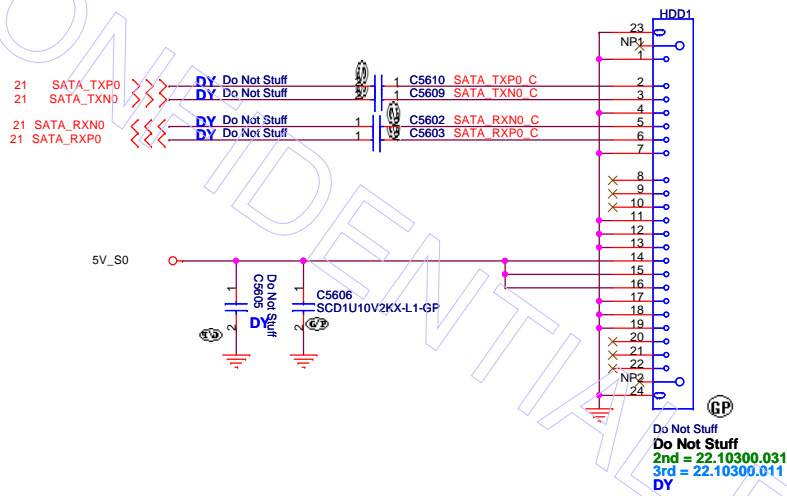


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Title			
ITP			
Size	Document Number		Rev
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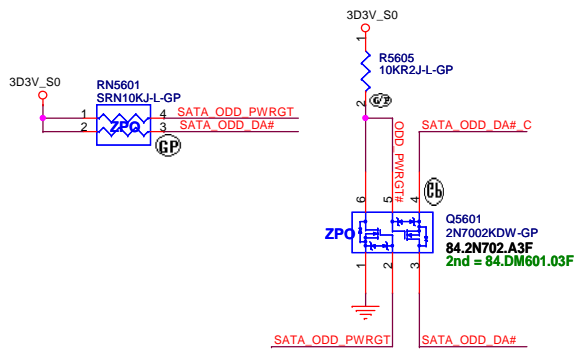
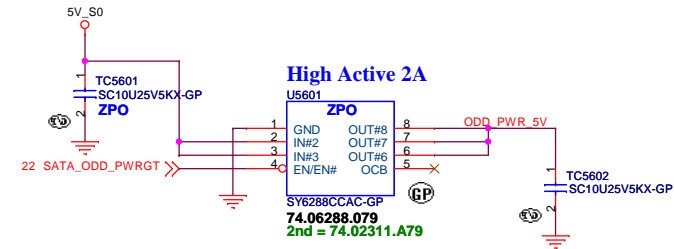
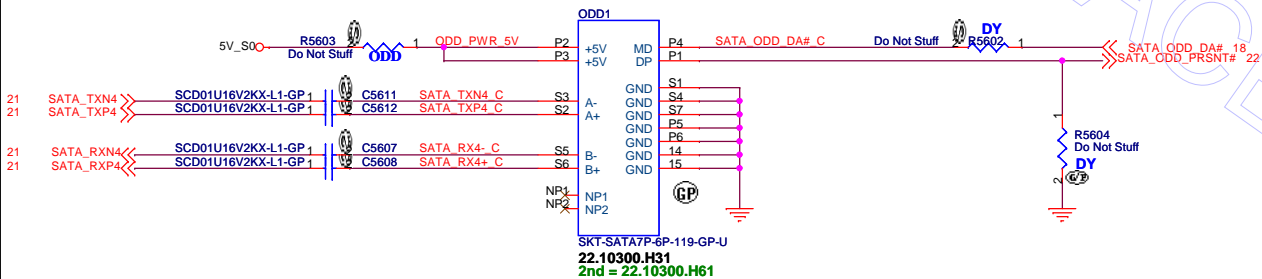
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD

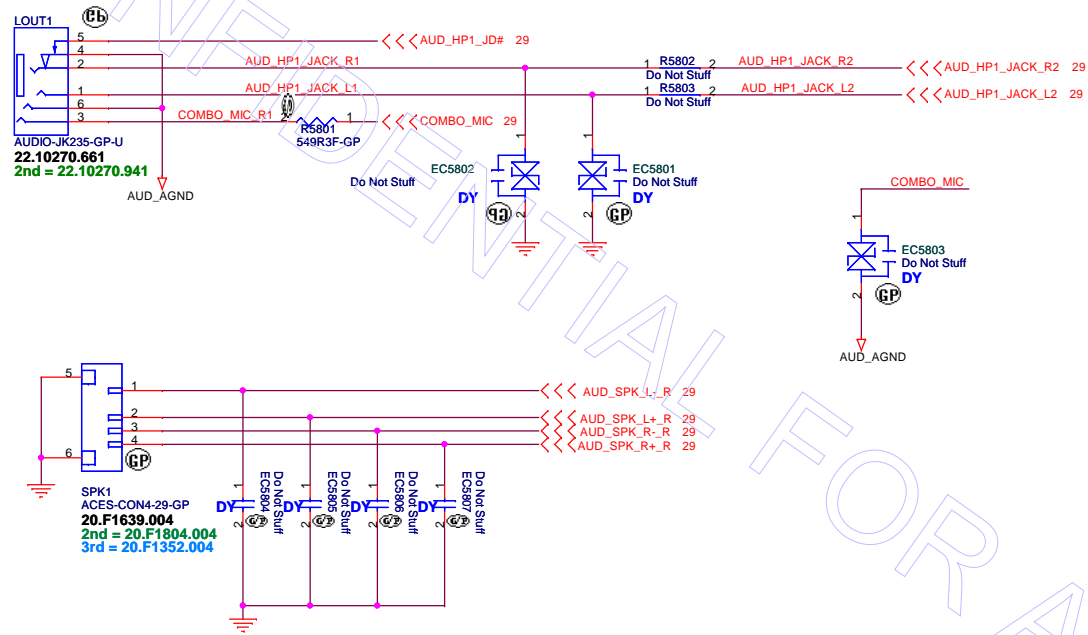


IVB

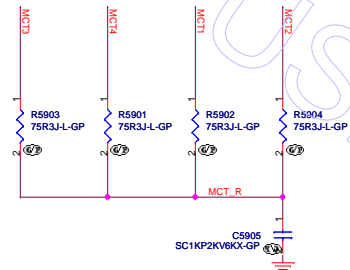
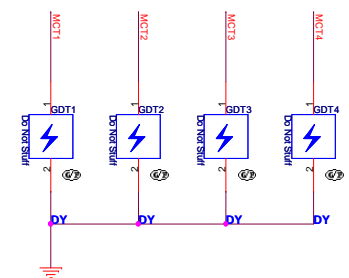
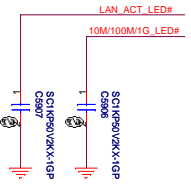
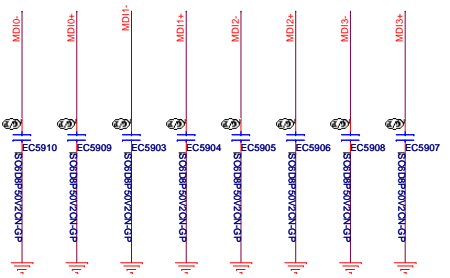
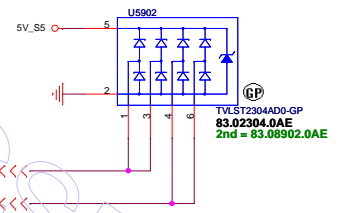
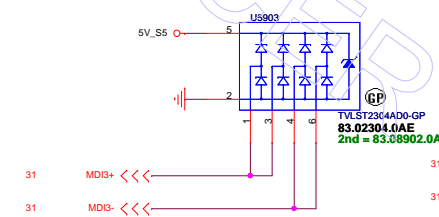
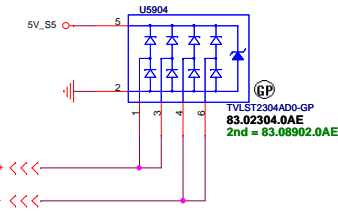
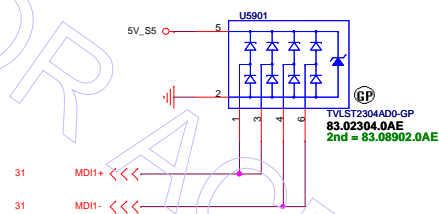
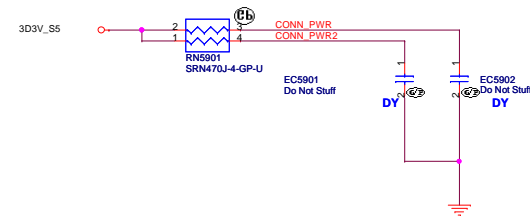
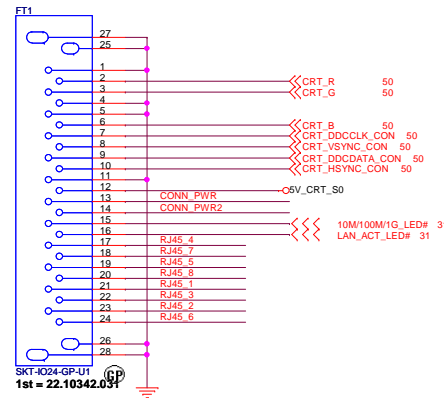
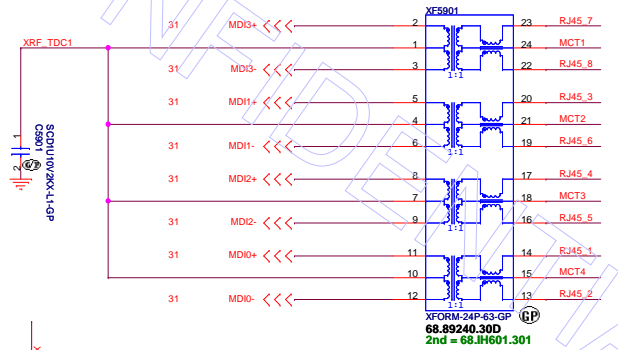
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IVB		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title E-SATA/USB CHARGER		
Size A3	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012	Sheet 57	of 103

SSID = AUDIO

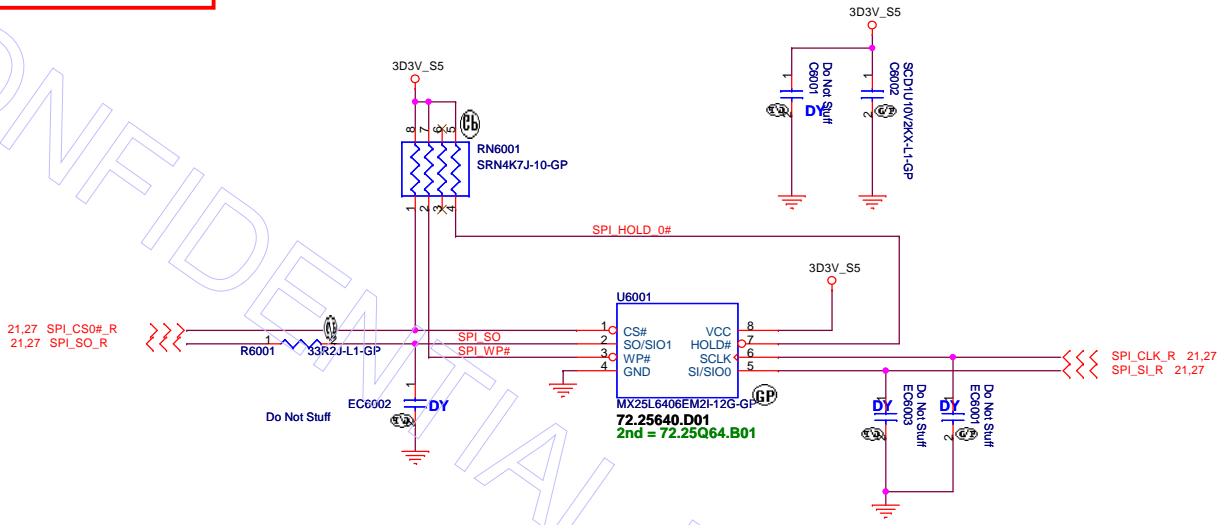


SSID = LAN

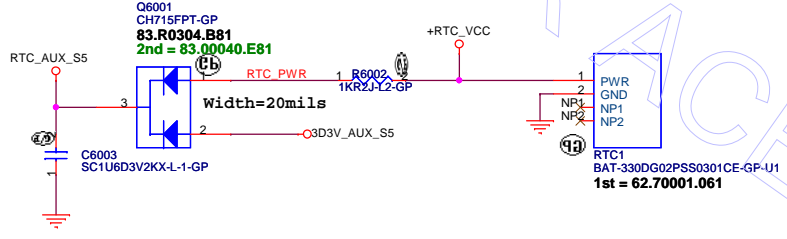


緯創資通 Wistron Corporation
 21F, 68, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LAN CONNECTOR
 Title: _____ Size: Custom Document Number: _____ Rev: -2
 Date: Monday, November 12, 2012 Sheet: 59 of 103

SSID = Flash.ROM



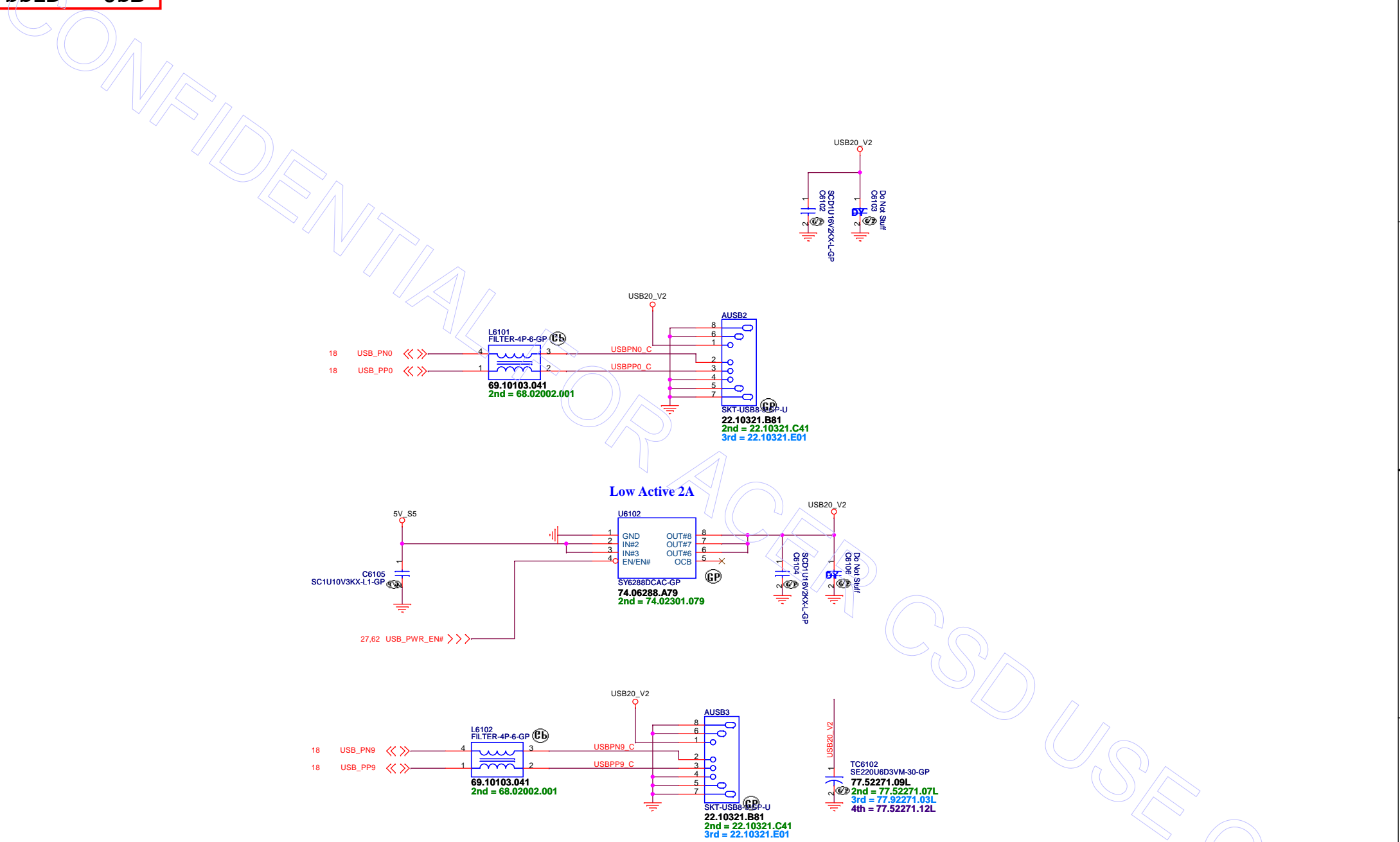
SSID = RTC

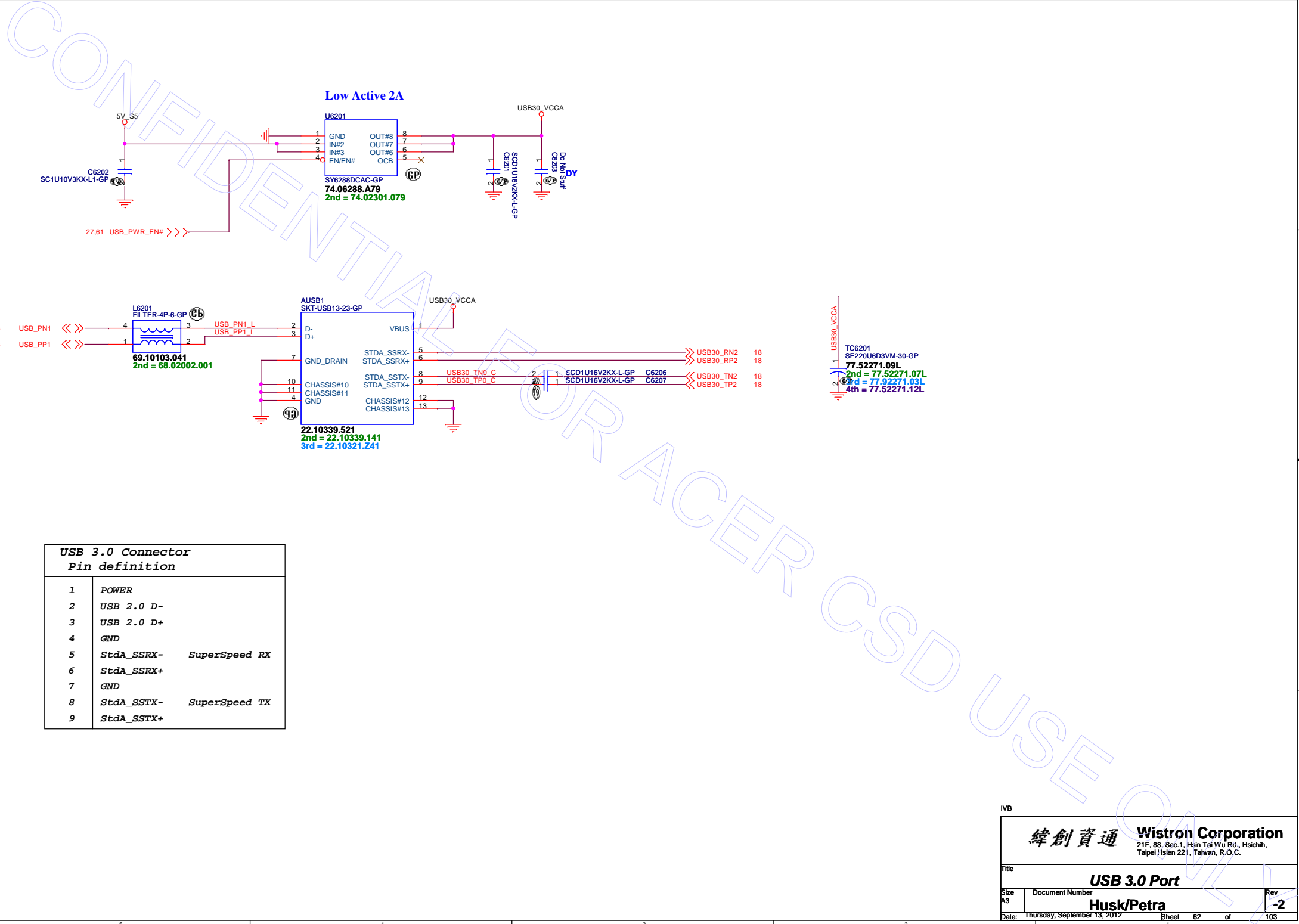


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Flash/RTC	
Size: Custom	Document Number: Husk/Petra
Date: Monday, June 11, 2012	Sheet 60 of 103
Rev: -2	

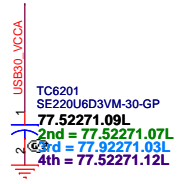
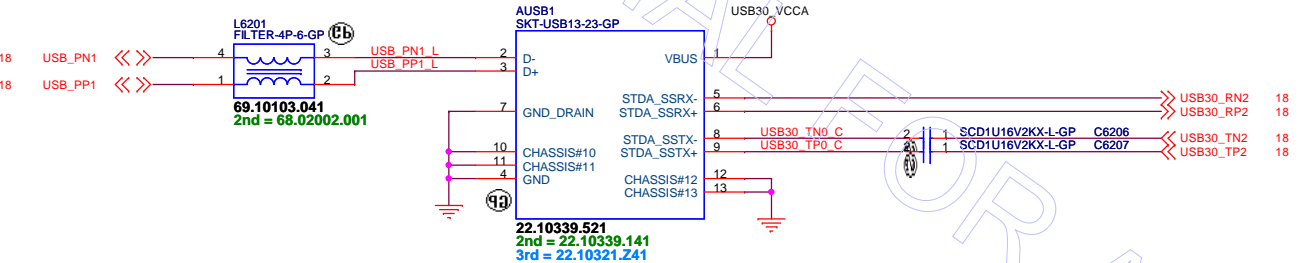
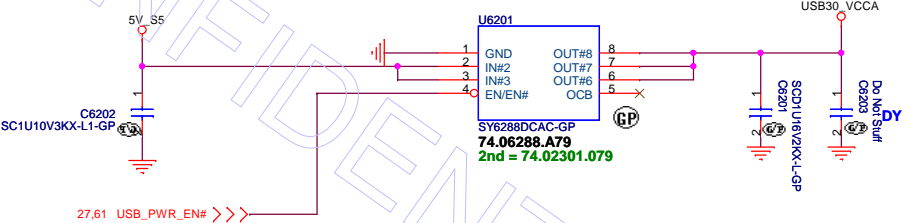
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SSID = USB





Low Active 2A



**USB 3.0 Connector
Pin definition**

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

IVB

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Bluetooth		
Size A4	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012		Sheet 63 of 103

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

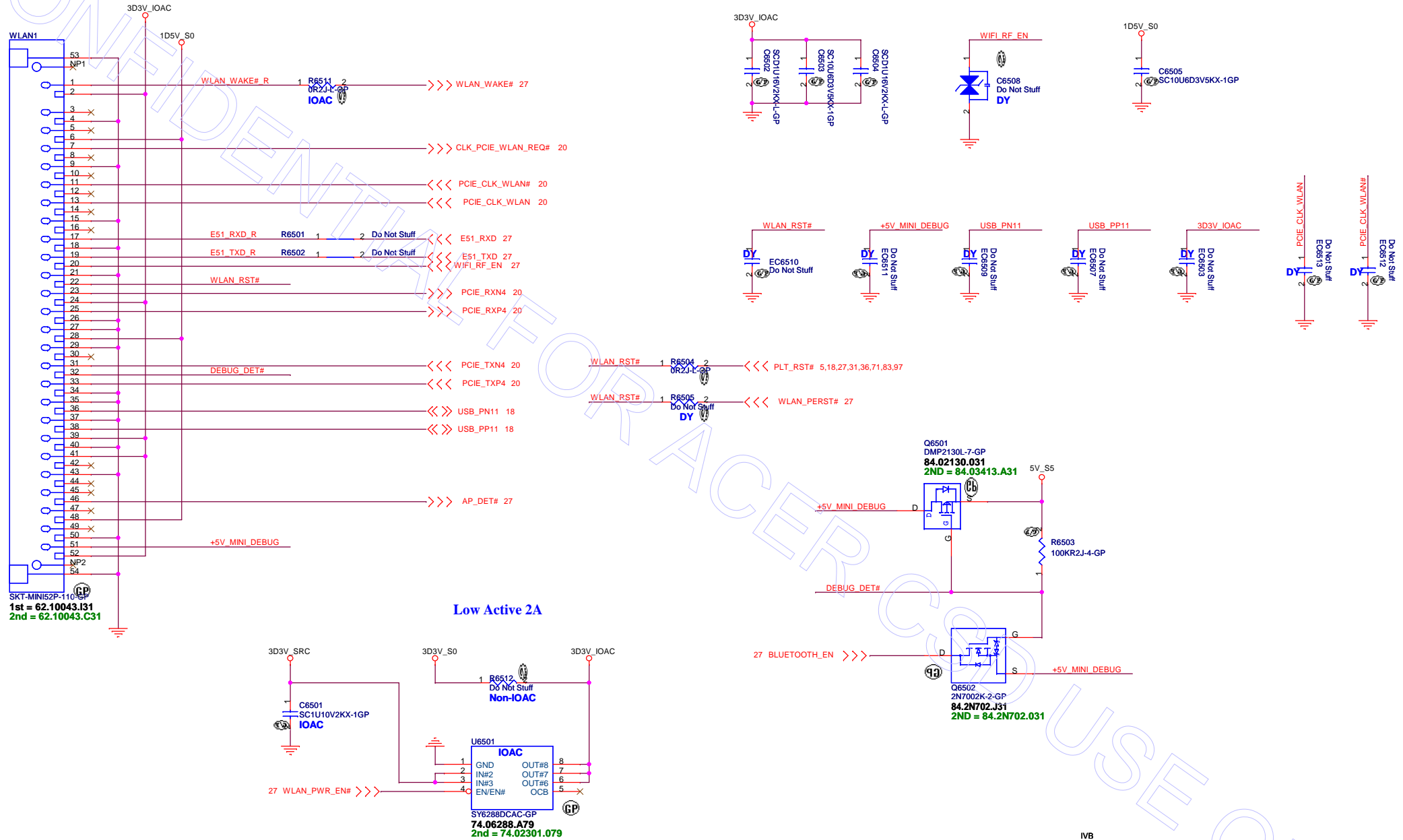
Title **RESERVED**

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



SSID = Wireless

Mini Card Connector(WWAN)

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Title **WWAN Connector**

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012 Sheet 66 of 103

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IVB

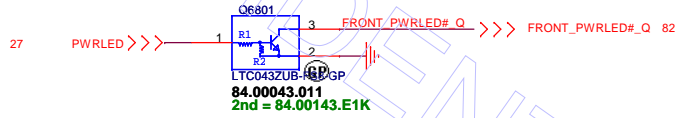
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

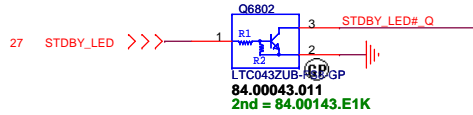
Size A4	Document Number Husk/Petra	Rev -2
------------	--------------------------------------	------------------

Date: Thursday, April 19, 2012 Sheet 67 of 103

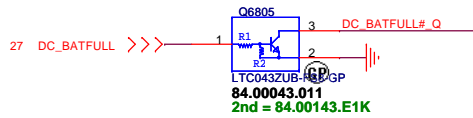
Power button LED



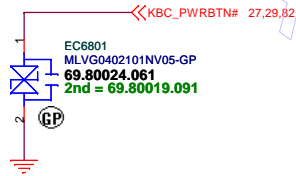
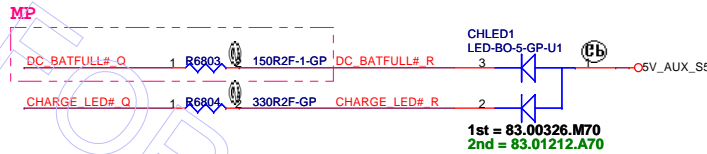
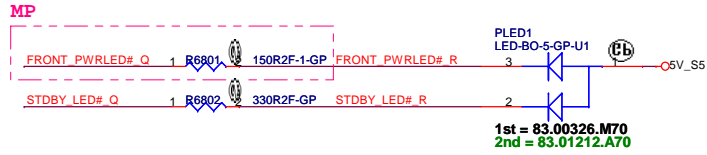
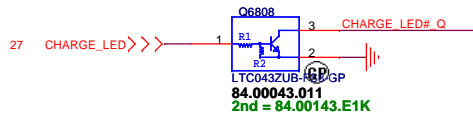
Power STDBY_LED



Battery LED2(DC_BATFULL)



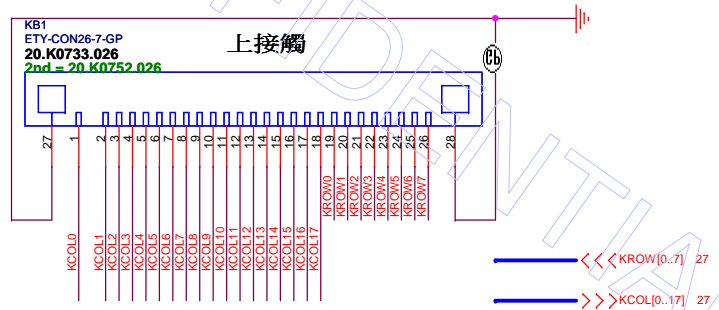
Battery LED1(CHARGE)



IVB		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED Bard/Power Button			
Size	Document Number	Rev	
Custom	Husk/Petra	-2	
Date:	Tuesday, October 09, 2012	Sheet	68 of 103

SSID = KBC

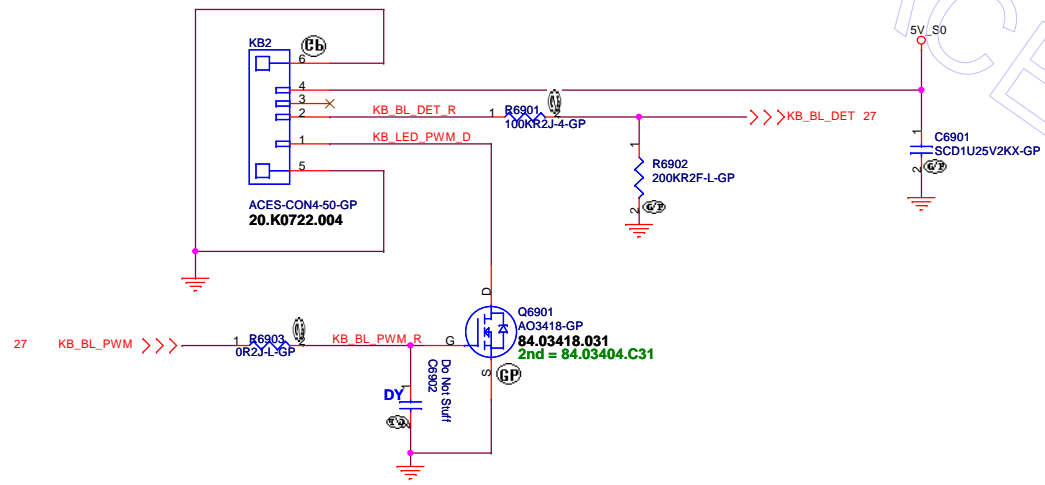
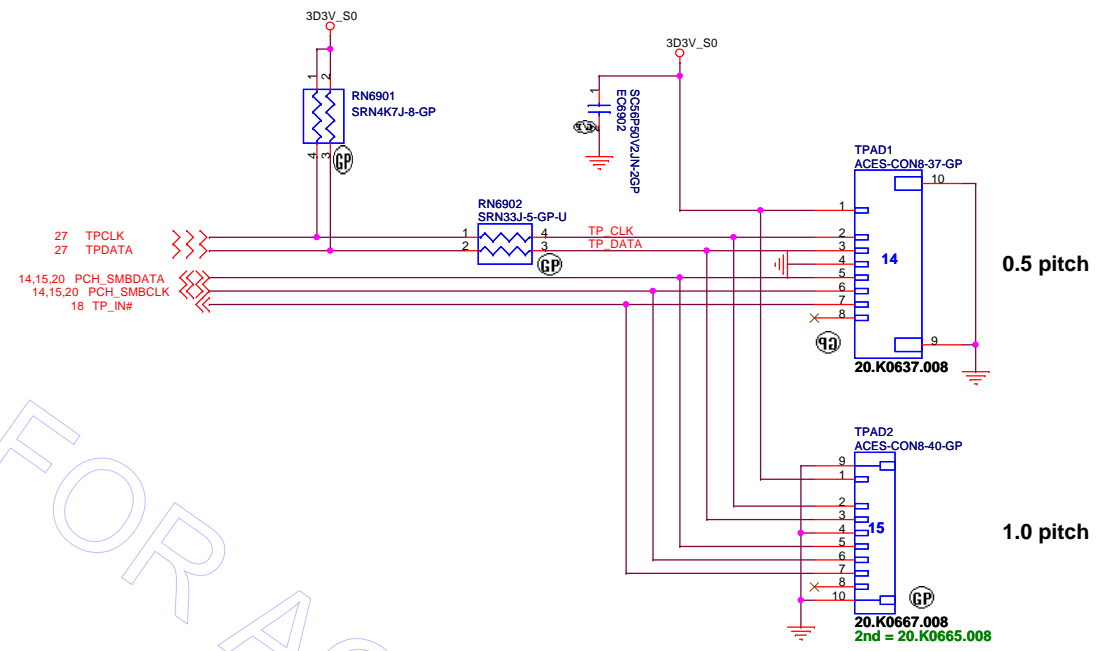
Internal KeyBoard Connector

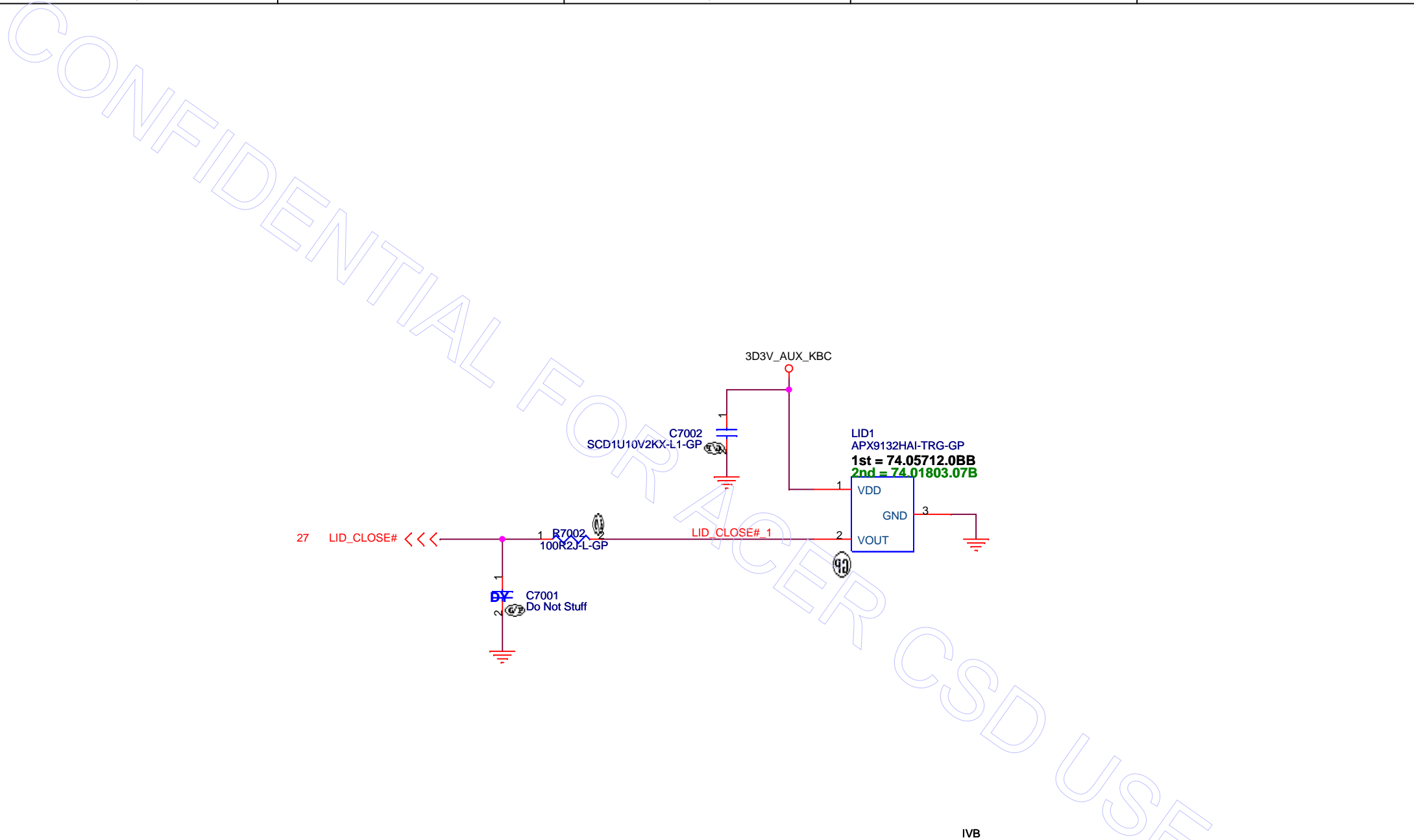


VIEW FROM TOP SIDE

R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18	C01	C02	C03	C04	C05	C06	C07	C08	
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
PIN NUMBER																										

TOUCH PAD





IVB

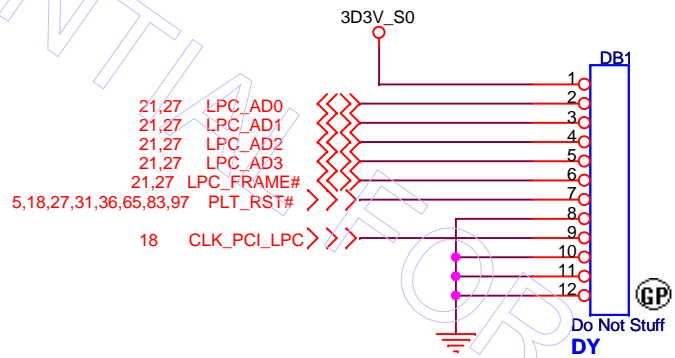
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **Hall Sensor**

Size A4	Document Number Husk/Petra	Rev -2
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size	Document Number		Rev
A4	Husk/Petra		-2
Date:	Thursday, April 19, 2012	Sheet 71	of 103

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IVB		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Reserved		
Size A3	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012	Sheet 72	of 103

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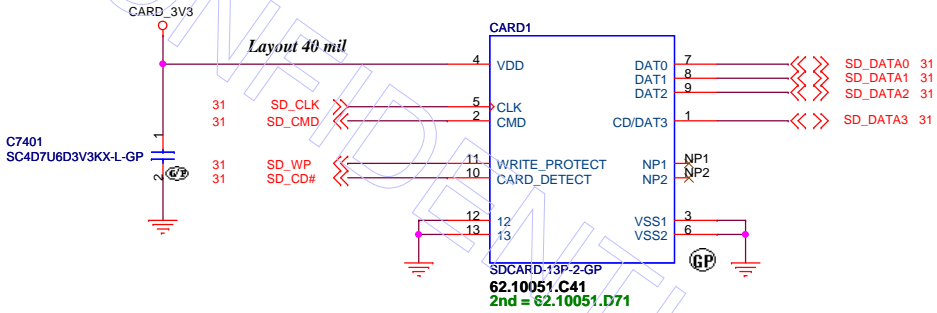
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IVB

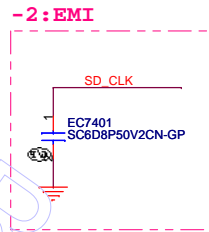
緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	Husk/Petra	-2	
Date:	Thursday, April 19, 2012	Sheet 73	of 103

SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5	MS_INS#	xD_CE#
SP4	SP4	SD_D4	MS_INS#	xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2	MS_D7	xD_D7
SP11	SP11	MS_BS	MS_D1	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16			xD_CD#



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CARD Reader CONN		
Size	Document Number	Rev
Custom	Husk/Petra	-2
Date:	Thursday, April 19, 2012	Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

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IVB		緯創資通 Wistron Corporation <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title		New Card	
Size A3	Document Number Husk/Petra	Rev -2	
Date: Thursday, April 19, 2012	Sheet 75	of 103	

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IVB

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012 Sheet 76 of 103

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Title

Reserved

Size

A4

Document Number

Husk/Petra

Rev

-2

Date: Thursday, April 19, 2012

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
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SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

IVB

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
G- Sensor					
Size	Document Number				Rev
A4	Husk/Petra				-2
Date:	Thursday, April 19, 2012			Sheet	79 of 103

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number Husk/Petra	Rev -2
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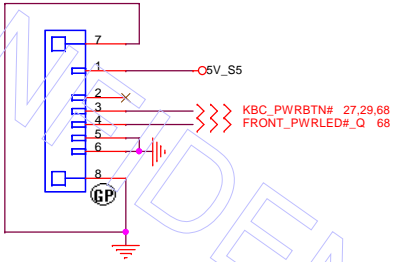
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(Blanking)

IVB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Reserved		
Size A4	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012		Sheet 81 of 103

PWRCN1
ACES-CON6-52-GP
20.K0721.006
2nd = 20.K0382.006

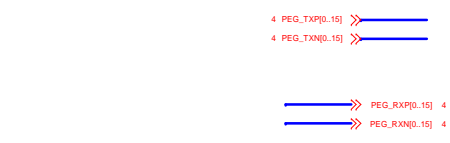
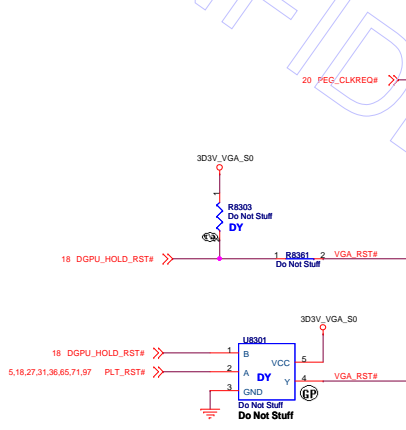


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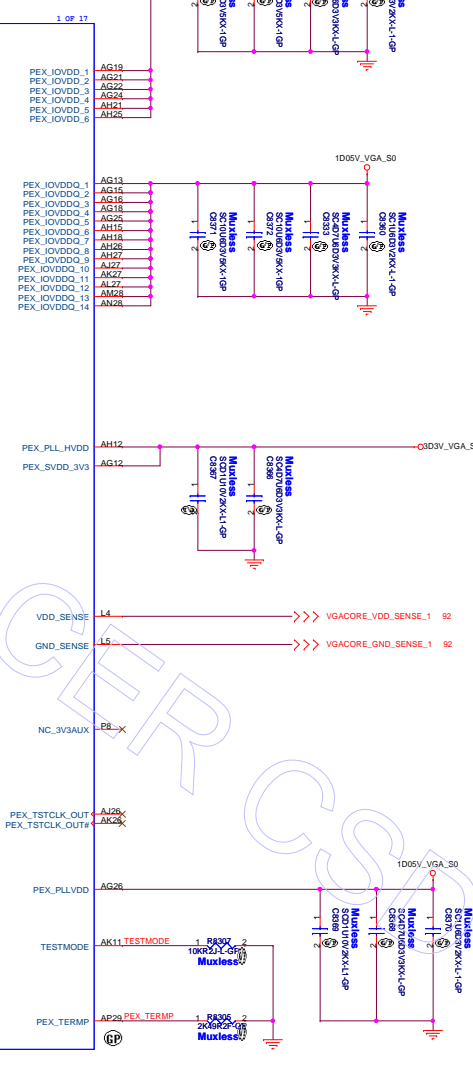
IVB

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title IO Board Connector		
Size A3	Document Number Husk/Petra	Rev -2
Date: Thursday, April 19, 2012	Sheet 82 of 103	

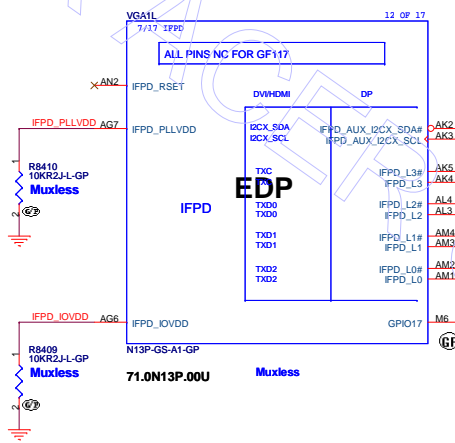
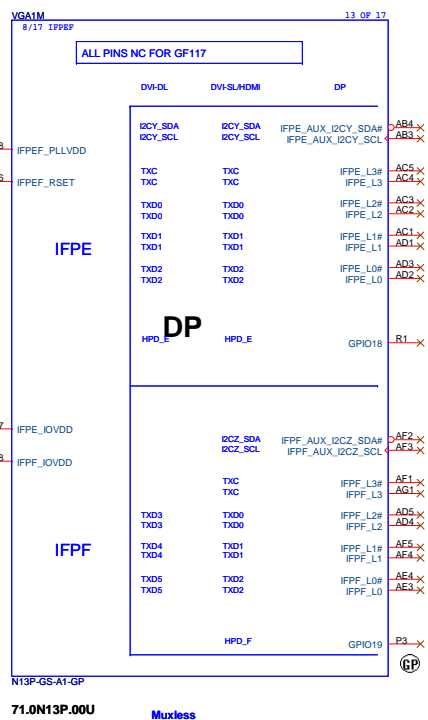
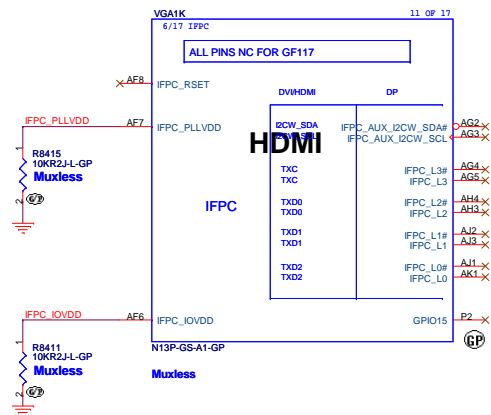
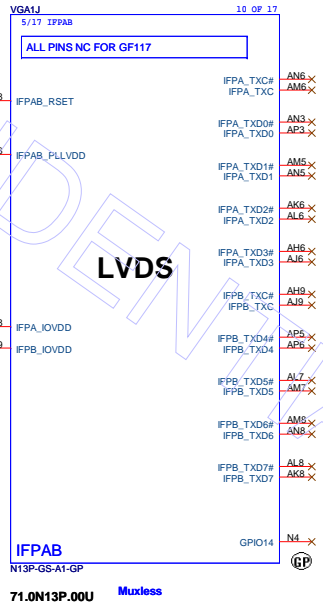
CONFIDENTIAL

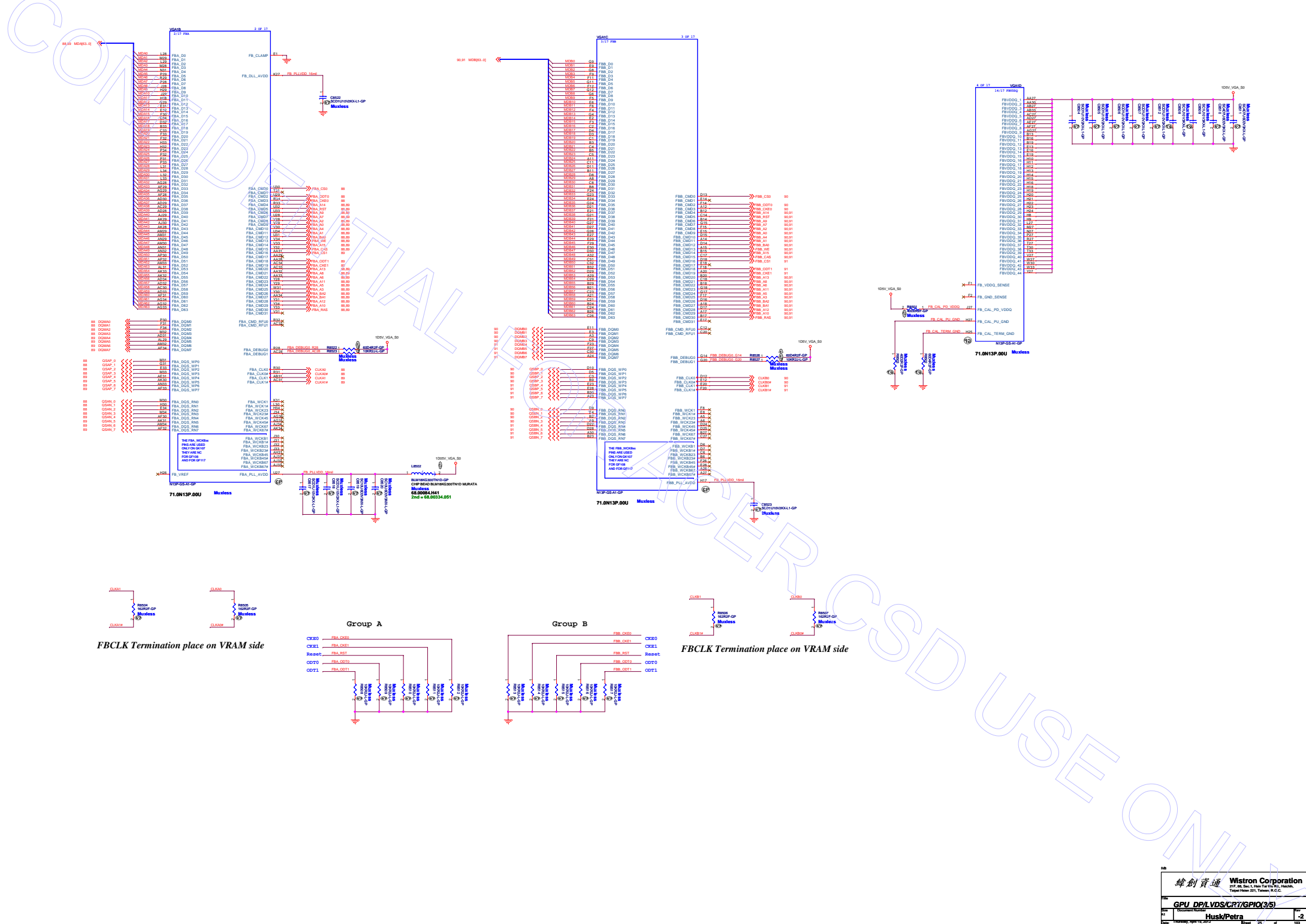


Signal	Component	Value	Model	Signal	Component	Value	Model
PEG_RXP0	C8301	1	SCD22U10V2KX-1GP	PEG_C_RXP0	AK14		
PEG_RXN0	C8302	1	SCD22U10V2KX-1GP	PEG_C_RXN0	AK14		
PEG_RXP1	C8303	1	SCD22U10V2KX-1GP	PEG_C_RXP1	AK14		
PEG_RXN1	C8304	1	SCD22U10V2KX-1GP	PEG_C_RXN1	AK14		
PEG_RXP2	C8305	1	SCD22U10V2KX-1GP	PEG_C_RXP2	AK15		
PEG_RXN2	C8306	1	SCD22U10V2KX-1GP	PEG_C_RXN2	AK15		
PEG_RXP3	C8307	1	SCD22U10V2KX-1GP	PEG_C_RXP3	AK16		
PEG_RXN3	C8308	1	SCD22U10V2KX-1GP	PEG_C_RXN3	AK16		
PEG_RXP4	C8309	1	SCD22U10V2KX-1GP	PEG_C_RXP4	AK17		
PEG_RXN4	C8310	1	SCD22U10V2KX-1GP	PEG_C_RXN4	AK17		
PEG_RXP5	C8311	1	SCD22U10V2KX-1GP	PEG_C_RXP5	AK17		
PEG_RXN5	C8312	1	SCD22U10V2KX-1GP	PEG_C_RXN5	AK17		
PEG_RXP6	C8313	1	SCD22U10V2KX-1GP	PEG_C_RXP6	AK18		
PEG_RXN6	C8314	1	SCD22U10V2KX-1GP	PEG_C_RXN6	AK18		
PEG_RXP7	C8315	1	SCD22U10V2KX-1GP	PEG_C_RXP7	AK19		
PEG_RXN7	C8316	1	SCD22U10V2KX-1GP	PEG_C_RXN7	AK19		
PEG_RXP8	C8317	1	SCD22U10V2KX-1GP	PEG_C_RXP8	AK20		
PEG_RXN8	C8318	1	SCD22U10V2KX-1GP	PEG_C_RXN8	AK20		
PEG_RXP9	C8319	1	SCD22U10V2KX-1GP	PEG_C_RXP9	AK20		
PEG_RXN9	C8320	1	SCD22U10V2KX-1GP	PEG_C_RXN9	AK20		
PEG_RXP10	C8321	1	SCD22U10V2KX-1GP	PEG_C_RXP10	AK21		
PEG_RXN10	C8322	1	SCD22U10V2KX-1GP	PEG_C_RXN10	AK21		
PEG_RXP11	C8323	1	SCD22U10V2KX-1GP	PEG_C_RXP11	AK22		
PEG_RXN11	C8324	1	SCD22U10V2KX-1GP	PEG_C_RXN11	AK22		
PEG_RXP12	C8325	1	SCD22U10V2KX-1GP	PEG_C_RXP12	AK23		
PEG_RXN12	C8326	1	SCD22U10V2KX-1GP	PEG_C_RXN12	AK23		
PEG_RXP13	C8327	1	SCD22U10V2KX-1GP	PEG_C_RXP13	AK24		
PEG_RXN13	C8328	1	SCD22U10V2KX-1GP	PEG_C_RXN13	AK24		
PEG_RXP14	C8329	1	SCD22U10V2KX-1GP	PEG_C_RXP14	AK24		
PEG_RXN14	C8330	1	SCD22U10V2KX-1GP	PEG_C_RXN14	AK24		
PEG_RXP15	C8331	1	SCD22U10V2KX-1GP	PEG_C_RXP15	AK25		
PEG_RXN15	C8332	1	SCD22U10V2KX-1GP	PEG_C_RXN15	AK25		



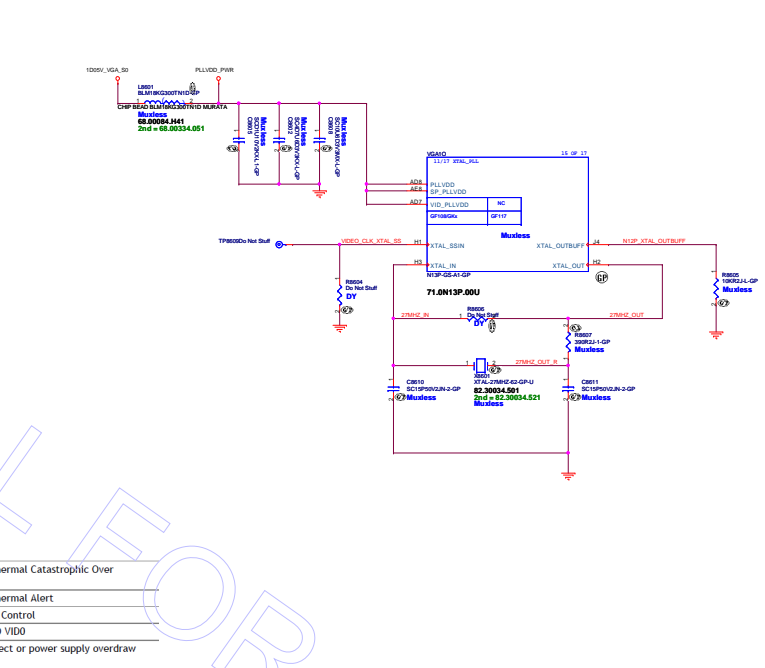
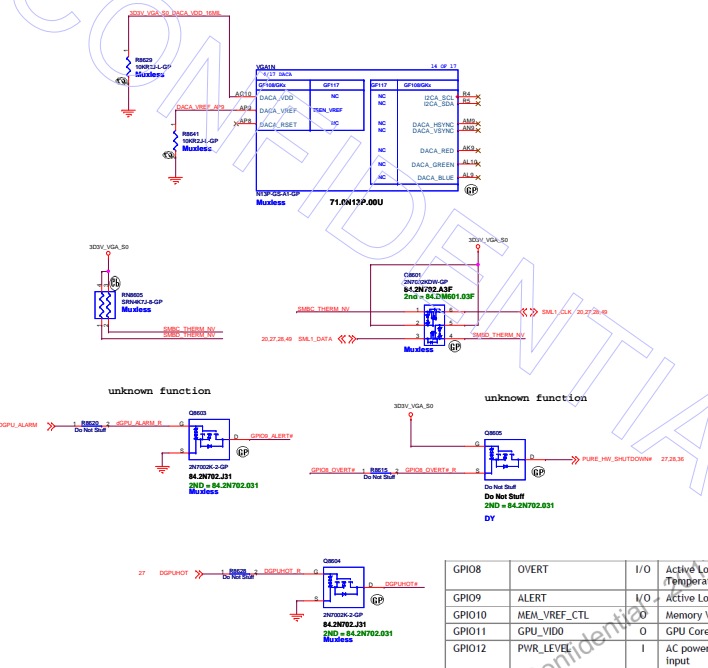
N13P-GS-A1-GP
71.0N13P.00U Muxless



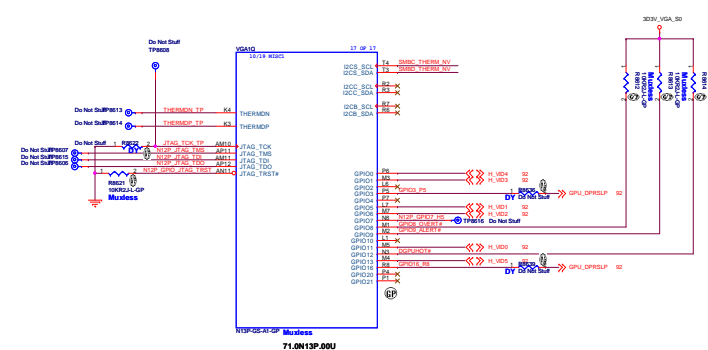


FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side



GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input



VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

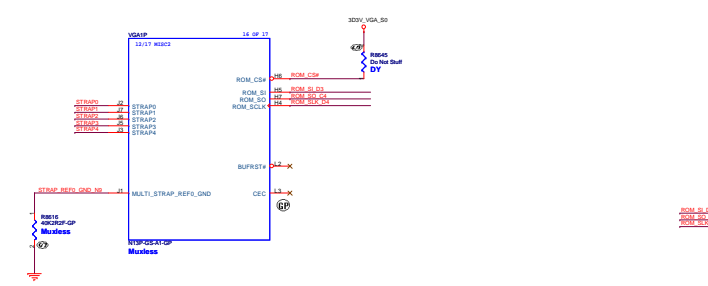
	Hynix 2G_D-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16	5Kohm 64.49915.6DL
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL	10Kohm 64.10025.L0L

VRAM Table(N13M-GS/NS)

Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

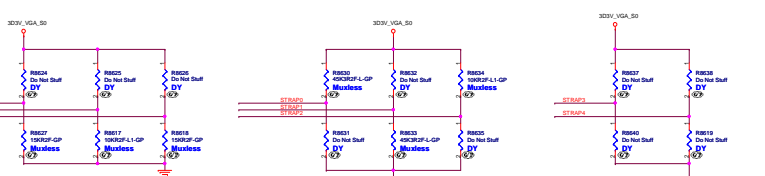
Mode	Product	NVCLK (MHz)	MCLK (MHz)	MVDD (V)
MAX Point (MP)	H13P-GL/-HS1	800	900	-
	H13P-GLP	660	900	-
TDP Point (TP)	H13P-GL/-HS1	660	900	-
	H13P-GLP	475	900	-
HW Boot Voltage	H13P-GL/-HS1	-	-	0.95
	H13P-GLP	-	-	0.90

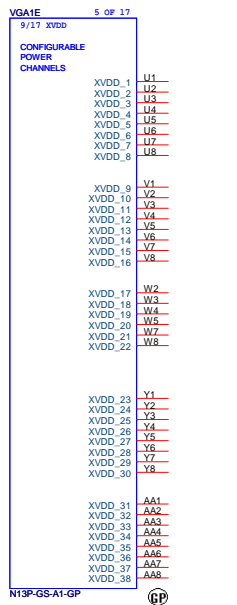
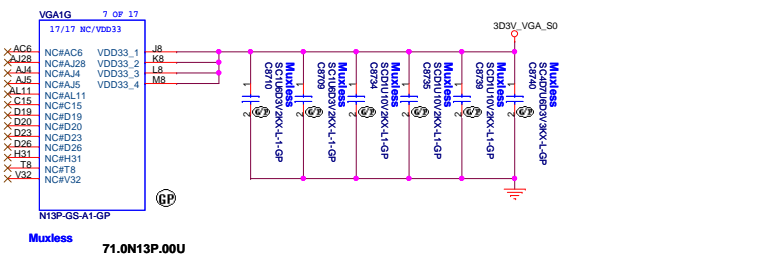
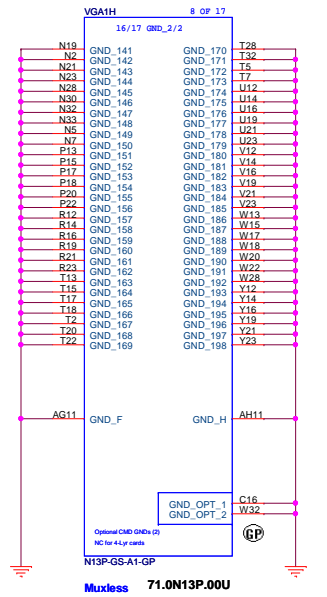
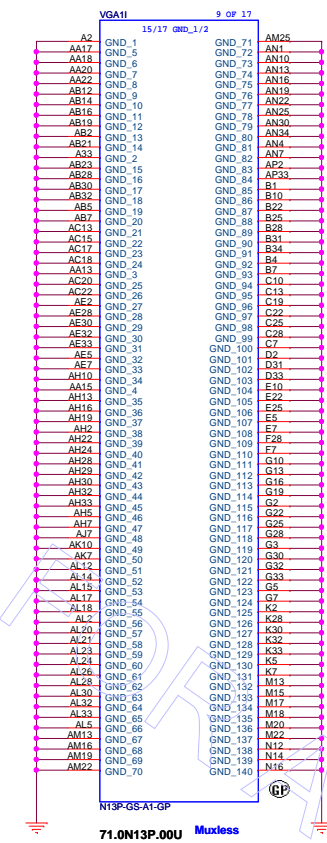
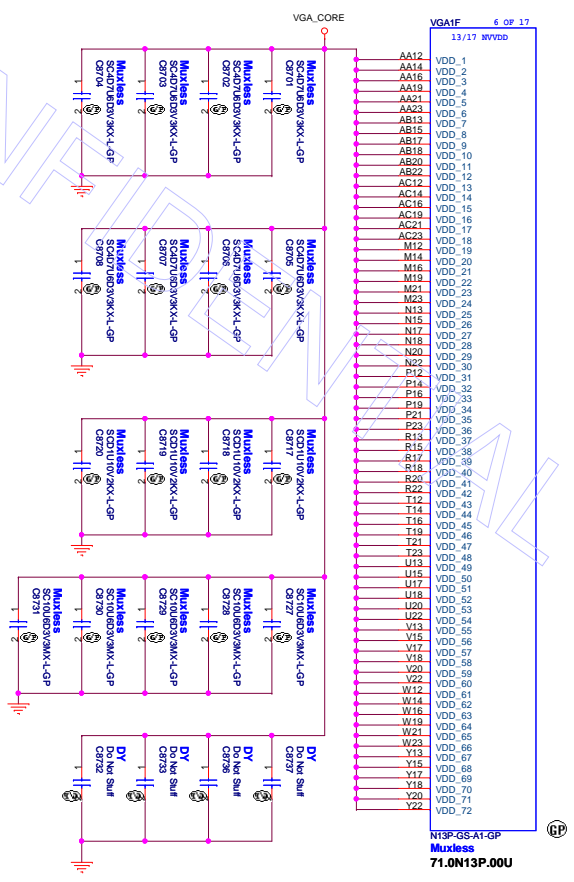
Strap Pin Nmae	Logical strapting name bit#3	Logical strapting name bit#2	Logical strapting name bit#1	Logical strapting name bit#0	
ROM_SCLK	PCLDEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/	PEX_PLLN_TERM	
	0	0	1	0	15K ohm pull-down
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
PON#SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	
	0	0	0	1	10K ohm pull-down
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[5]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	1	1	1	45K ohm pull-down
STRAP2	PCLDEVID[1]	PCLDEVID[2]	PCLDEVID[1]	PCLDEVID[0]	
	1	0	0	1	10K ohm pull-up
STRAP3	N/A	N/A	N/A	N/A	
STRAP4	N/A	N/A	N/A	N/A	



Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
50kohms	1000	0000
100kohms	1001	0001
150kohms	1010	0010
200kohms	1011	0011
250kohms	1100	0100
300kohms	1101	0101
350kohms	1110	0110
400kohms	1111	0111

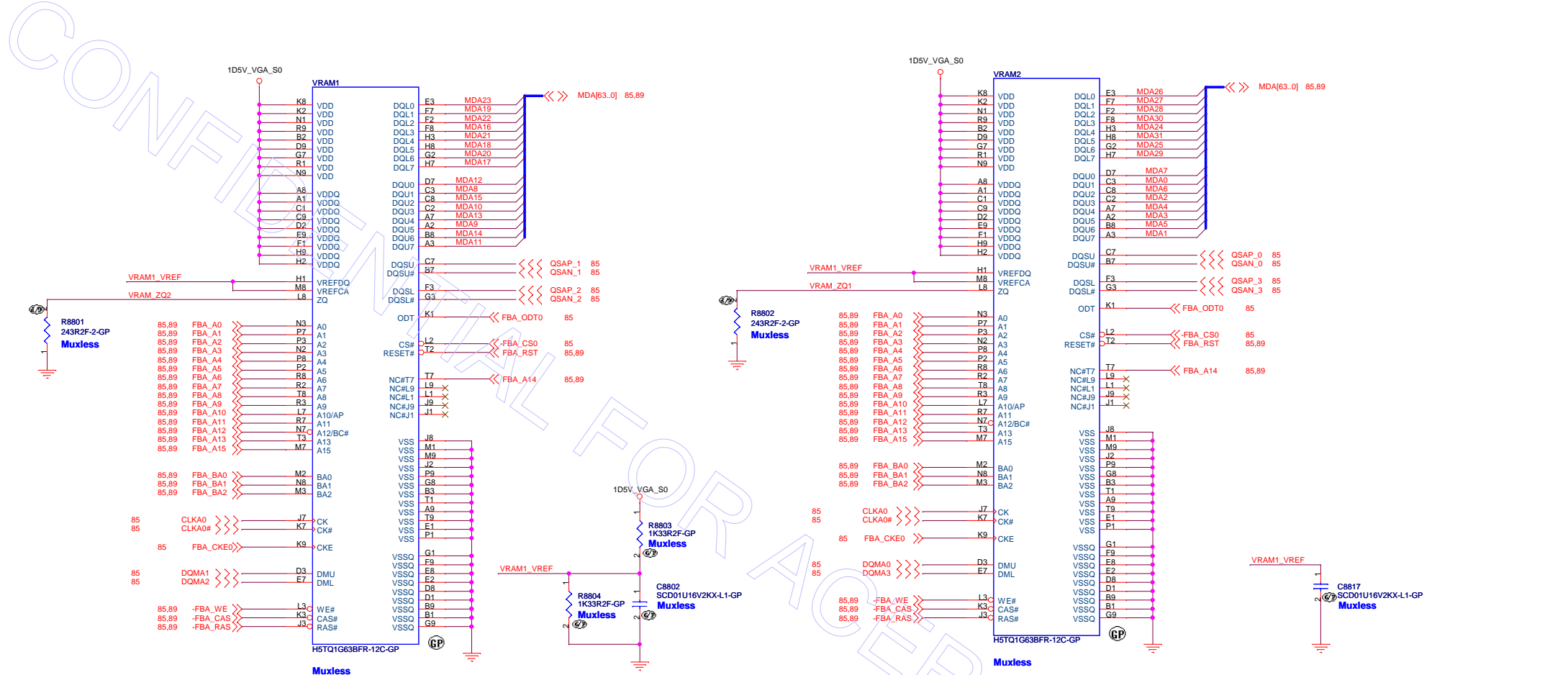




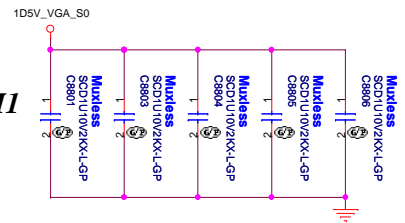
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 Taipei Hsien 221, Taiwan, R.O.C.

Title GPU_DPPWR/GND(5/5)
Size Document Number
Customer Husk/Petra
Date Thursday, April 19, 2012 **Sheet** 87 of 103

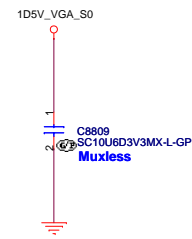
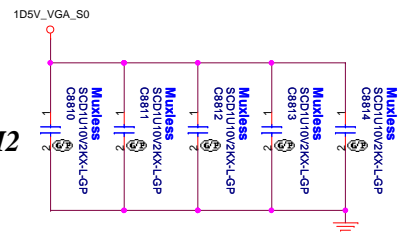
Rev -2

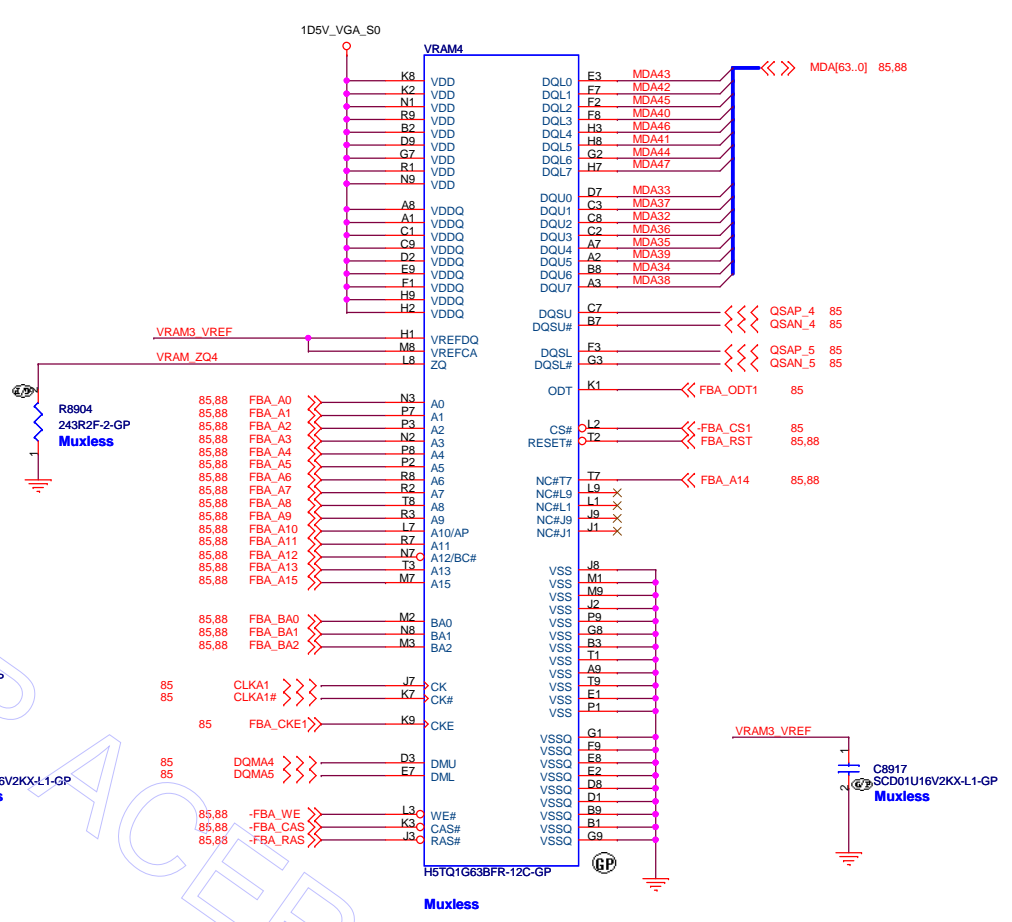
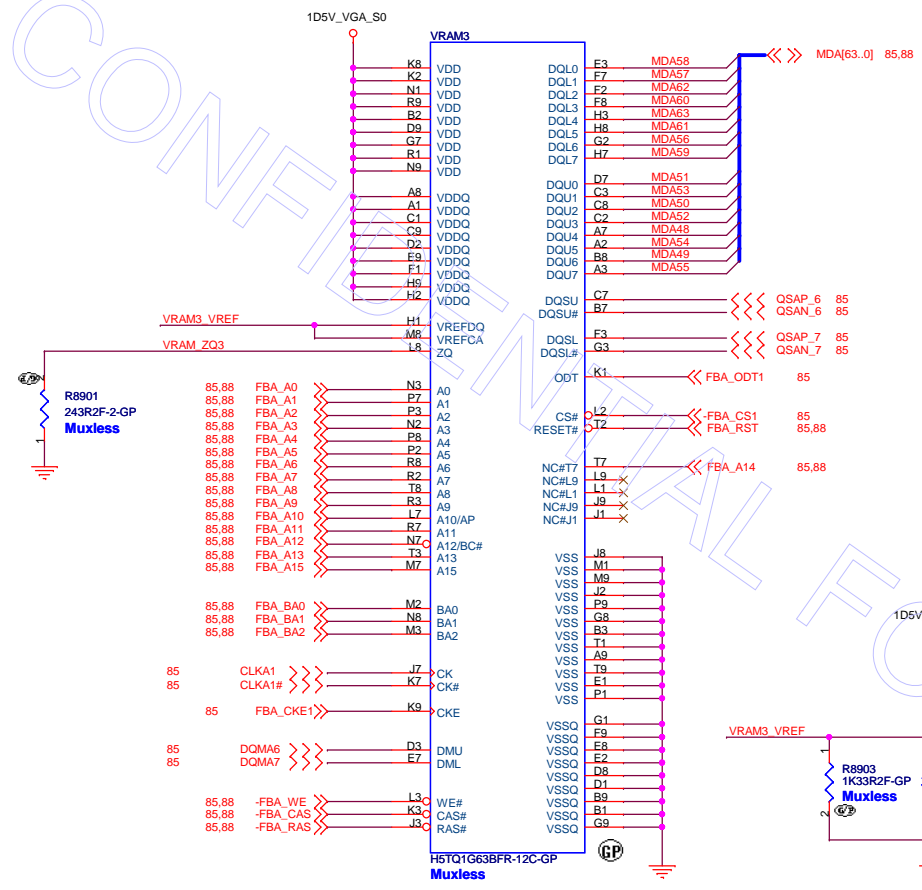


FOR VRAM1

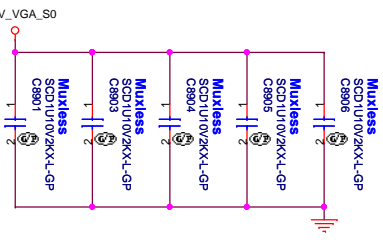


FOR VRAM2

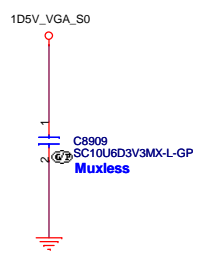
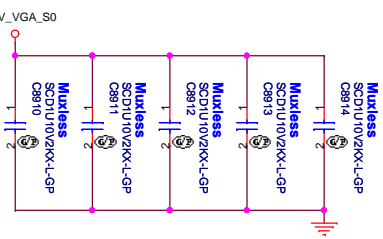




FOR VRAM3



FOR VRAM4



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Title: **GPU-VRAM3,4 (2/4)**

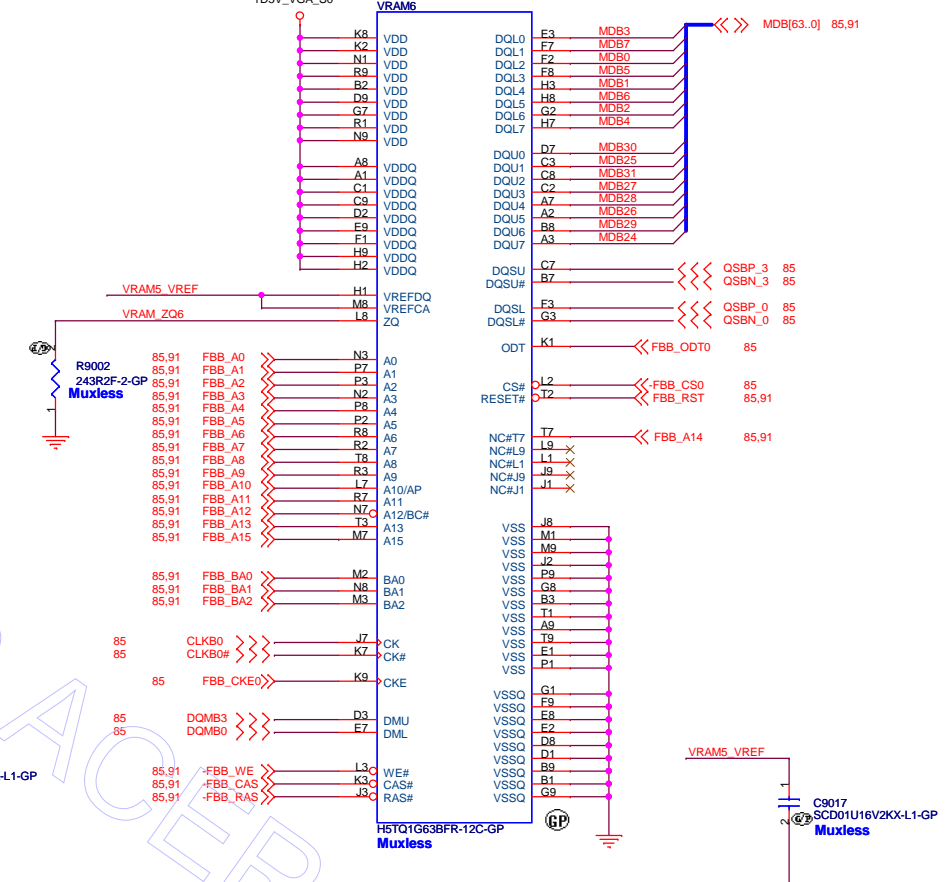
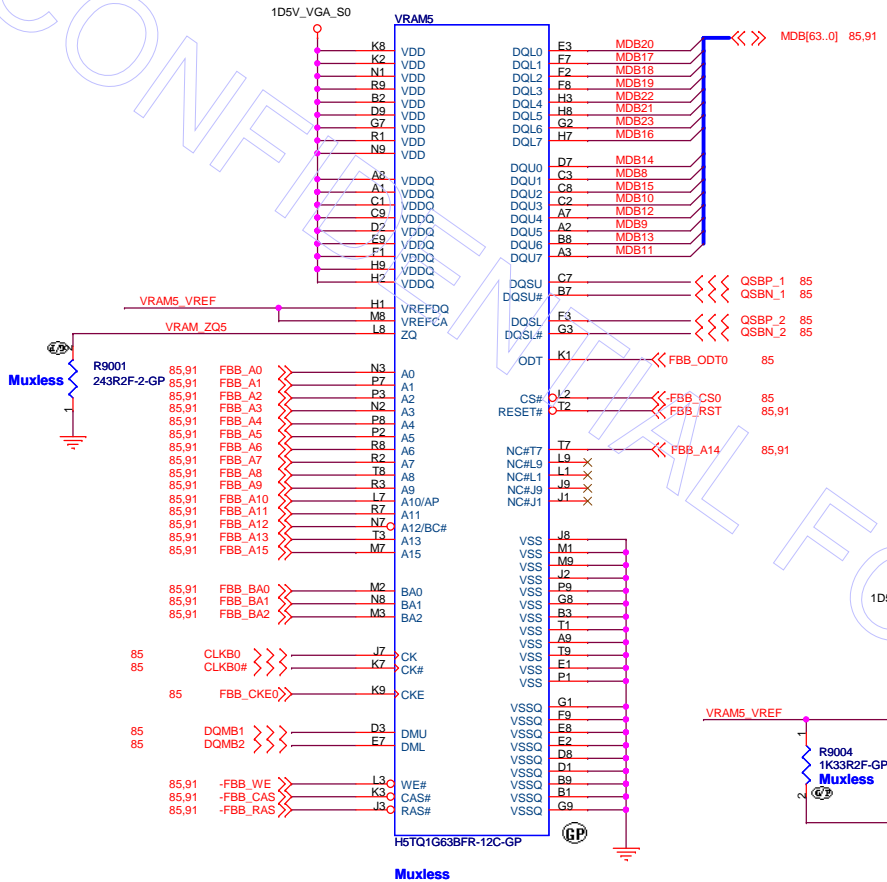
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Document Number: **Husk/Petra**

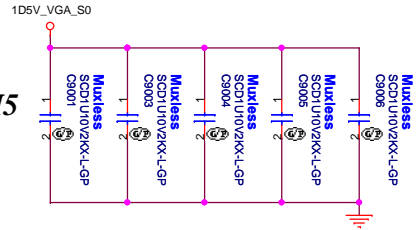
Date: Thursday, April 19, 2012

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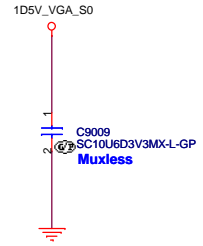
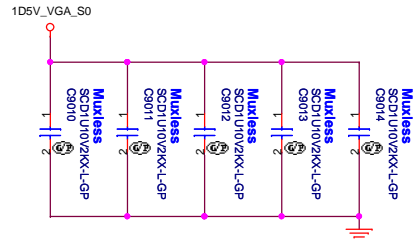
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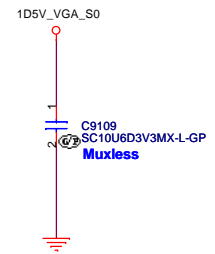
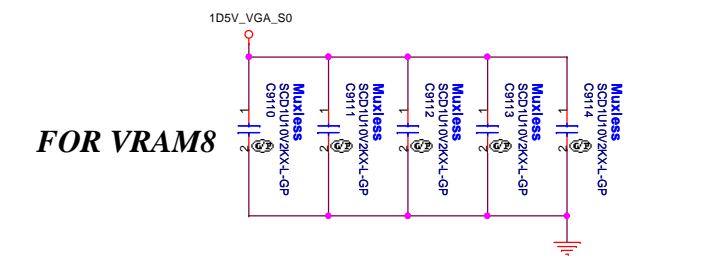
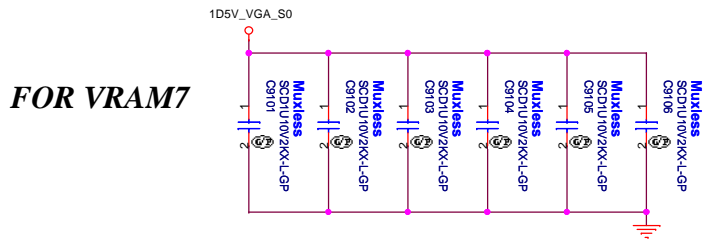
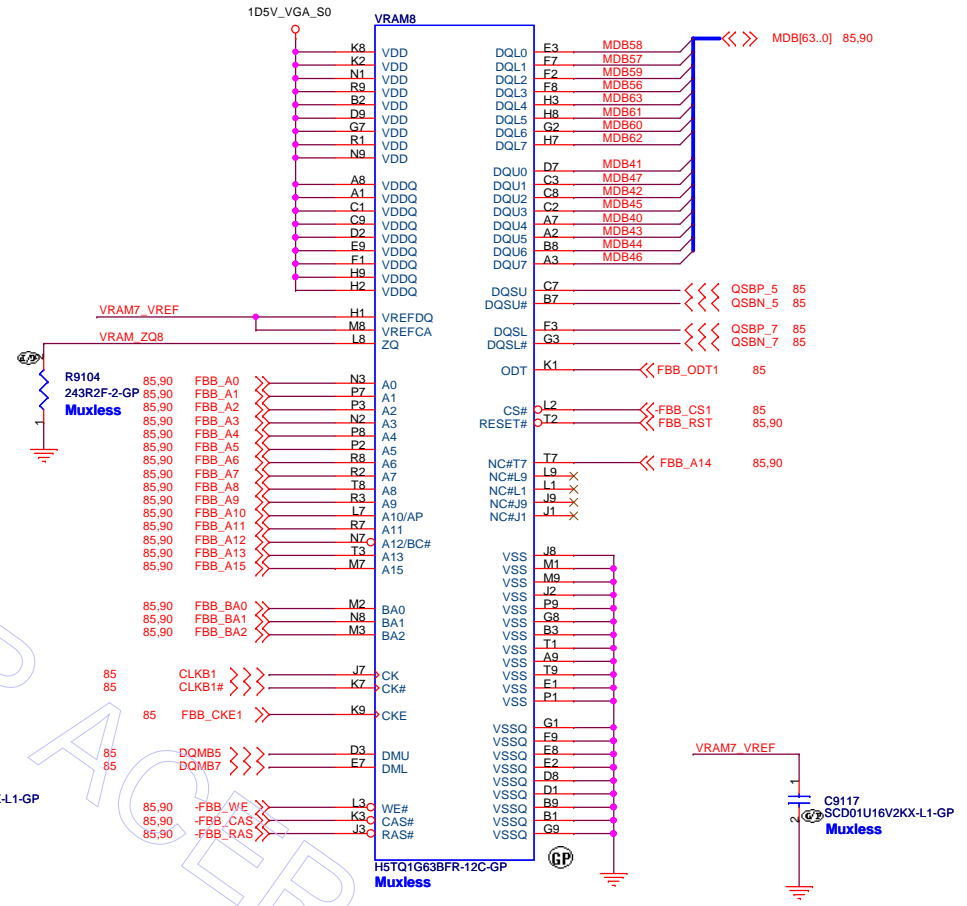
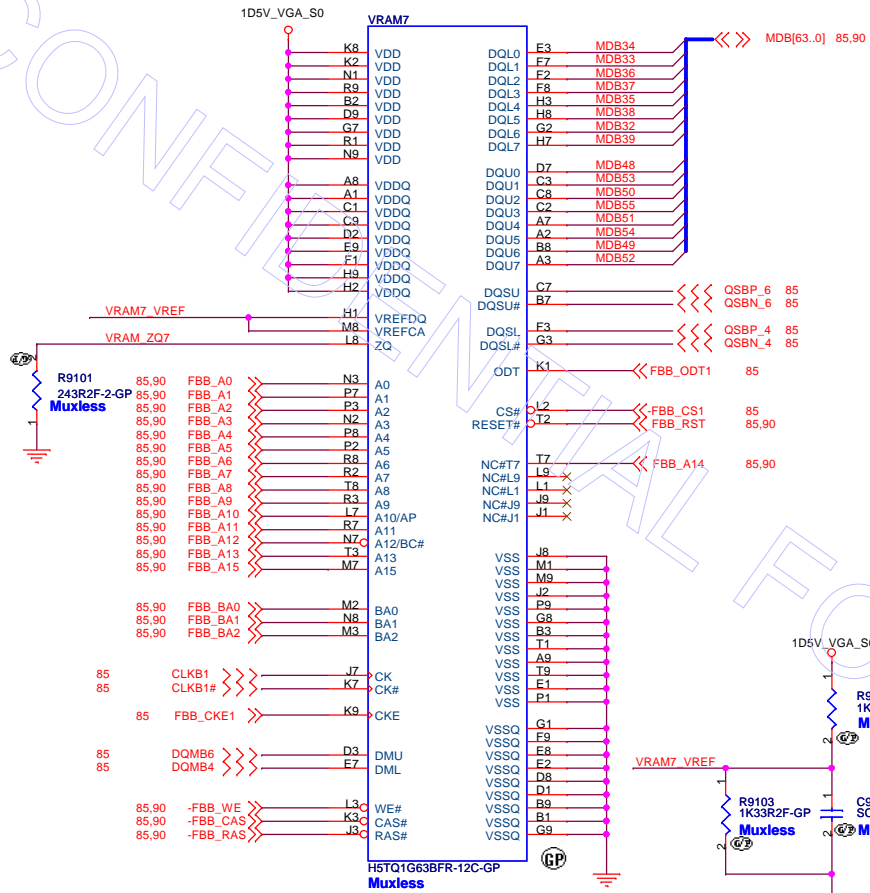


FOR VRAM5

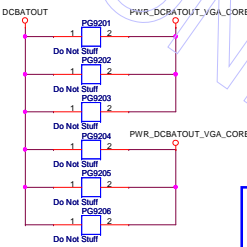


FOR VRAM6



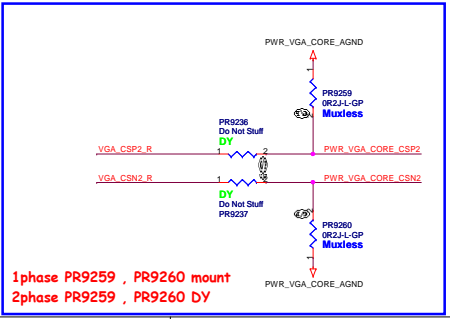
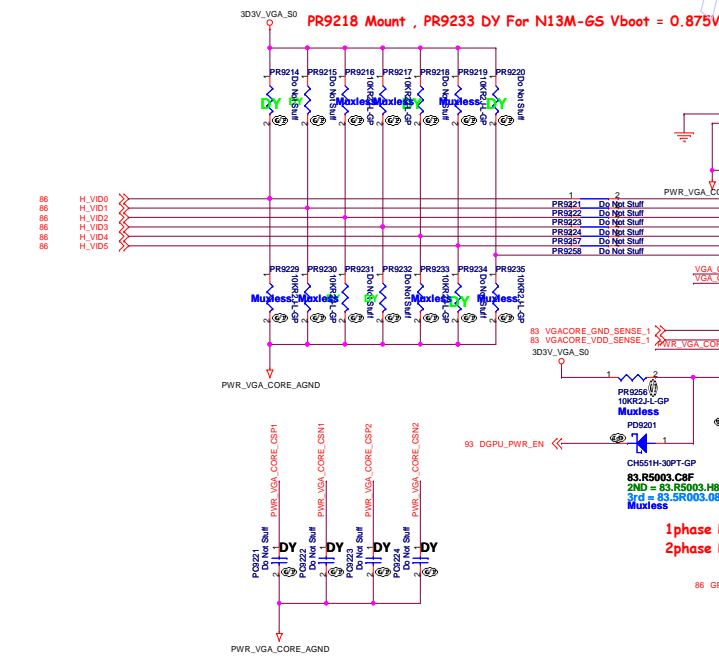


SSID = PWR.Plane.Regulator_GFX

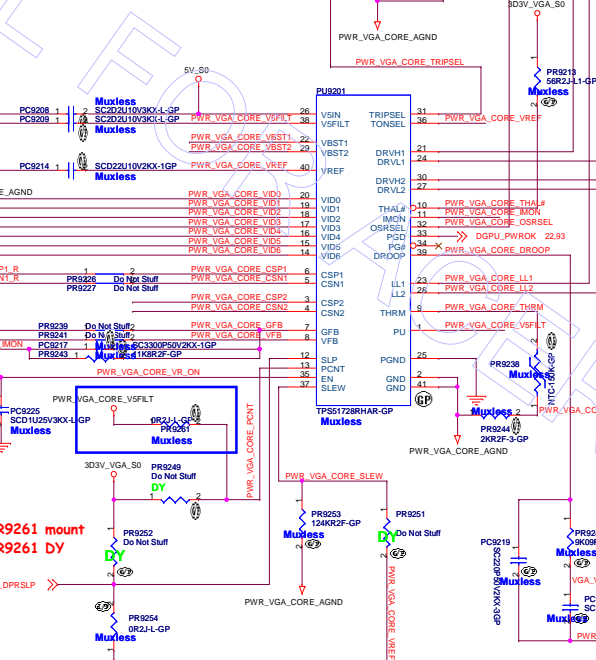


	N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NV_VDD Boot Voltage	0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]01010010
NV_VID1	PR9215 DY	DY	63.10334.L0L
	PR9230 63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217 DY	63.10334.L0L	DY
	PR9232 63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218 63.10334.L0L	DY	63.10334.L0L
	PR9233 DY	63.10334.L0L	DY

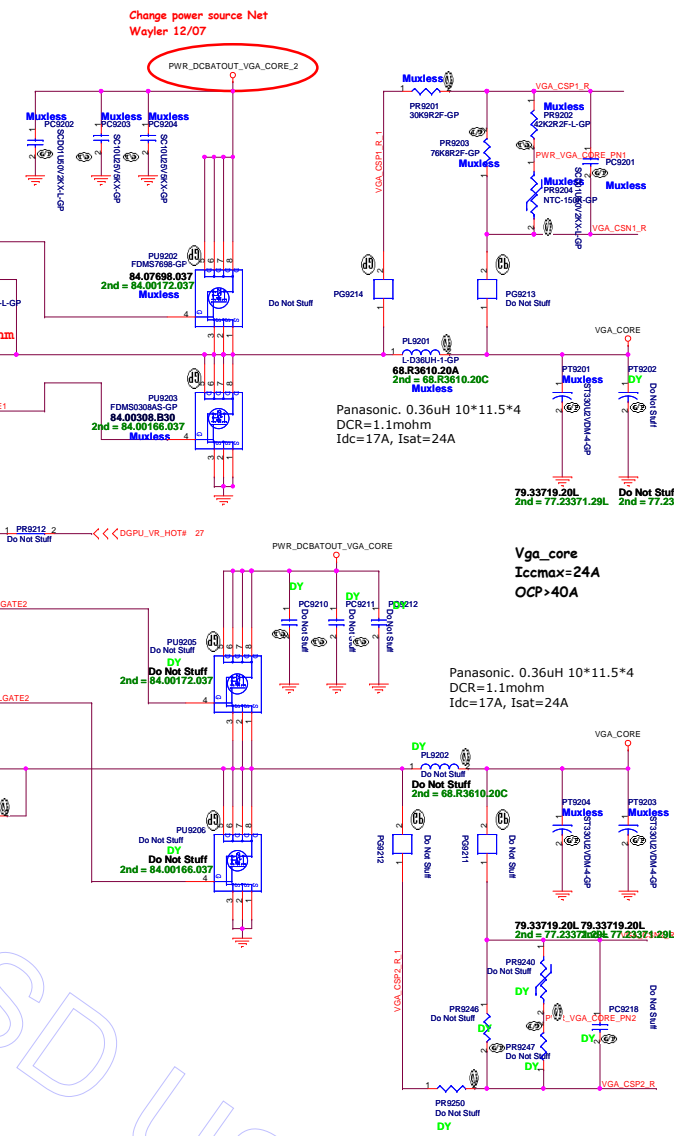
PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V



1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY



1phase PR9261 mount
2phase PR9261 DY



Change power source Net
Wayler 12/07

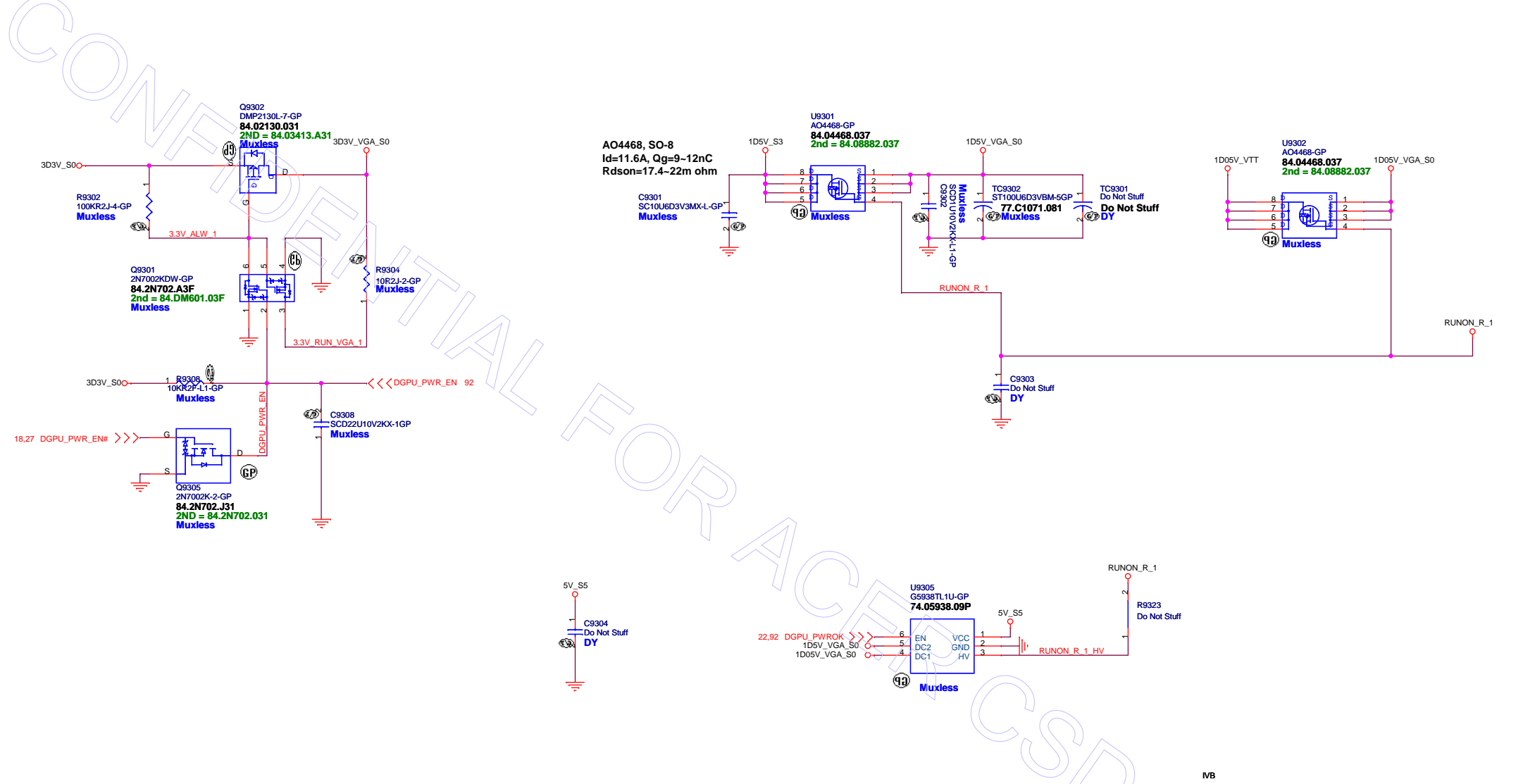
PWR_DCBATOUT_VGA_CORE_2

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A



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DISCRETE VGA POWER	
Title	
Size	Document Number
Custom	Husk/Petra
Date	Tuesday, October 09, 2012
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Title	
LVDS Switch	

Size A4	Document Number Husk/Petra	Rev -2
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Date: Thursday, April 19, 2012	Sheet 94 of 103
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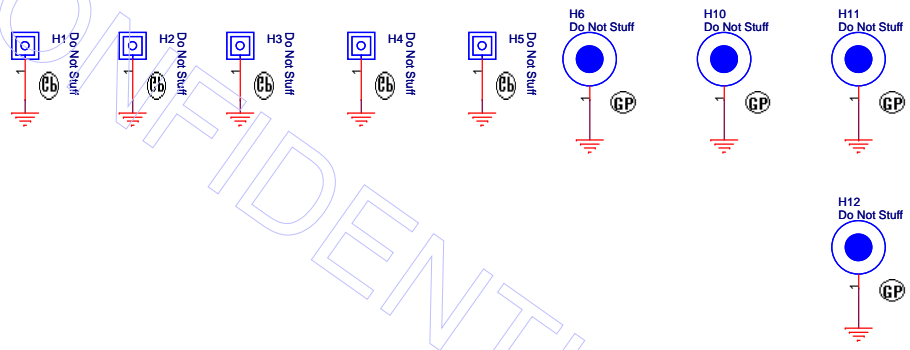
IVB

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Title			
CRT Switch			
Size	Document Number	Rev	
A3	Husk/Petra	-2	
Date:	Thursday, April 19, 2012	Sheet 95	of 103

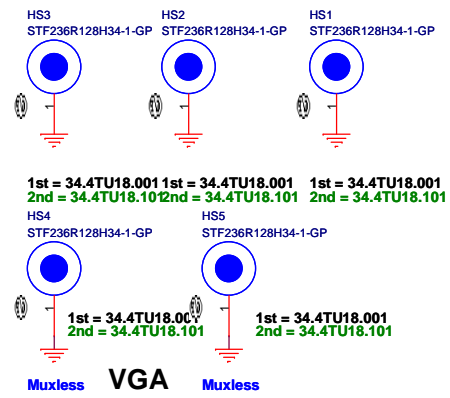
SSID = SDIO

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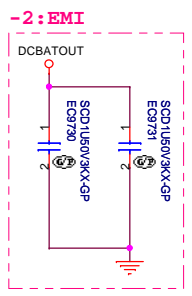
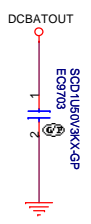
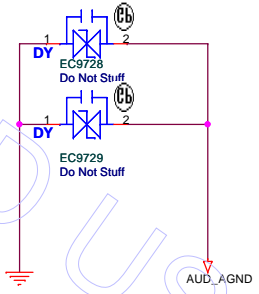
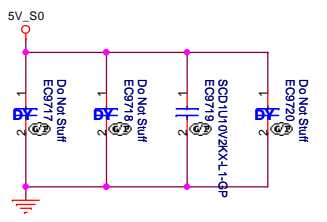
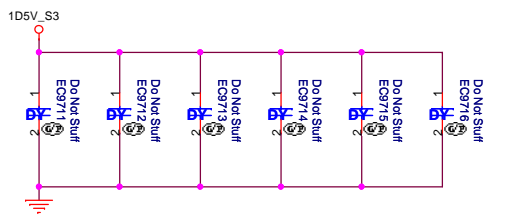
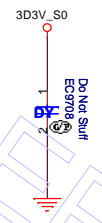
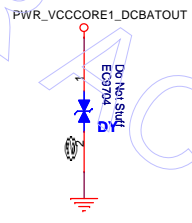
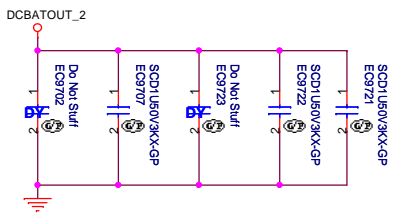
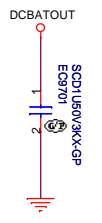
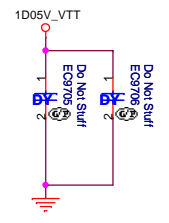
CPU



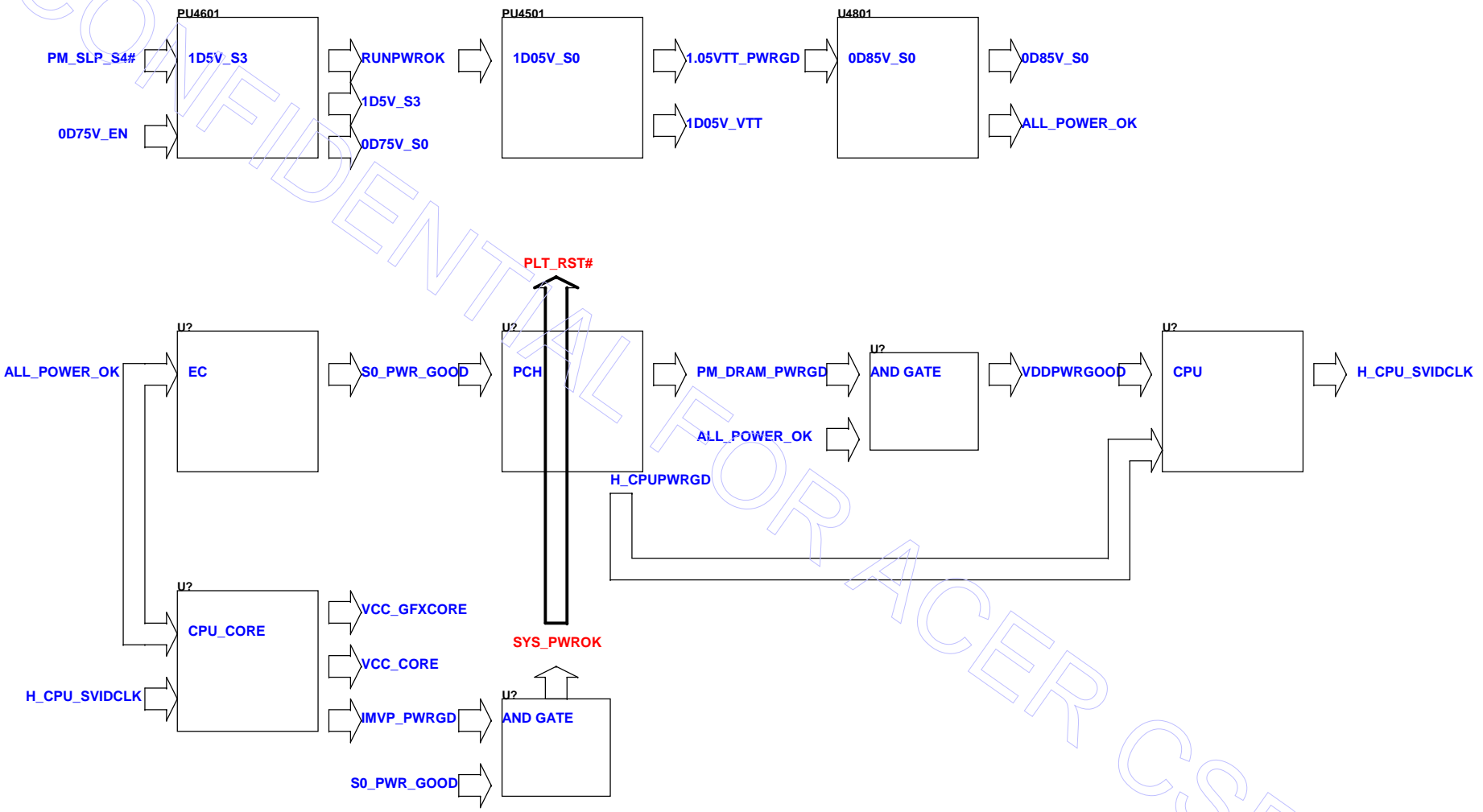
Check test point

3D3V_S0C	1	⊖	AFTP1
3D3V_AUX_S5C	1	⊖	AFTP7
3D3V_S5C	1	⊖	AFTP8
5V_S5C	1	⊖	AFTP9
19.27 PM_PWRBTN#	<<<	⊖	AFTP10
5.22.36 H_CPUUPWRGD	>>>	⊖	AFTP11
27.36 S5_ENABLE	<<<	⊖	AFTP12
5.19.27.31.36.65.71.83 PLT_RST#	>>>	⊖	AFTP13

Test Point放在Dimm Door打開可量測處



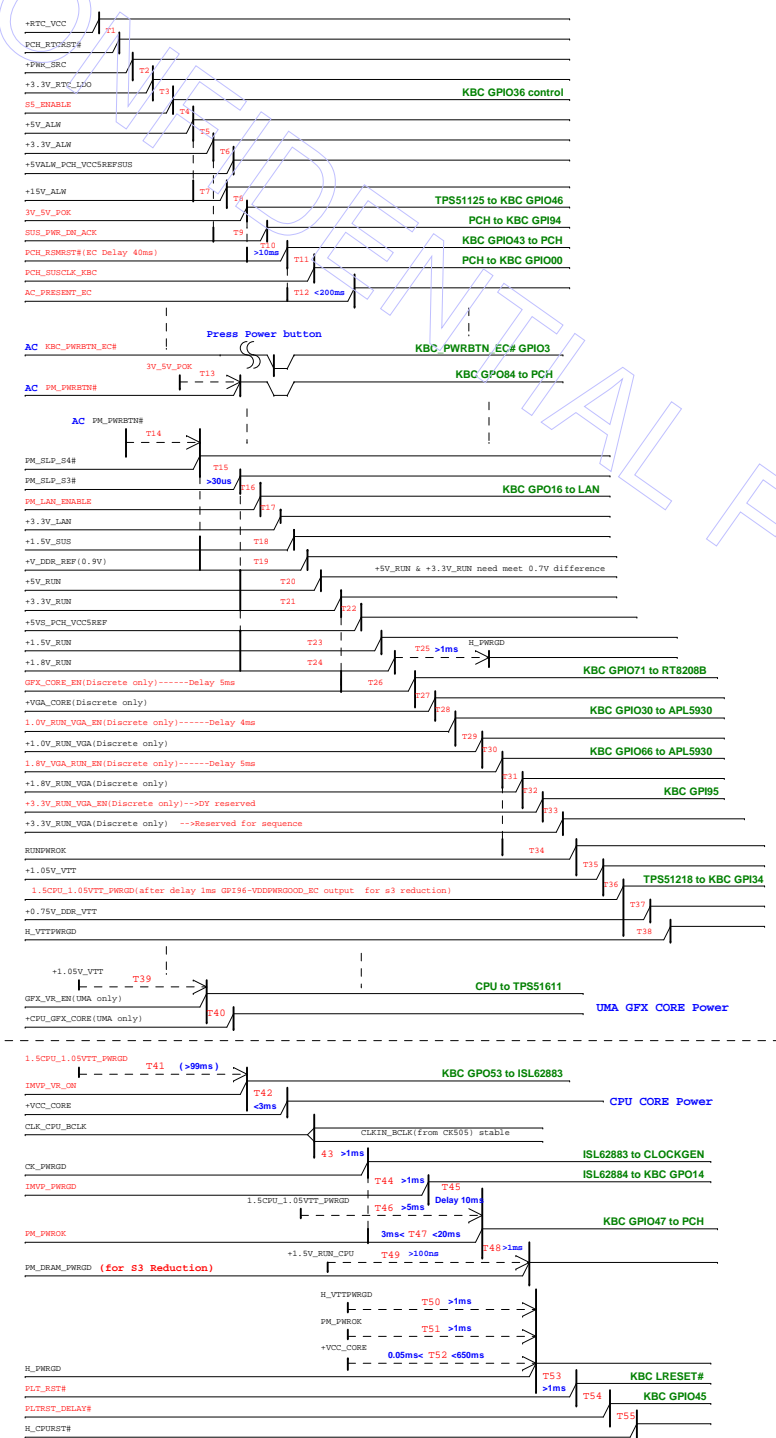
Power Sequence



Intel-Power Up Sequence

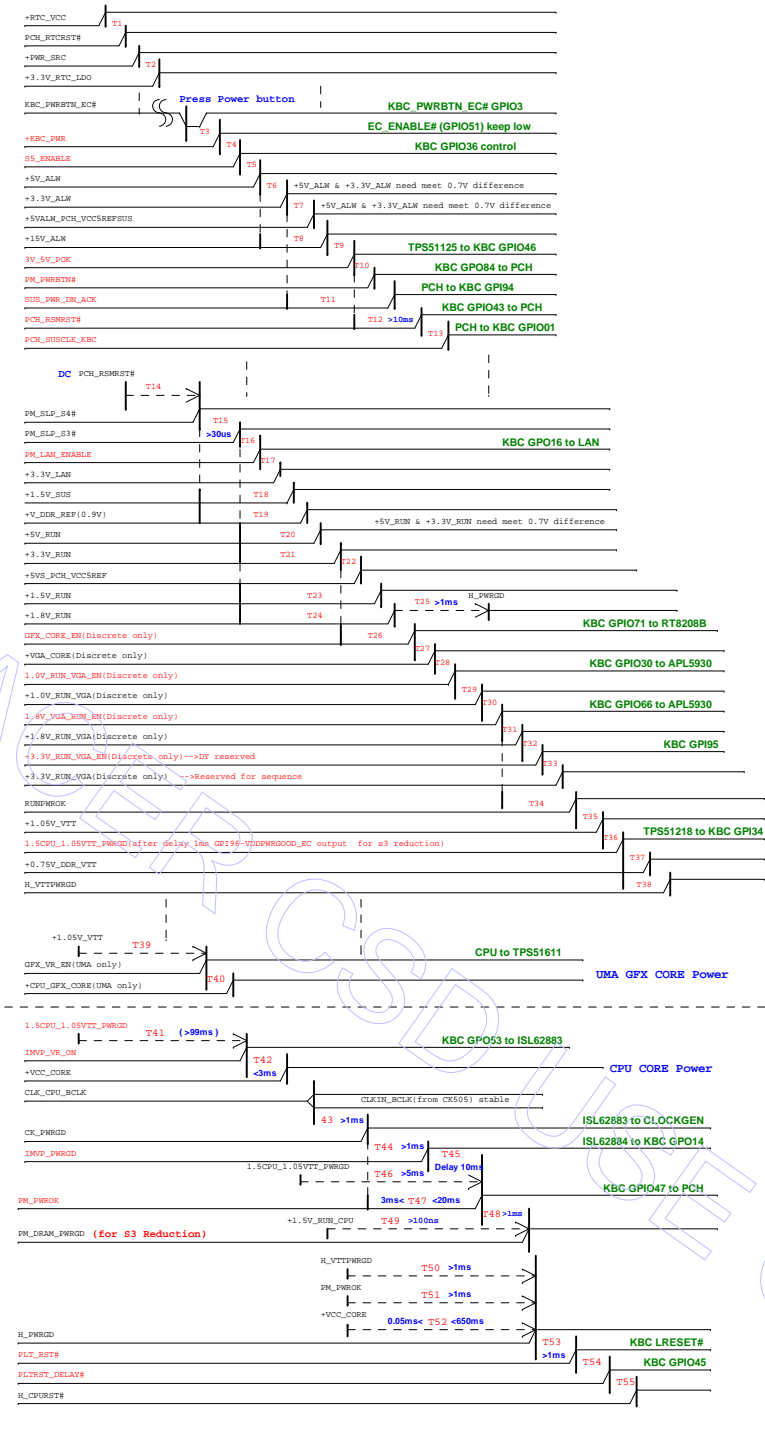
(AC mode)

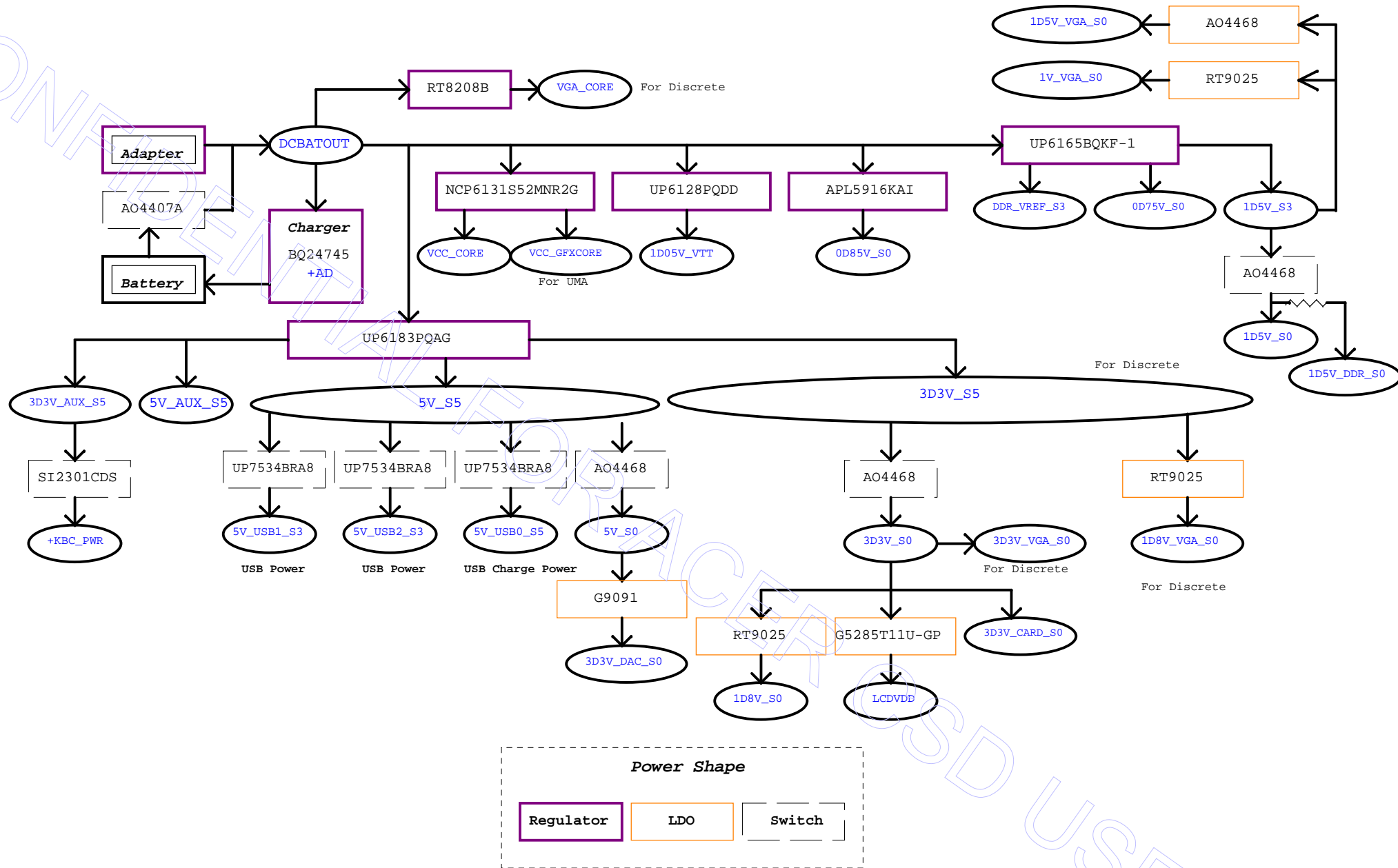
red word: KBC GPIO



(DC mode)

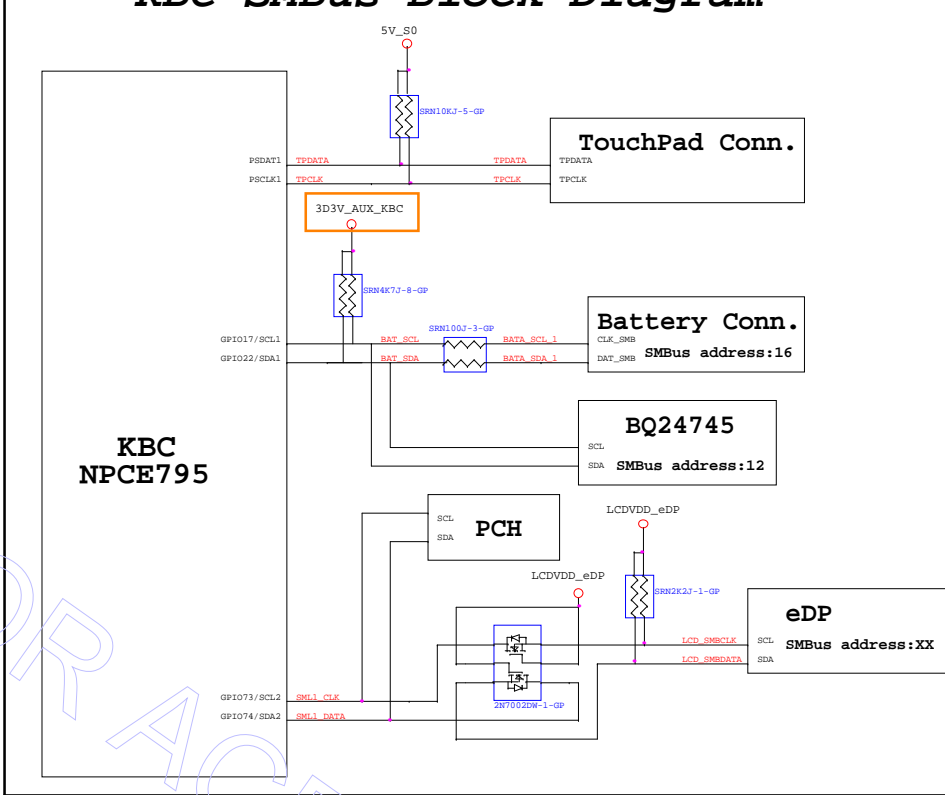
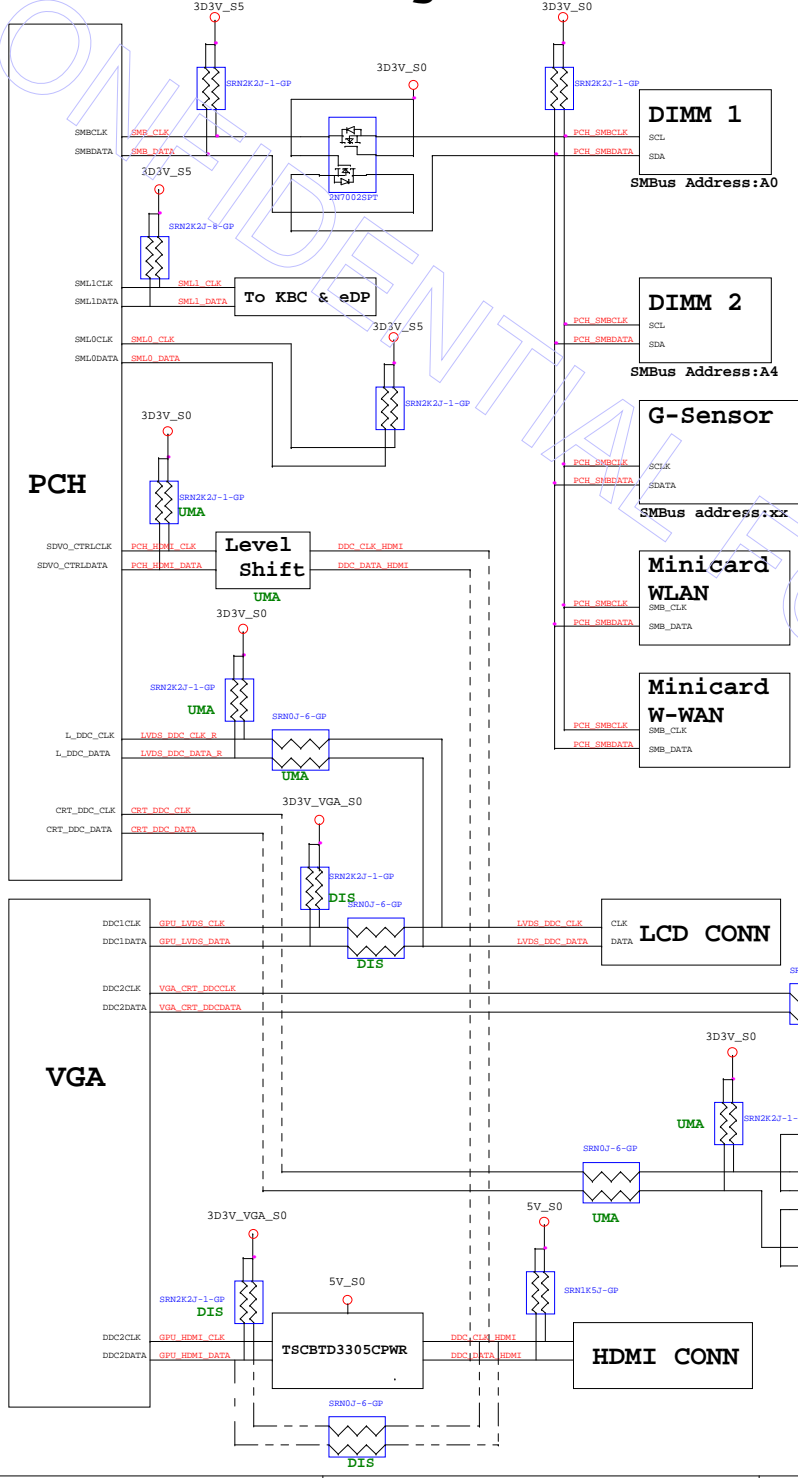
red word: KBC GPIO



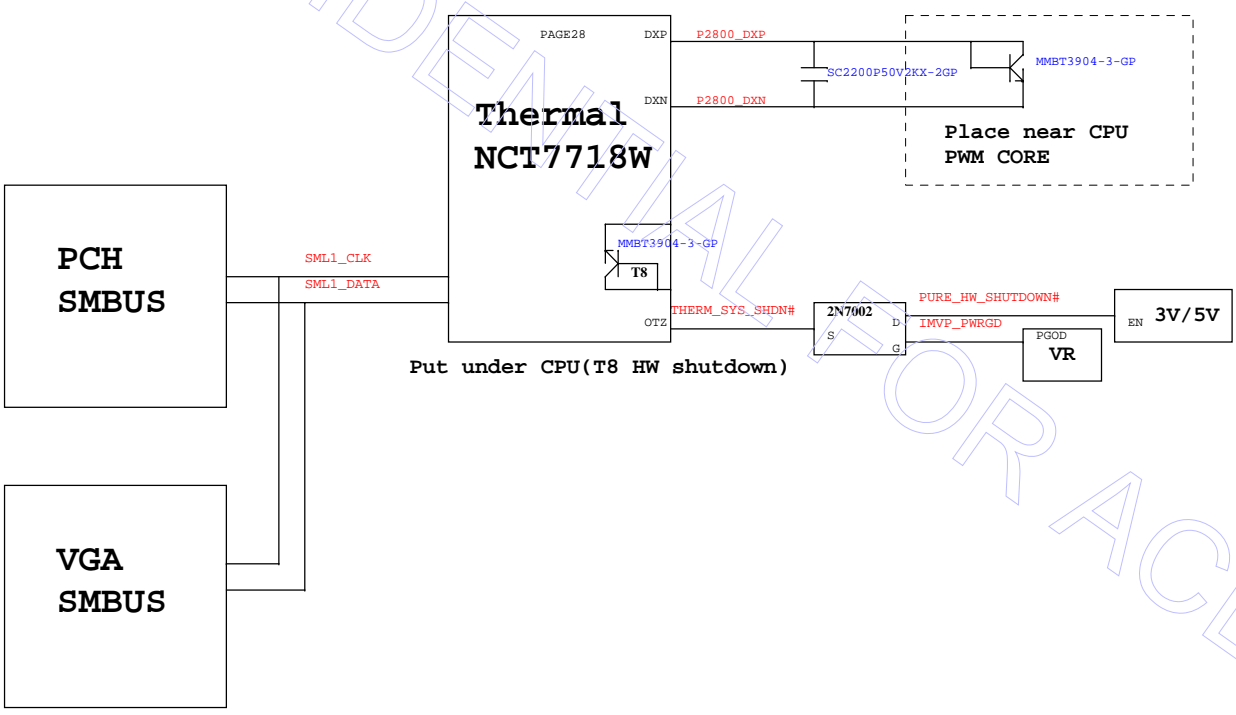


PCH SMBus Block Diagram

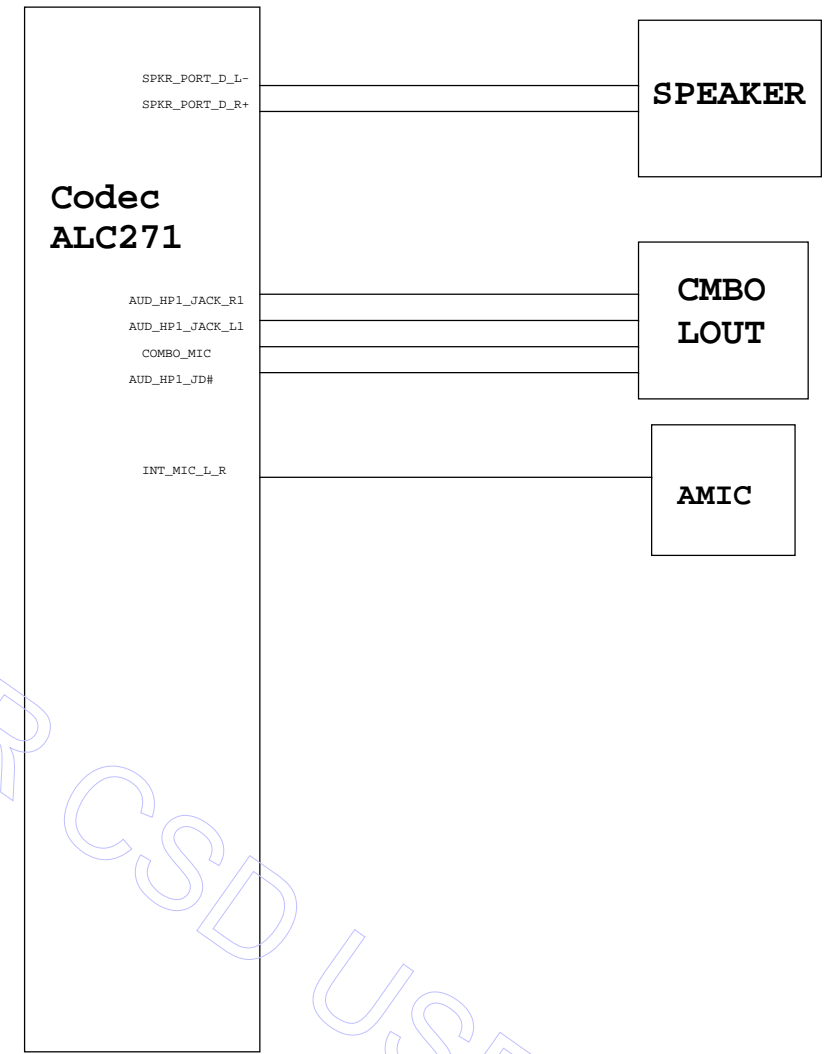
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Title			
USB charger			
Size	Document Number	Rev	
A3	Husk/Petra	-2	
Date:	Thursday, April 19, 2012	Sheet	103 of 103