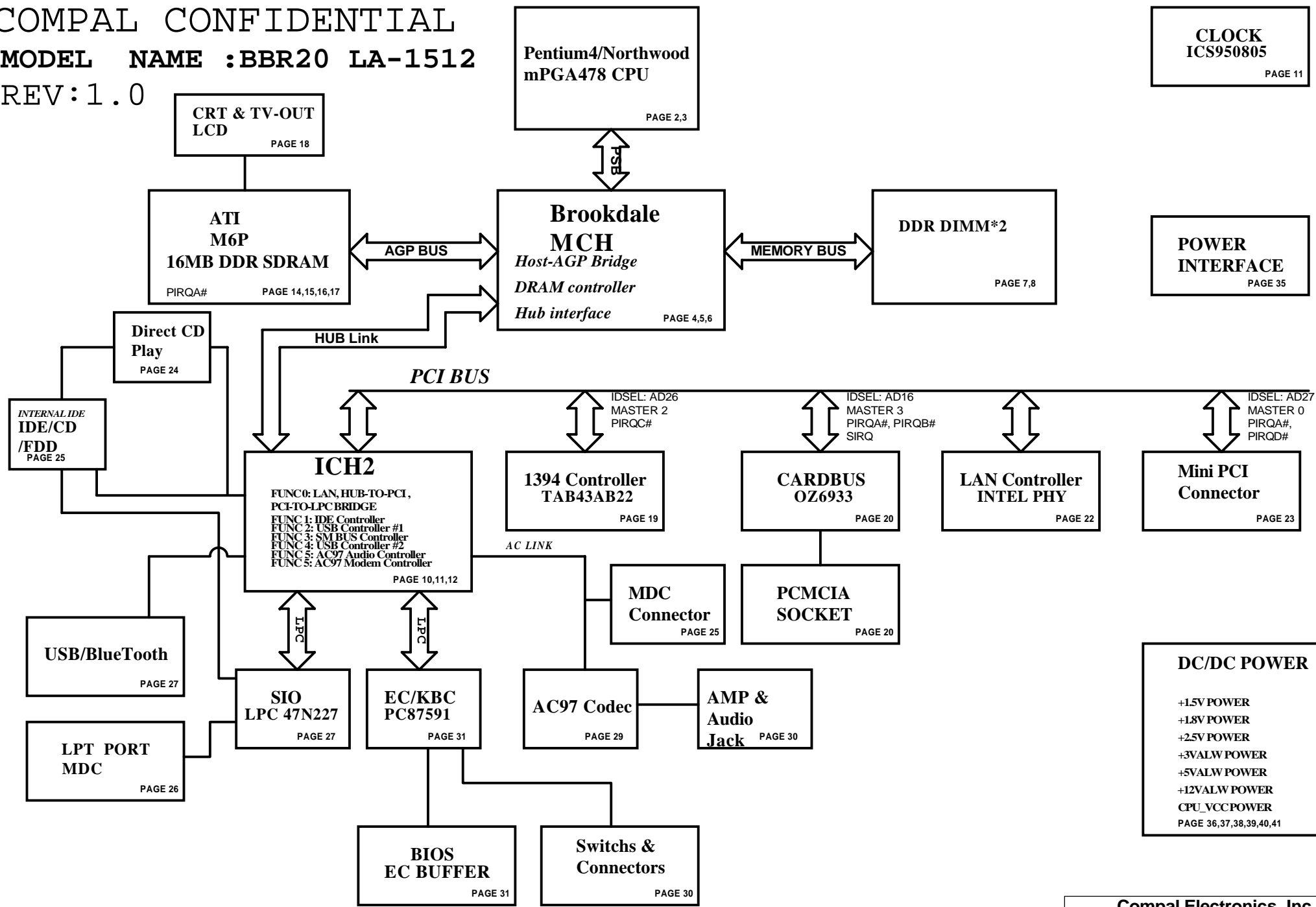
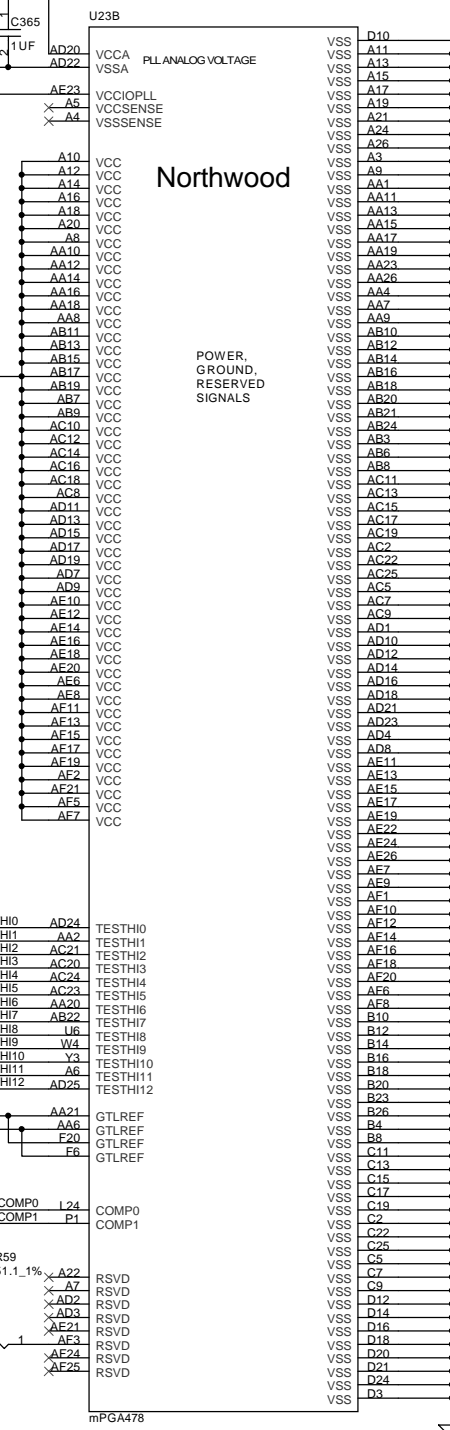
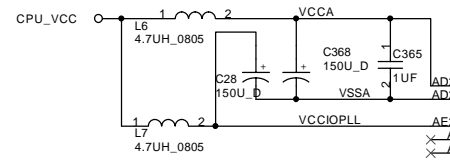


COMPAL CONFIDENTIAL
 MODEL NAME : BBR20 LA-1512
 REV: 1.0



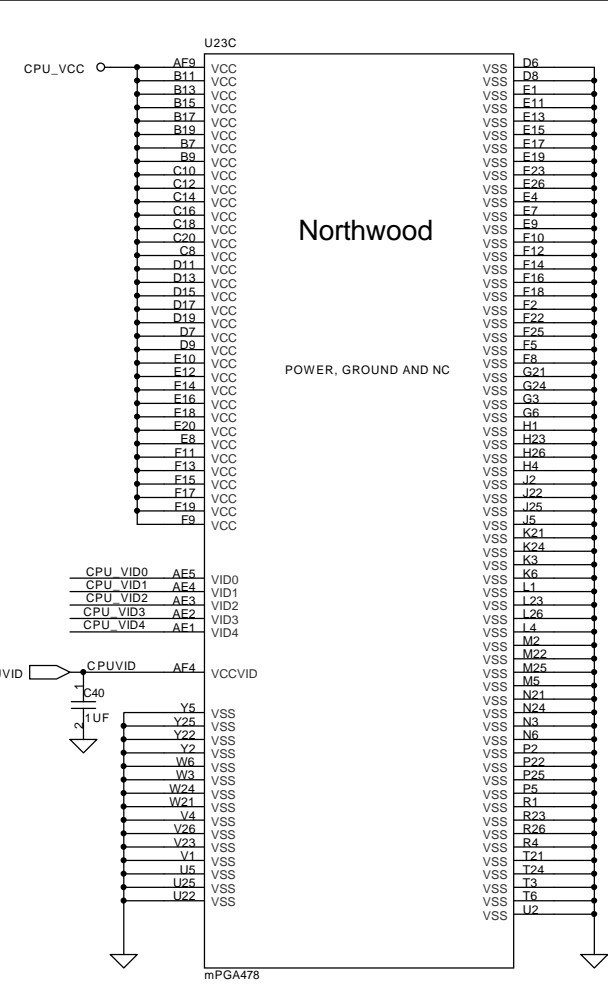
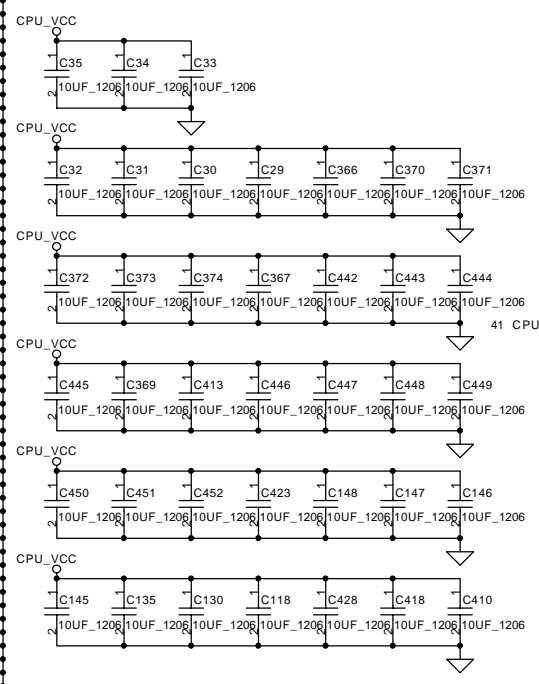
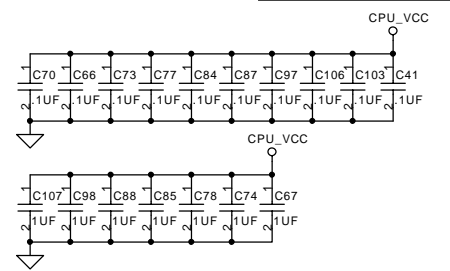
Compal Electronics, Inc.		
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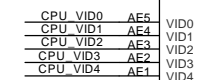
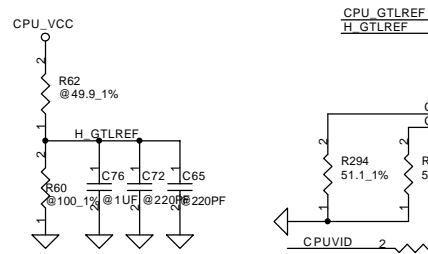
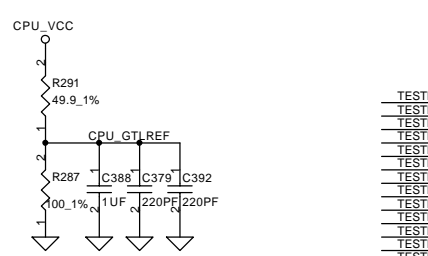
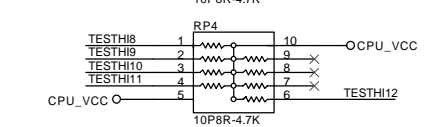
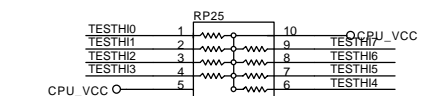
Northwood

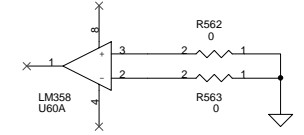
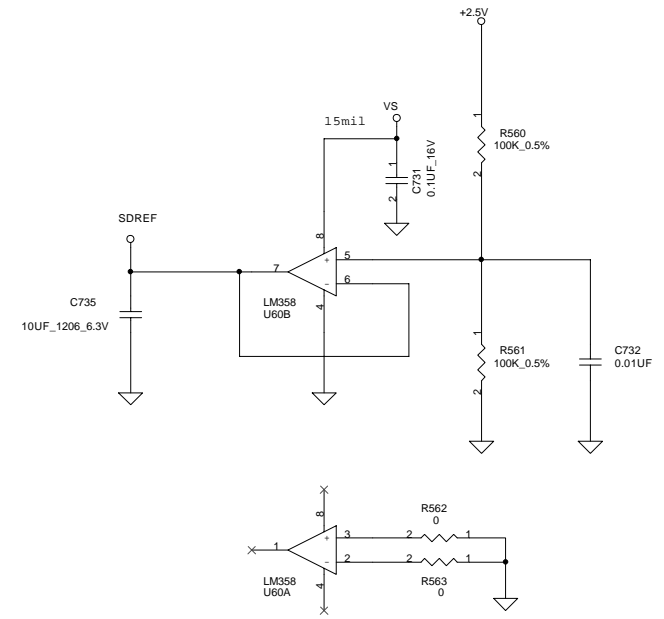
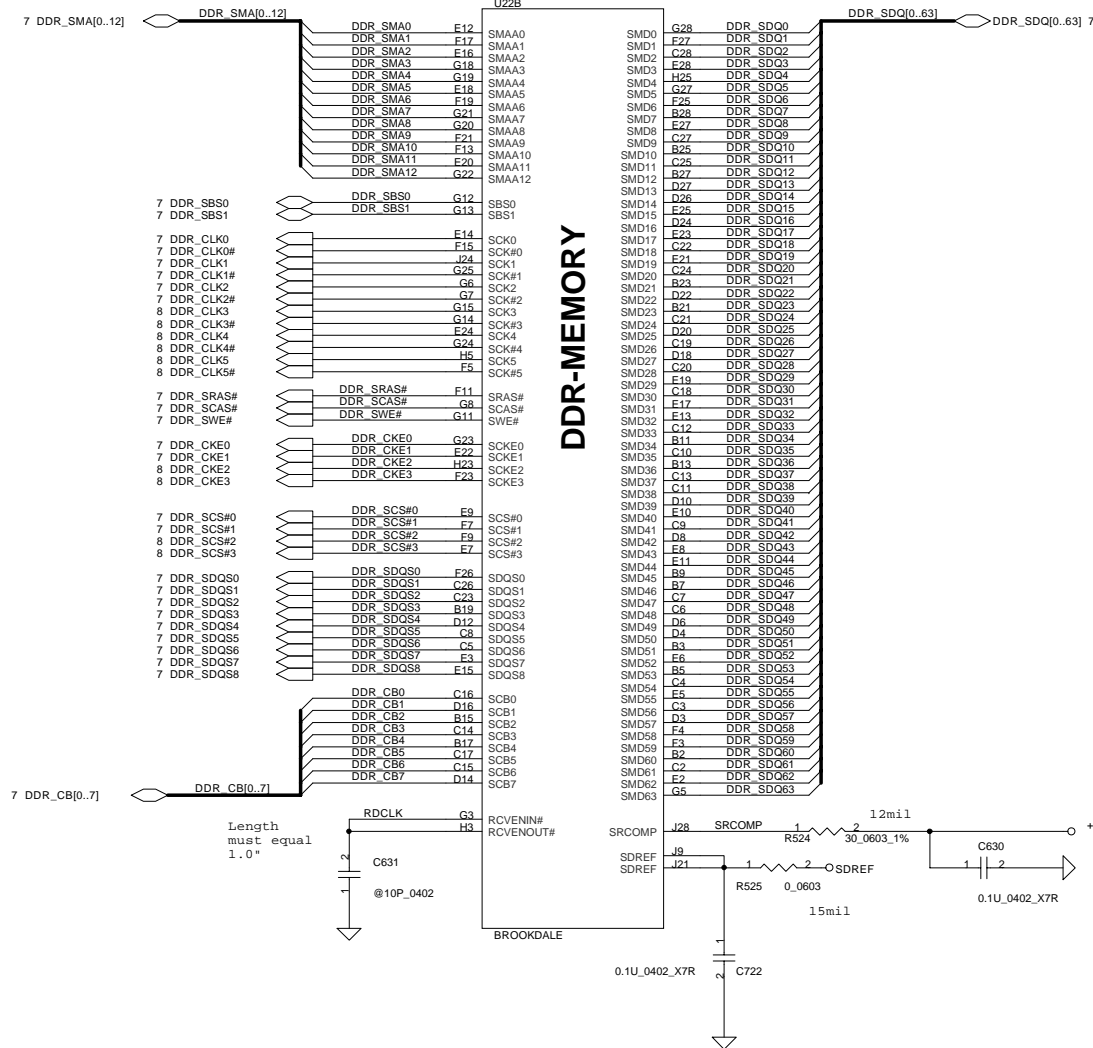
POWER, GROUND, RESERVED SIGNALS



Northwood

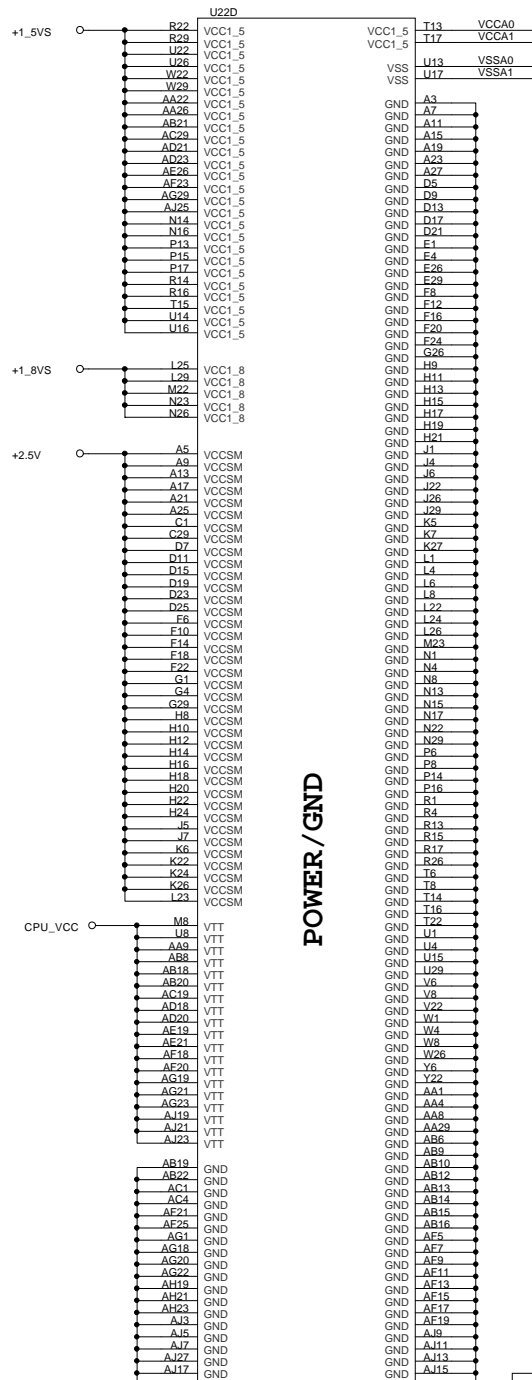
POWER, GROUND AND NC



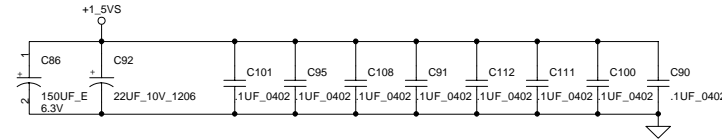
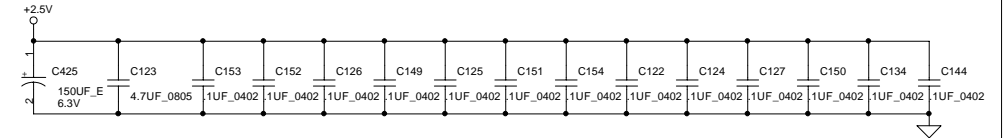
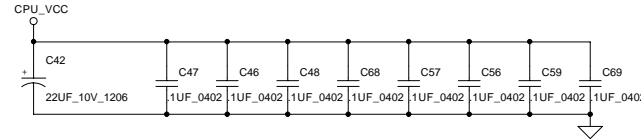
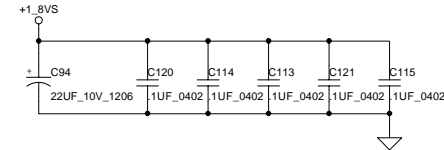
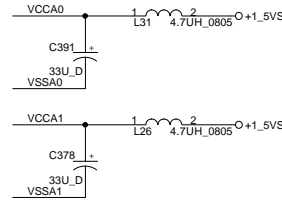


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POWER / GND

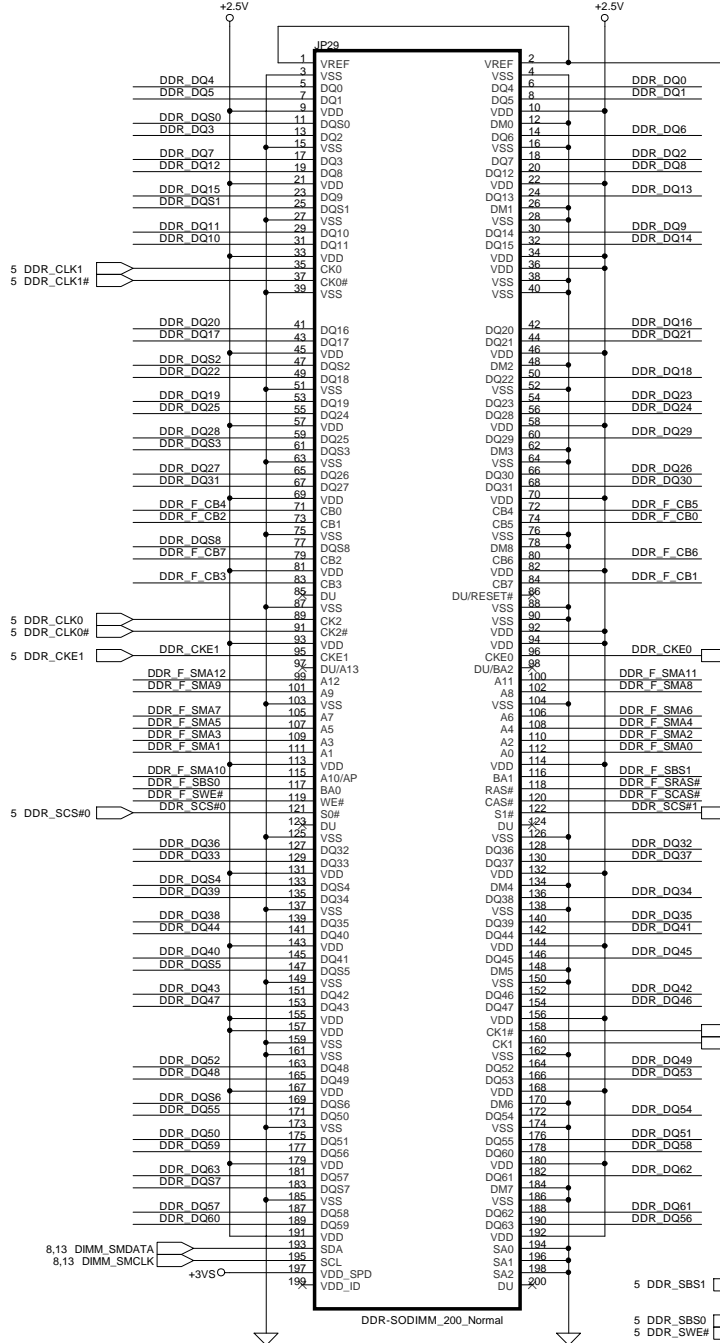
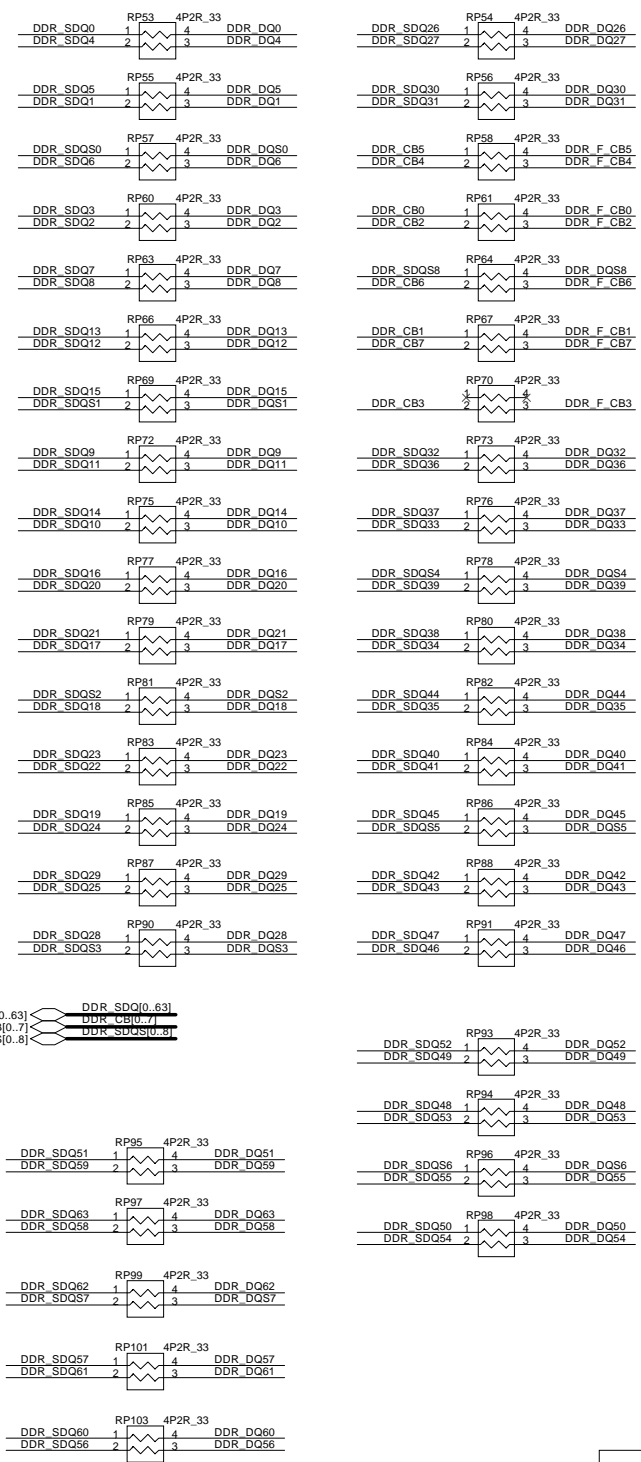


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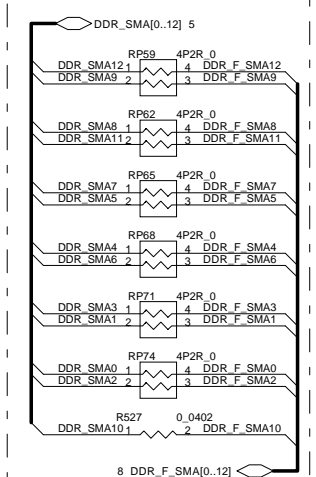
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Layout note

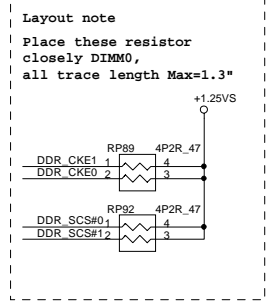
Place these resistor closely DIMMO, all trace length<750mil



DIMMO (STD)
Top side



Layout note
Place these resistor closely DIMMO, all trace length<=750mil



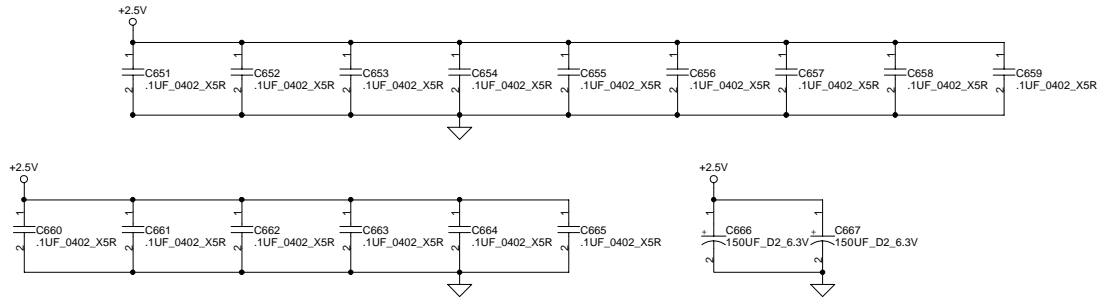
Layout note
Place these resistor closely DIMMO, all trace length<=750mil

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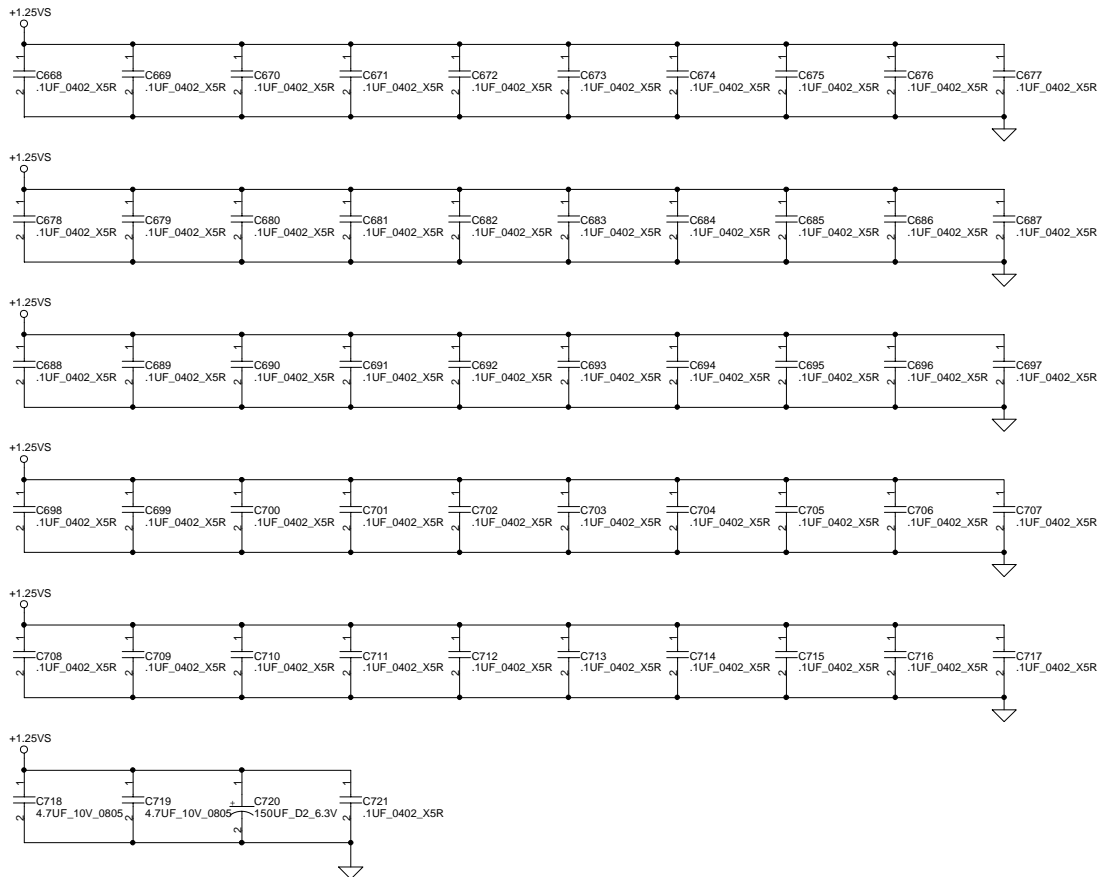
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V

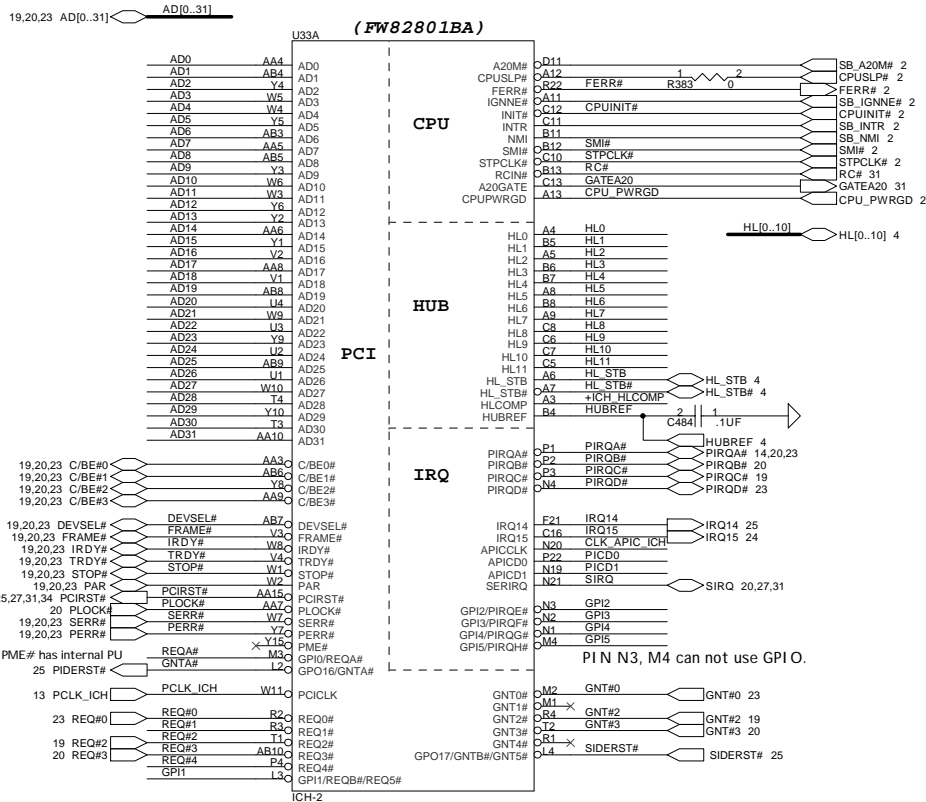


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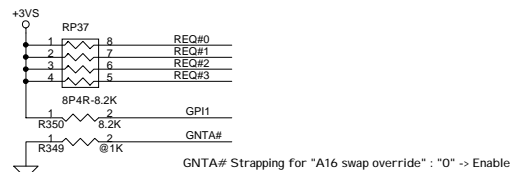
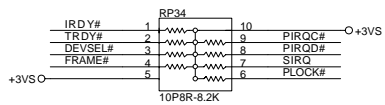
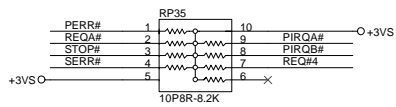
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ICH-2

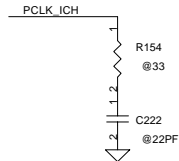
(FW82801BA)



PCI Pullups



REQ#	Assignment
REQ#0	WLAN
REQ#1	NC
REQ#2	1394
REQ#3	PCMCIA CONTROLLER
REQ#4	NC

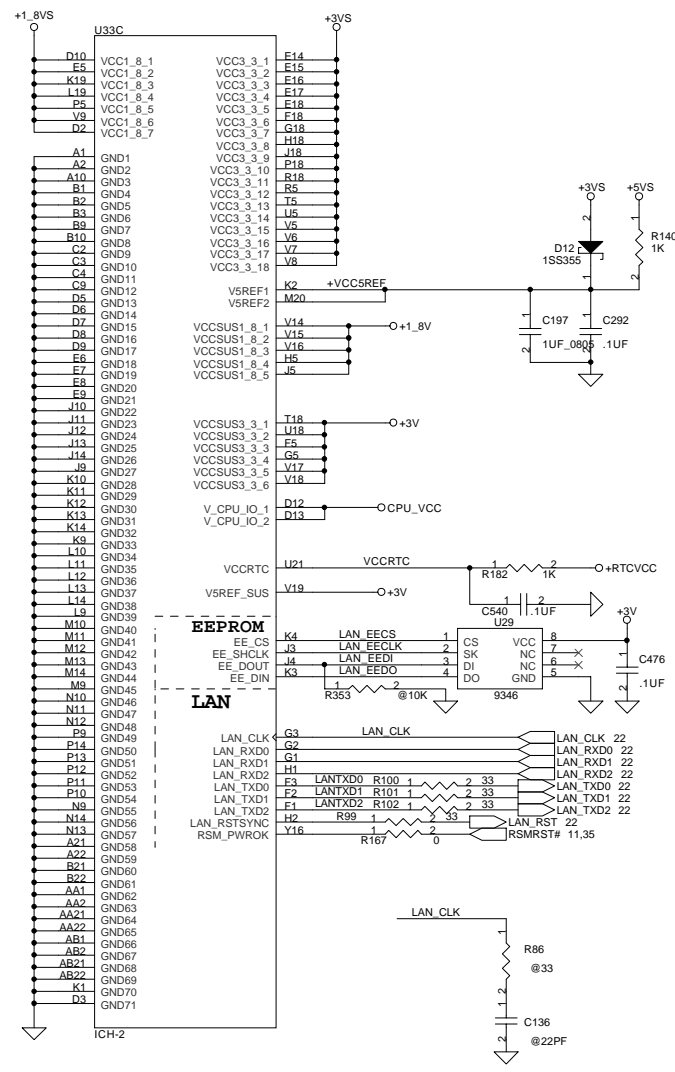
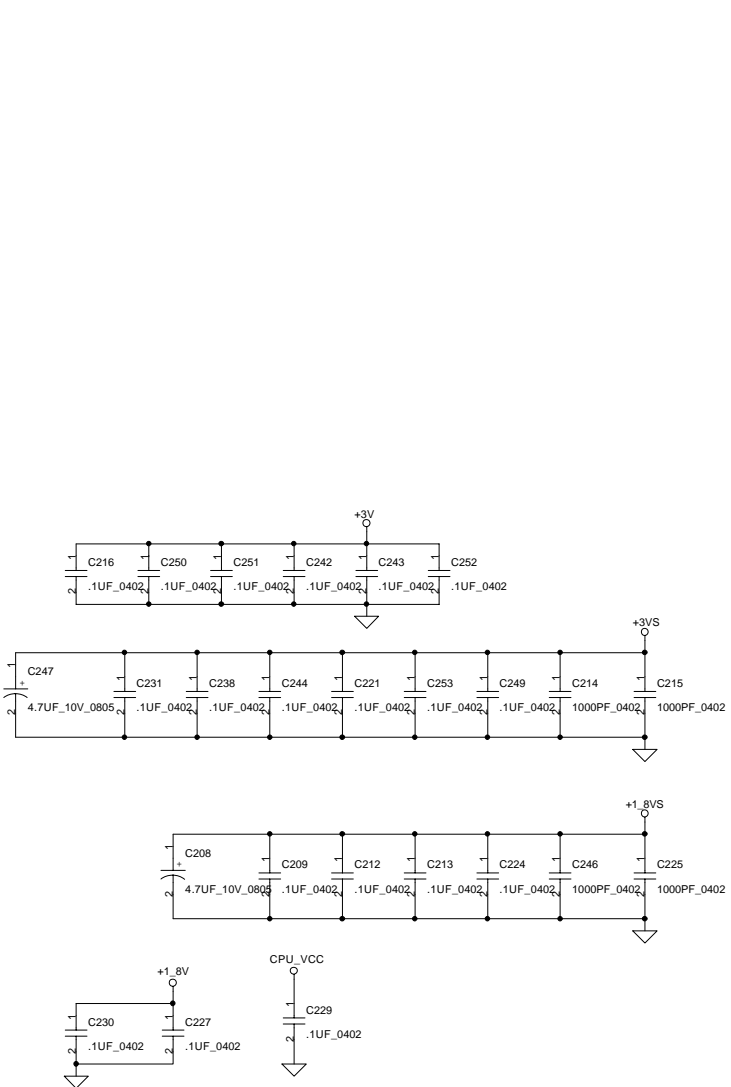


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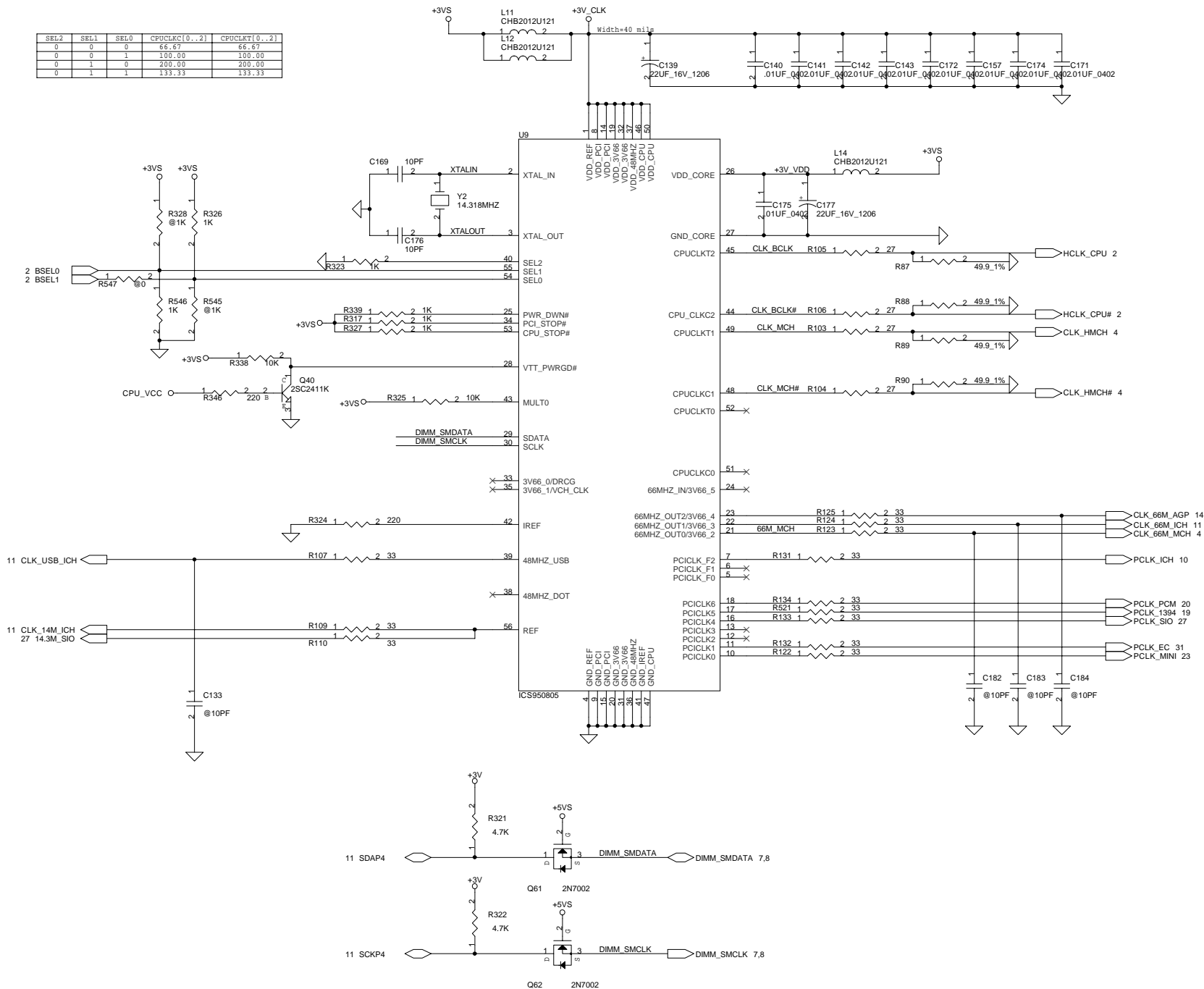
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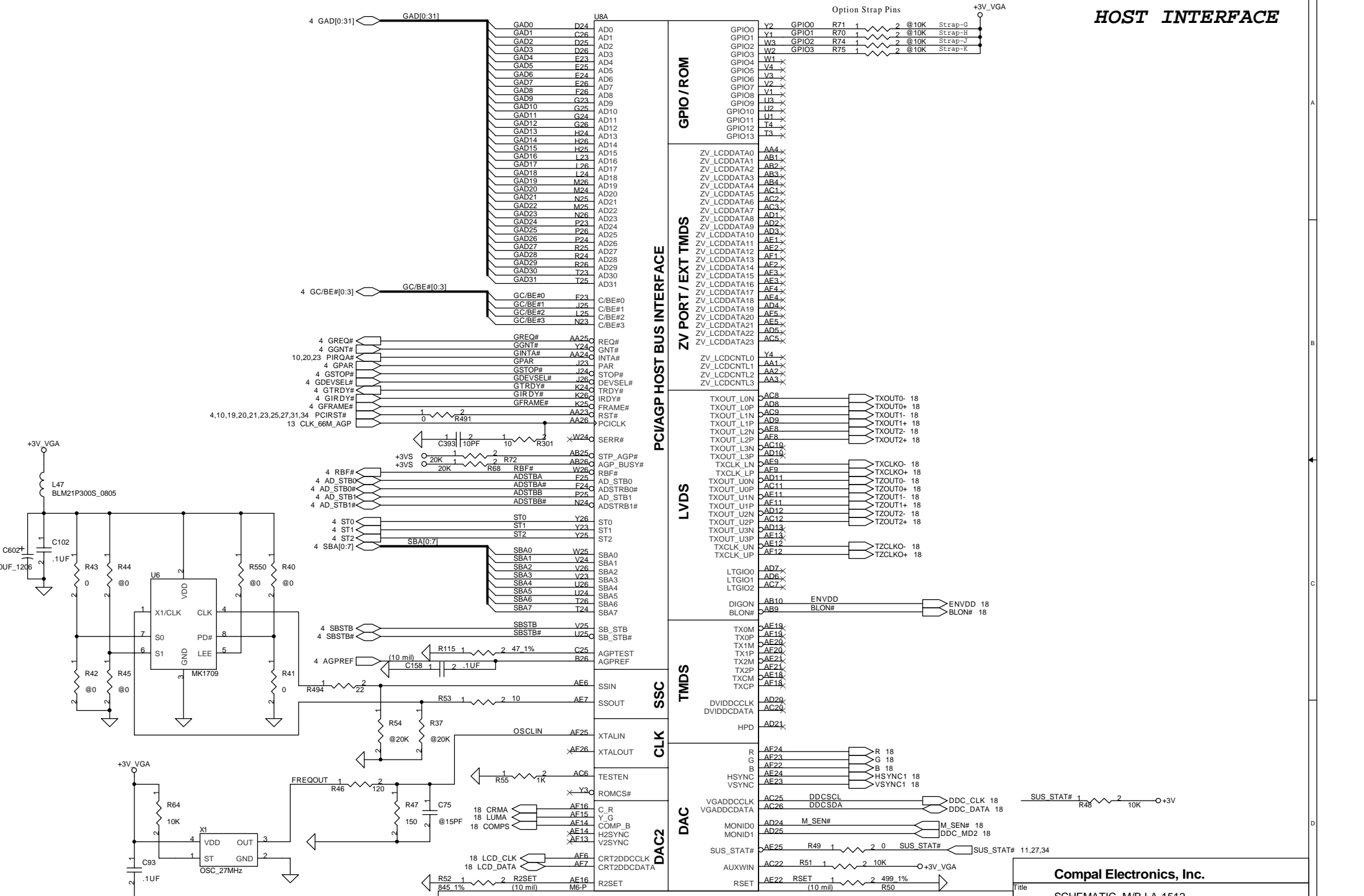
SEL2	SEL1	SEL0	CPUCLK[0..2]	CPUCLK1[0..2]
0	0	0	56.57	56.57
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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HOST INTERFACE

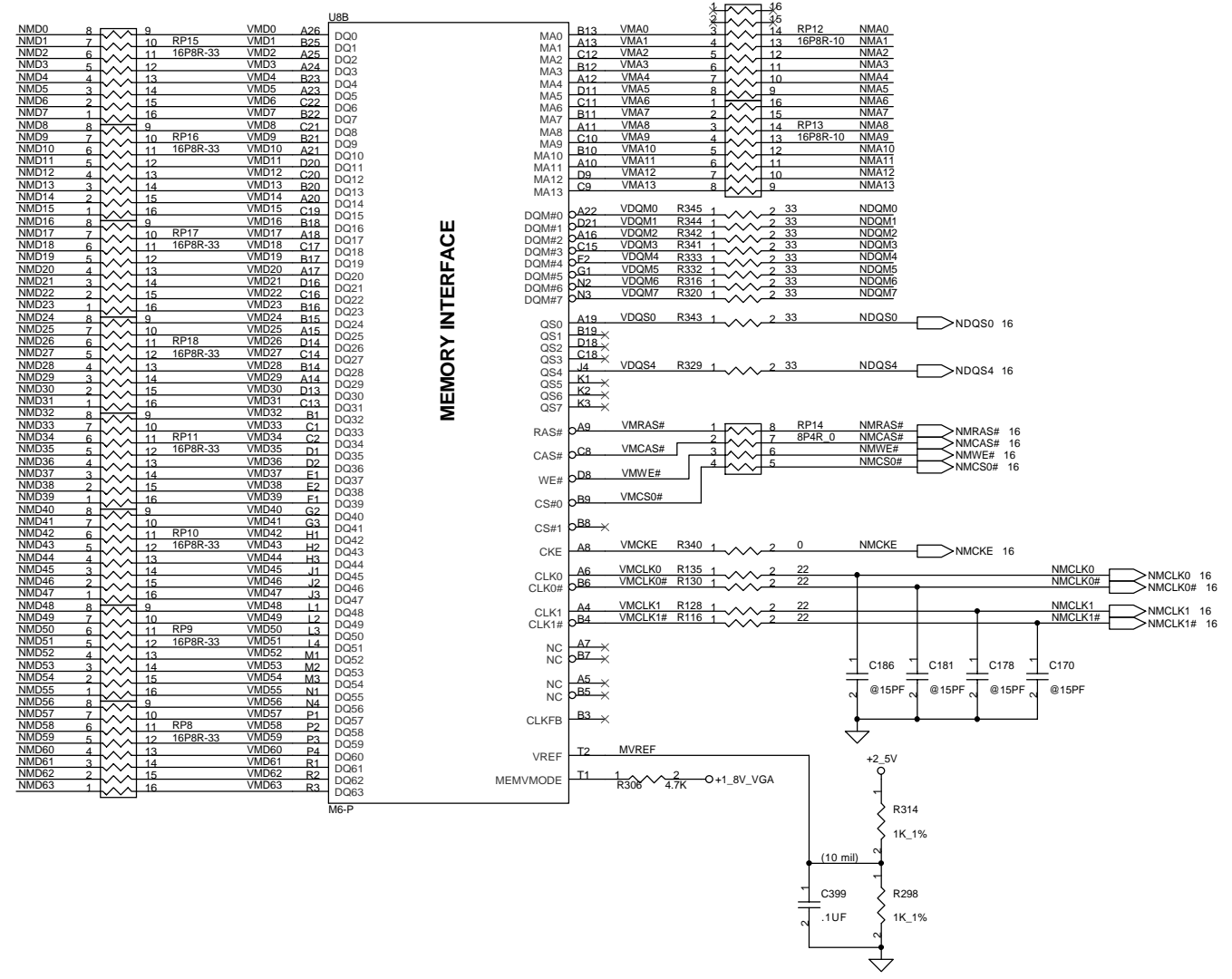
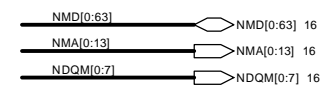


Divider circuit for 1.8Vdc XTALIN from 3.3Vdc OSC out

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MEMORY INTERFACE



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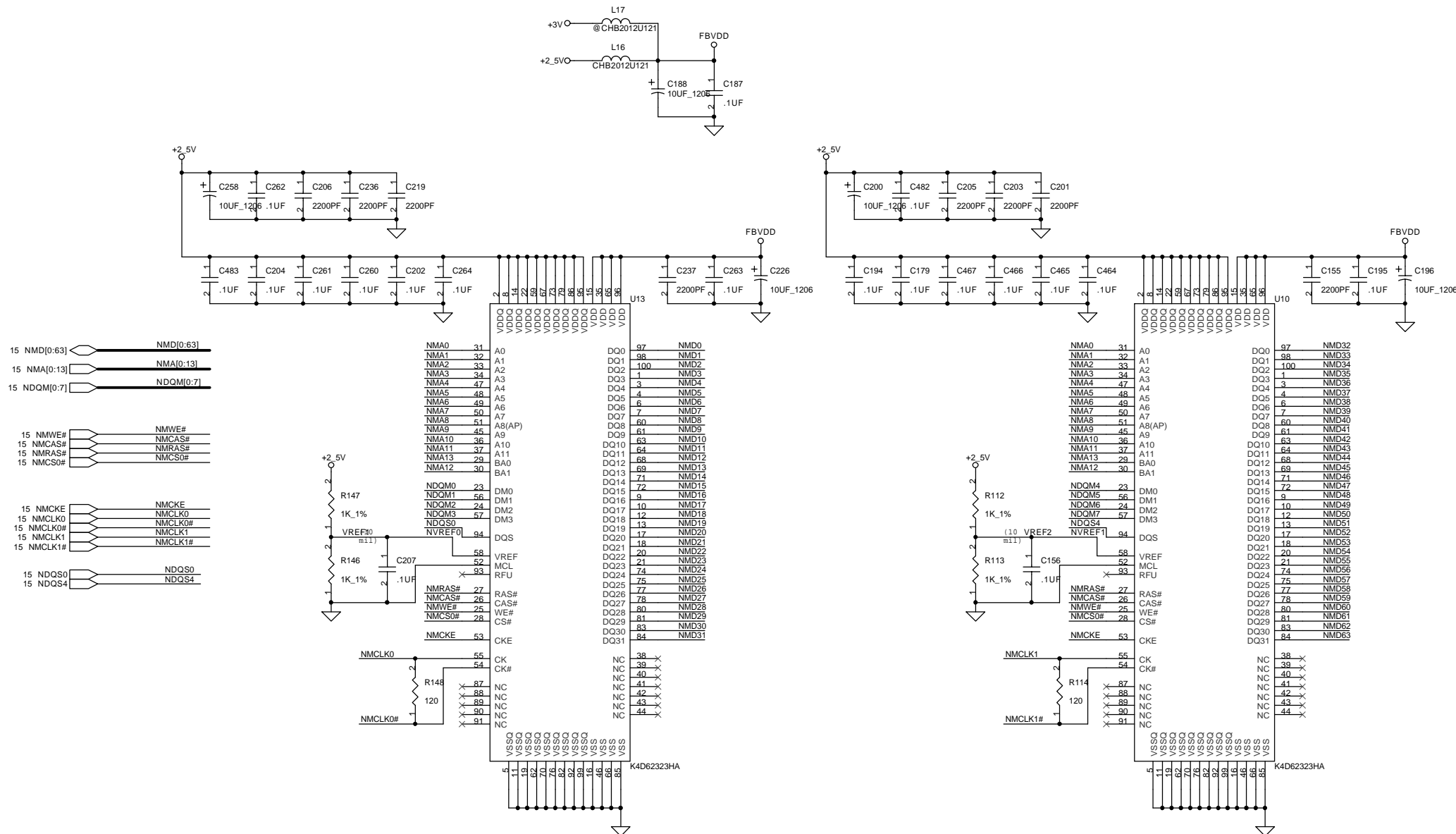
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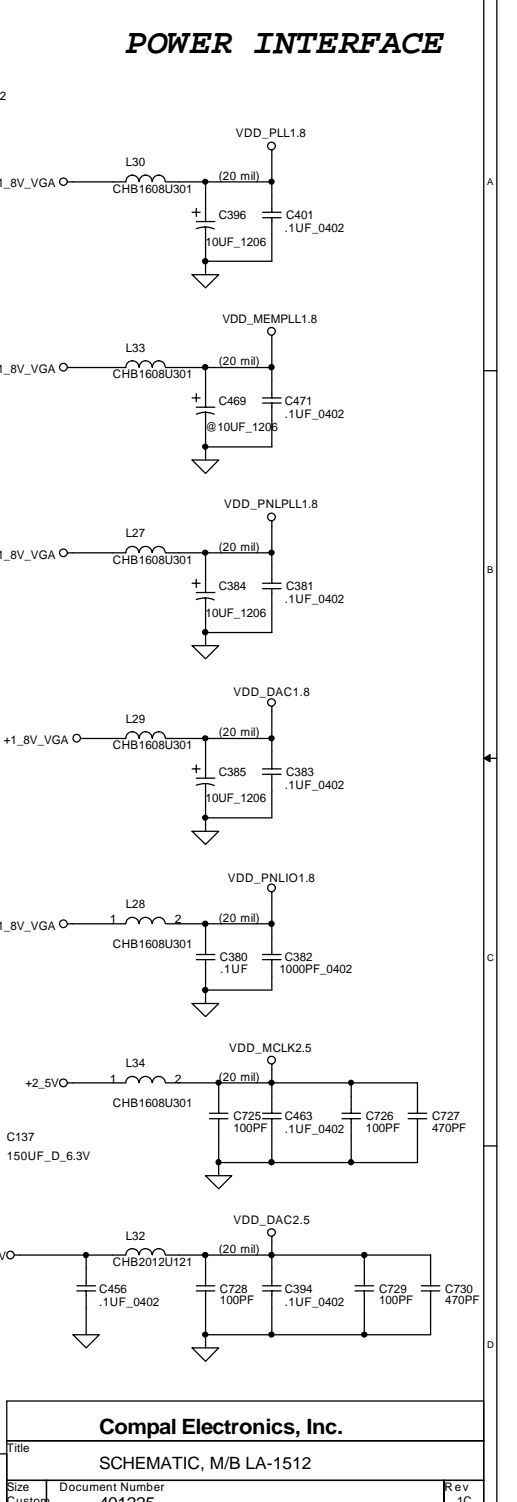
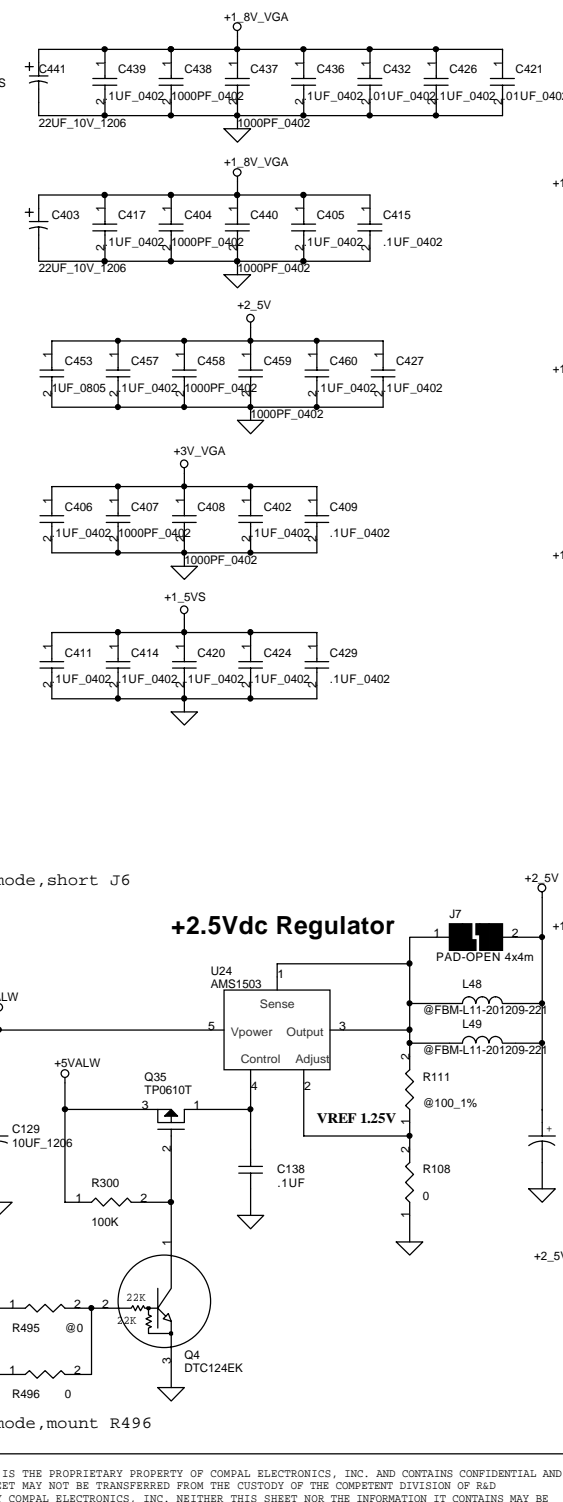
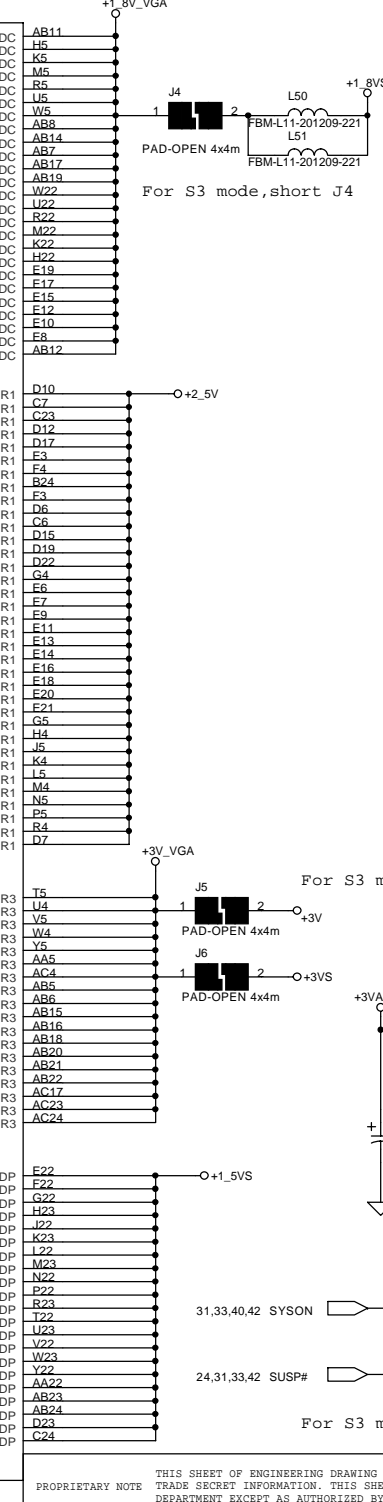
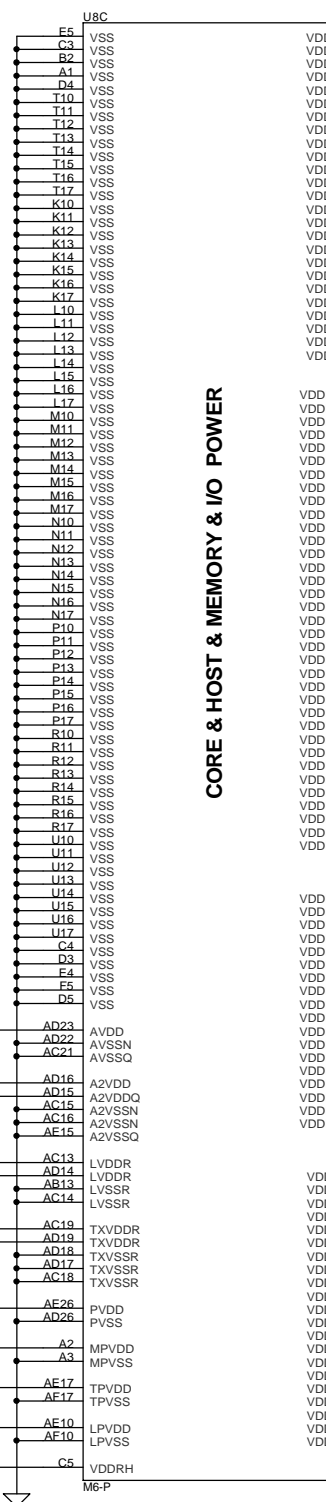
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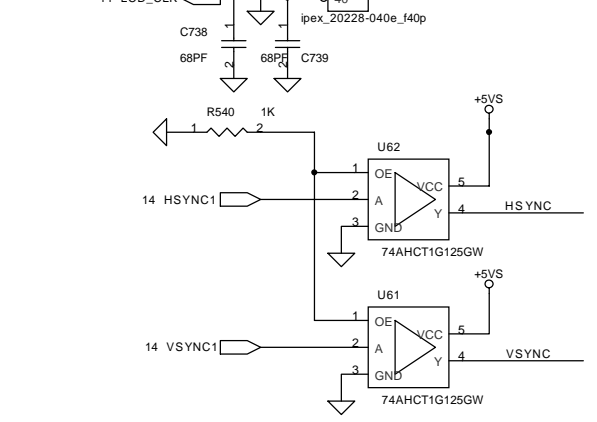
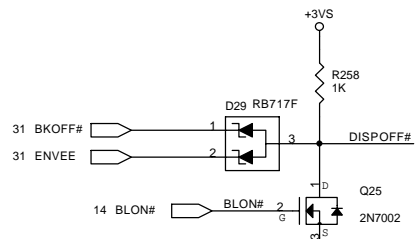
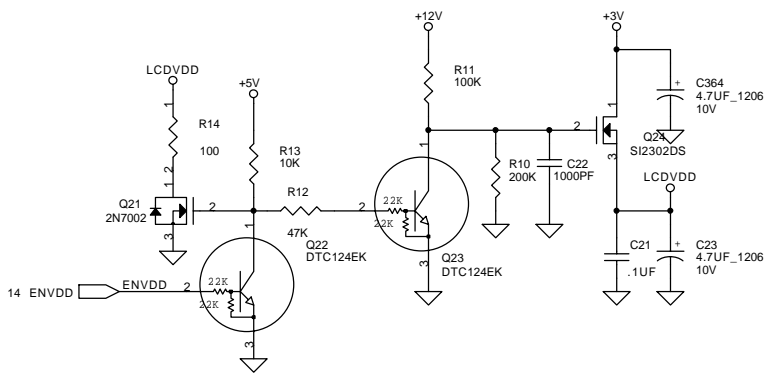
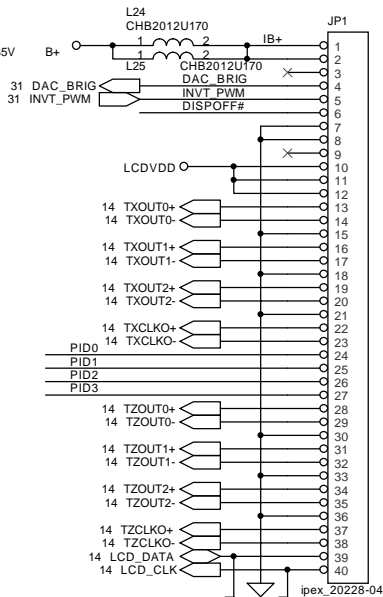
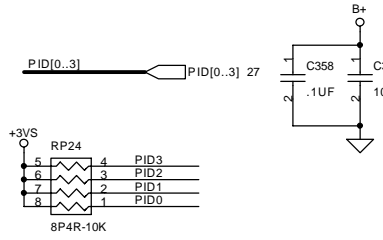
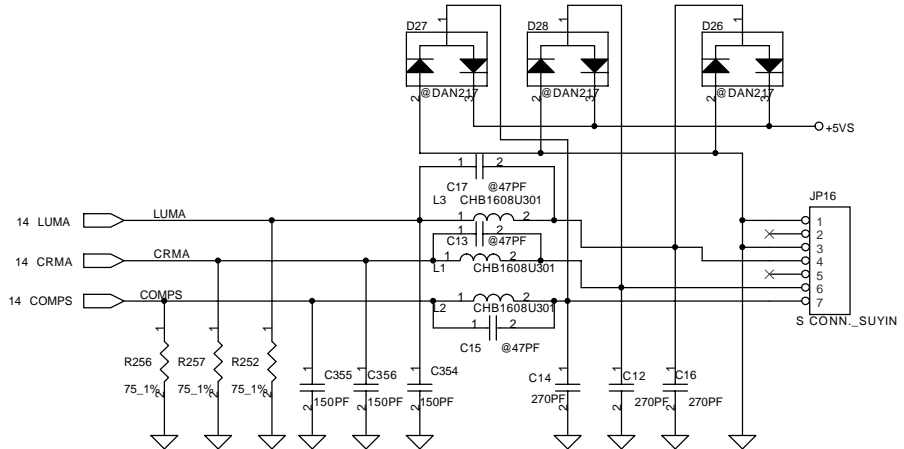
POWER INTERFACE

CORE & HOST & MEMORY & I/O POWER

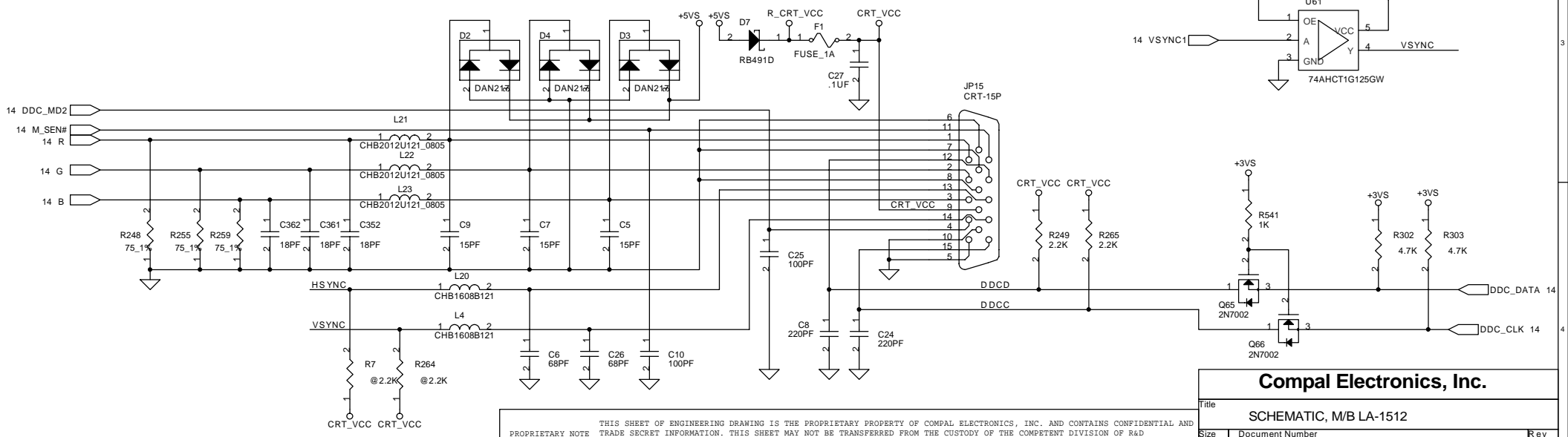


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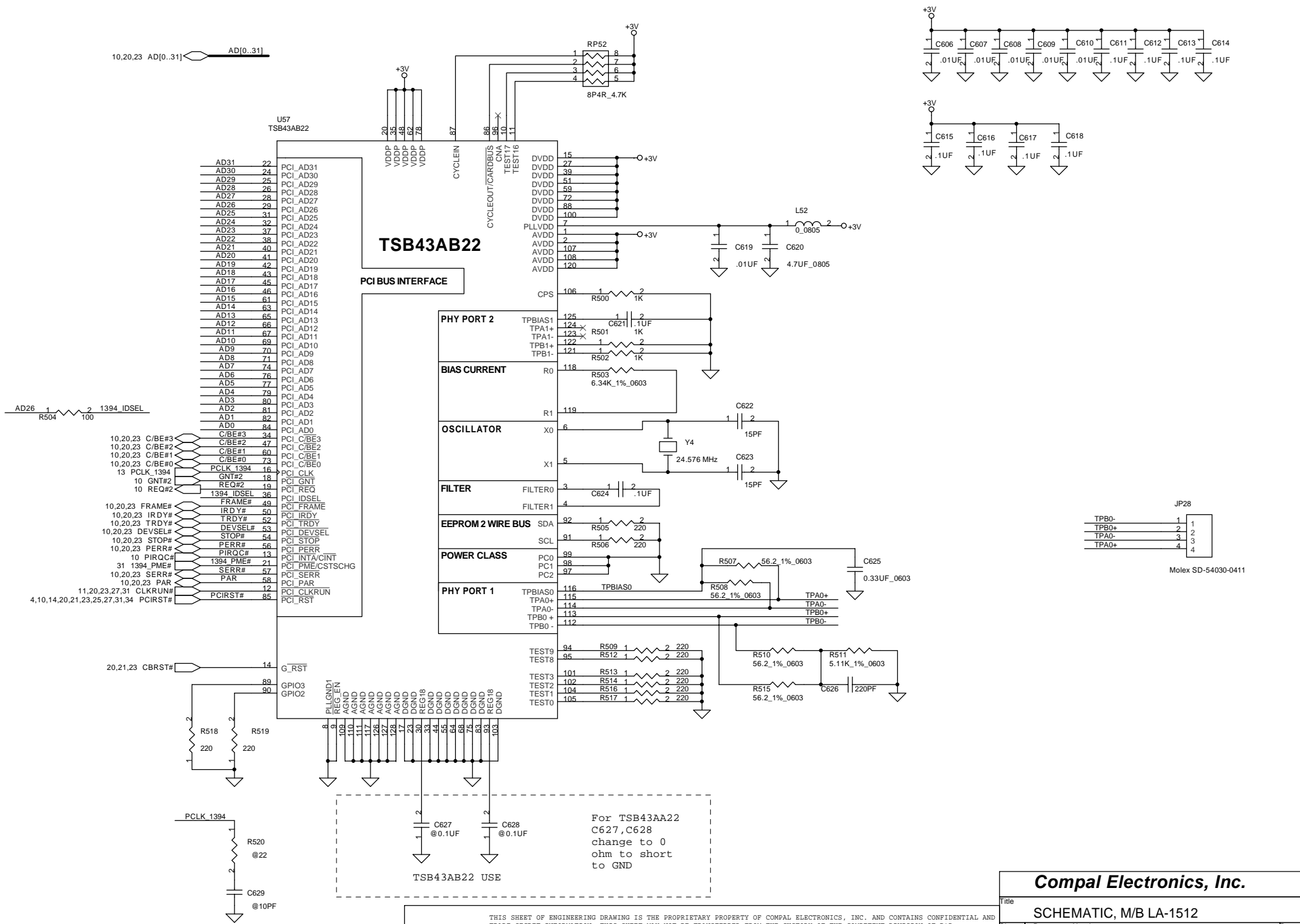


CRT Connector



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TSB43AB22

PCI BUS INTERFACE

PHY PORT 2

BIAS CURRENT

OSCILLATOR

FILTER

EEPROM 2 WIRE BUS

POWER CLASS

PHY PORT 1

For TSB43AA22
C627, C628
change to 0
ohm to short
to GND

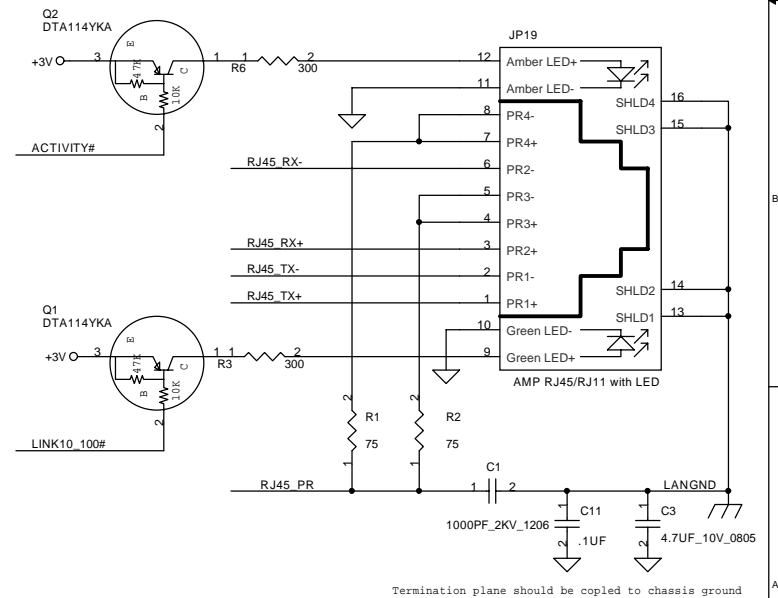
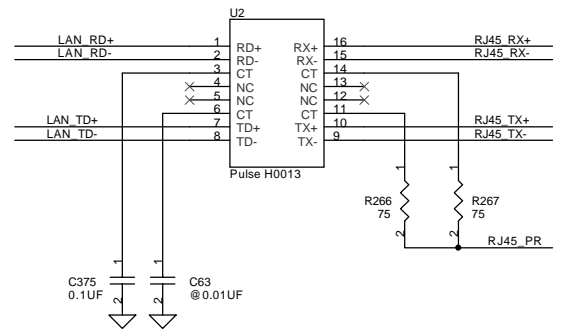
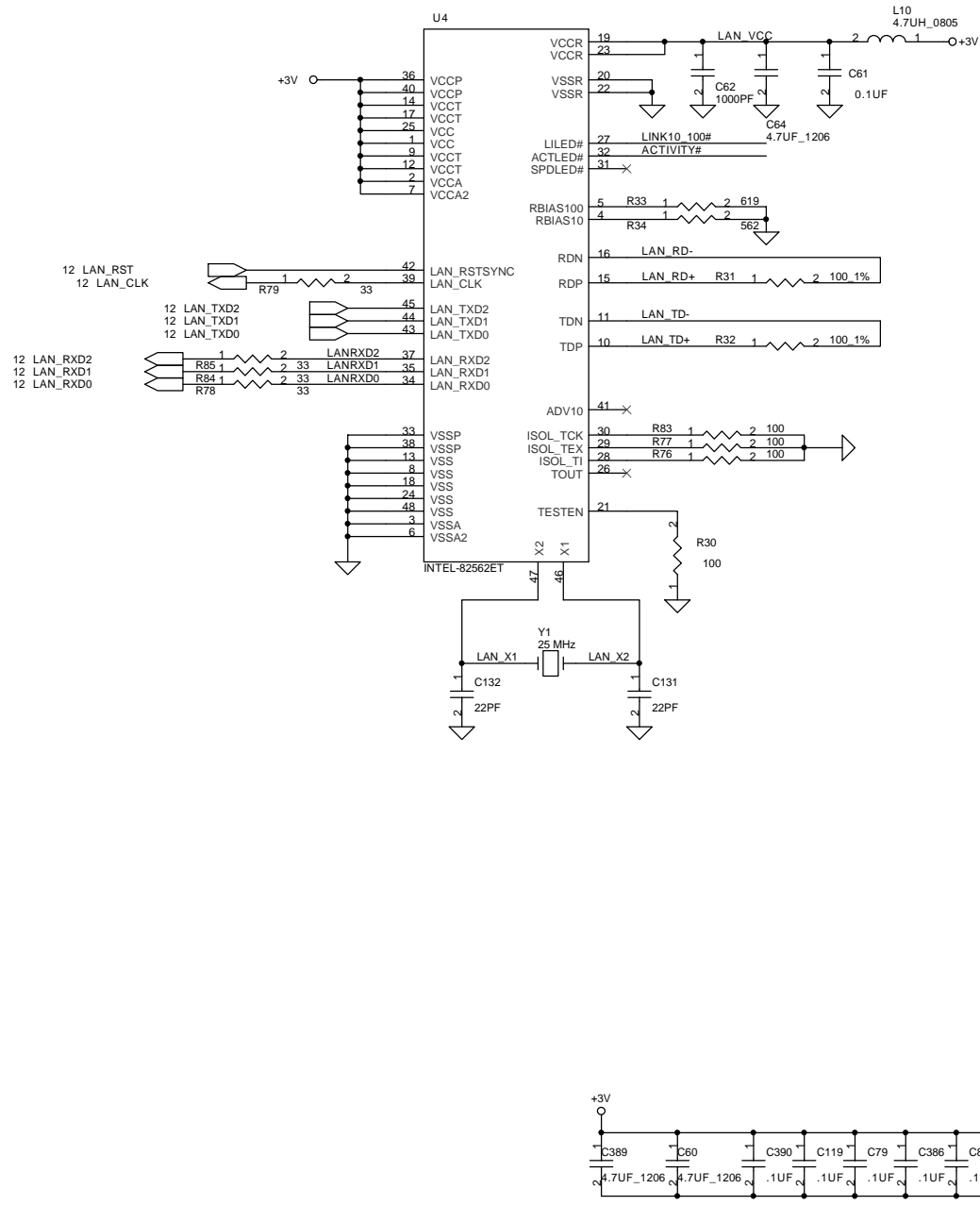
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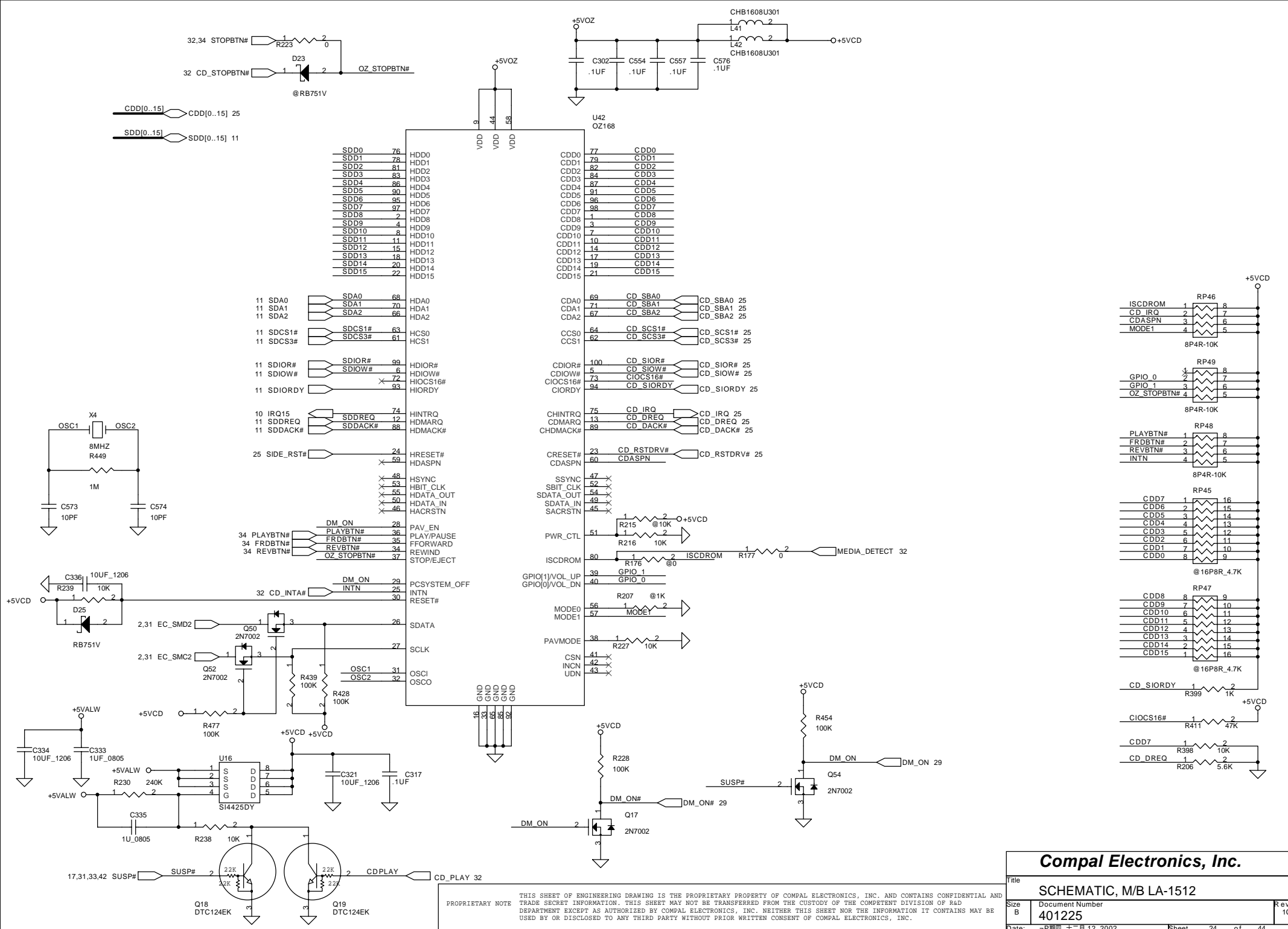
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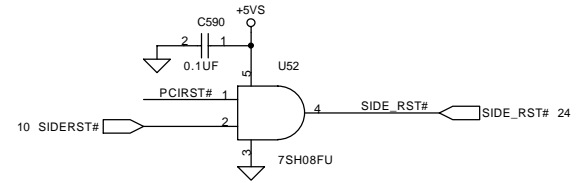
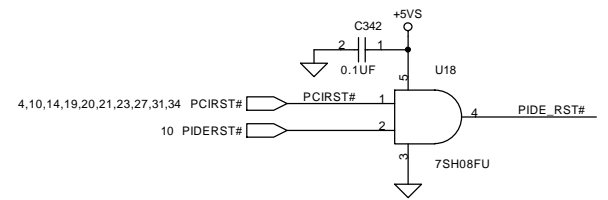
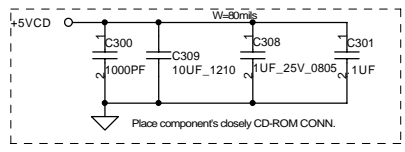
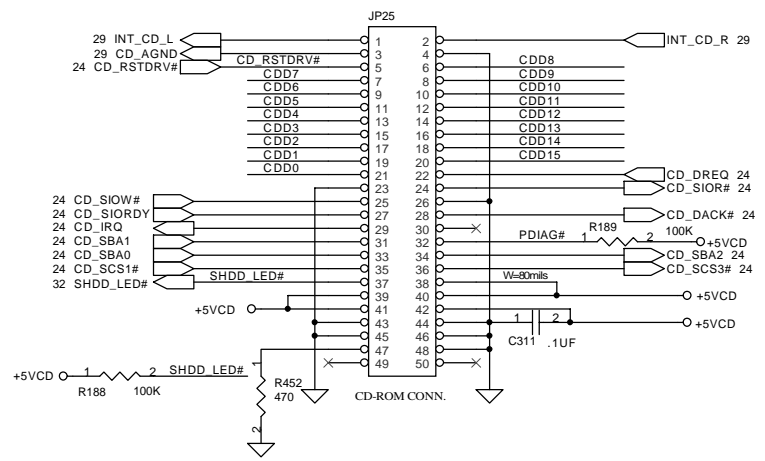
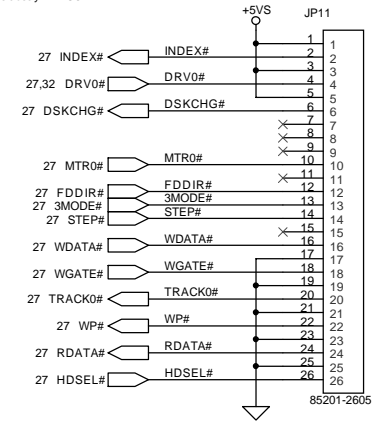
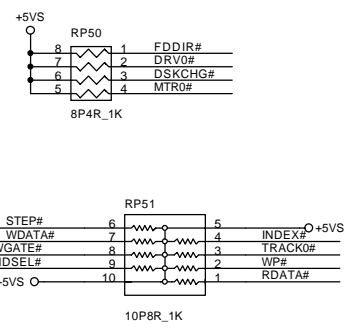
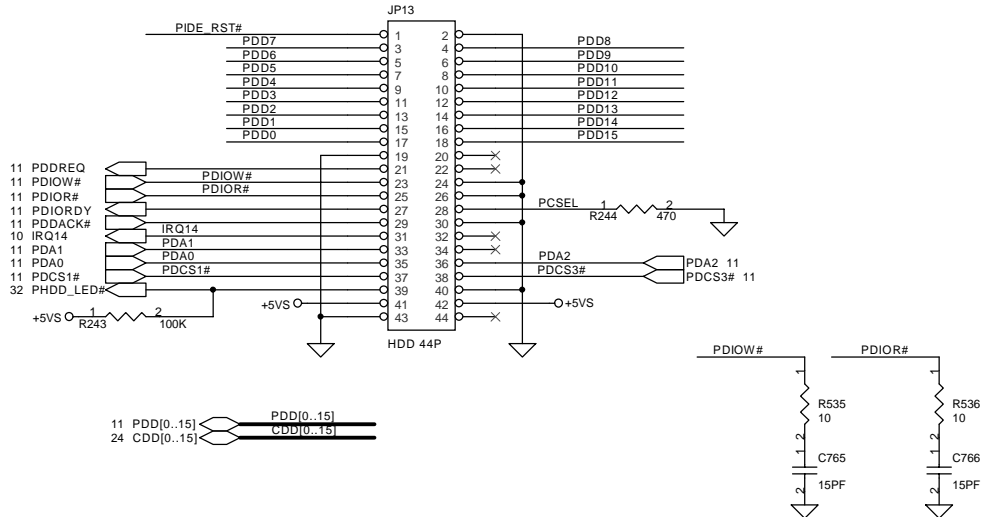
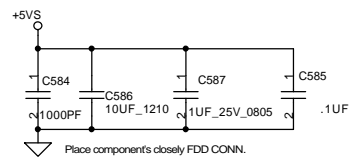
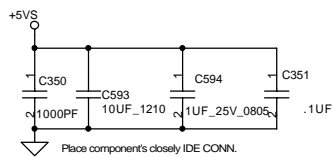
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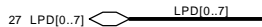
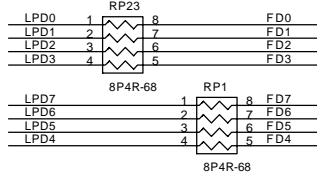
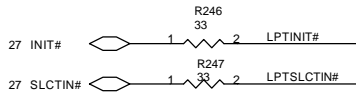
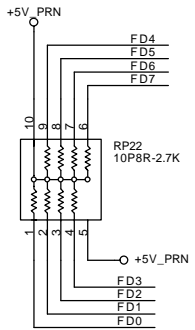
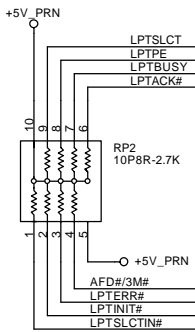
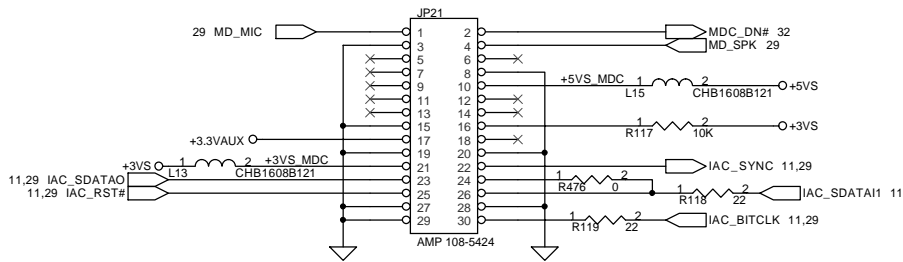


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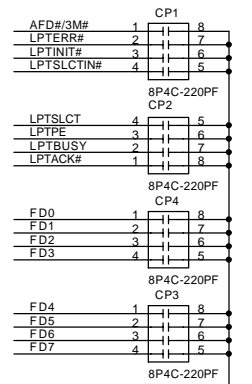
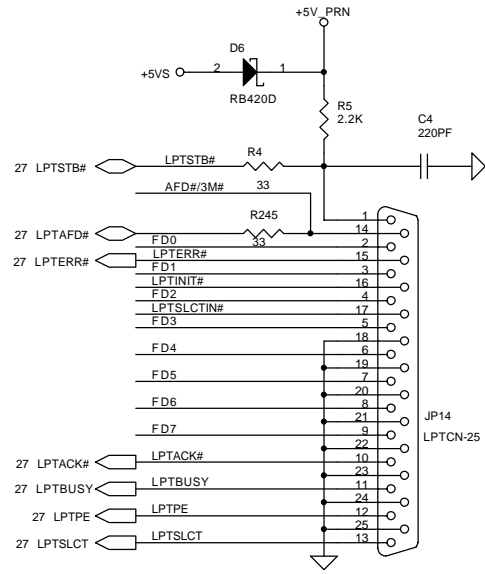
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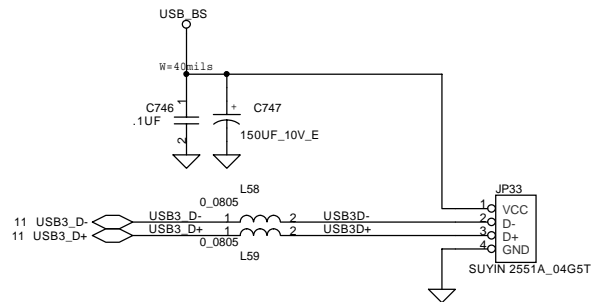
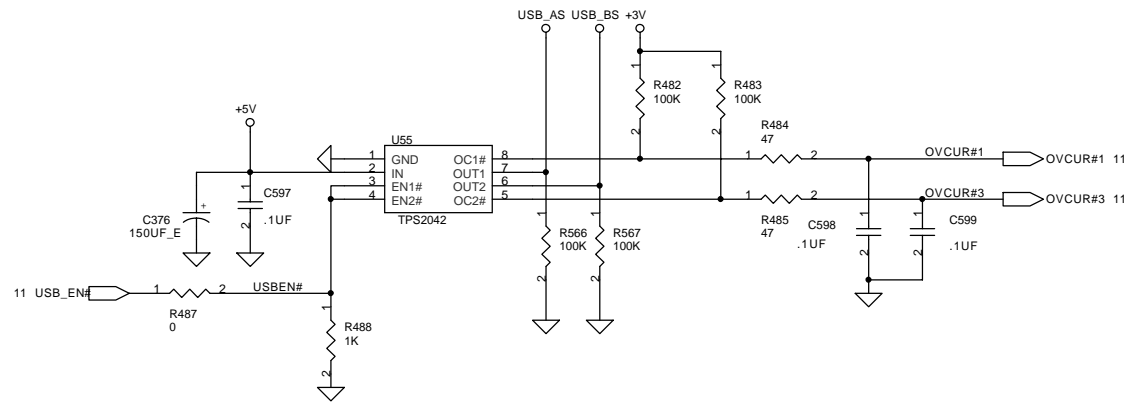
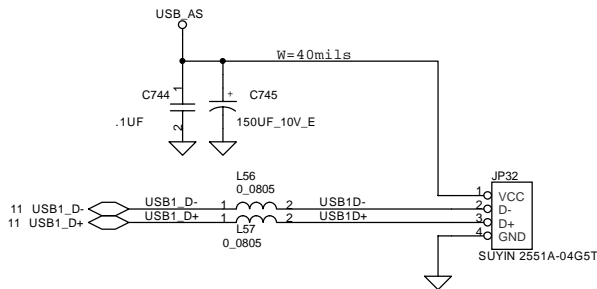
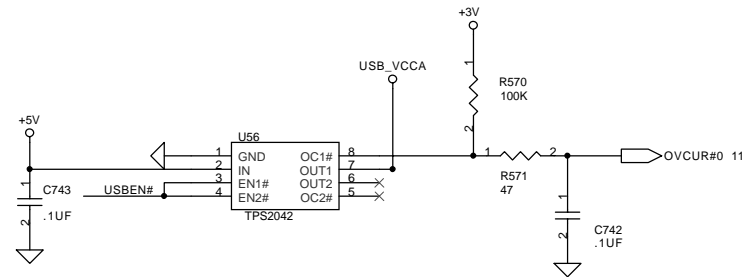
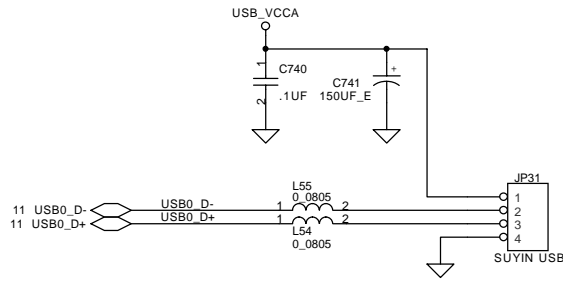


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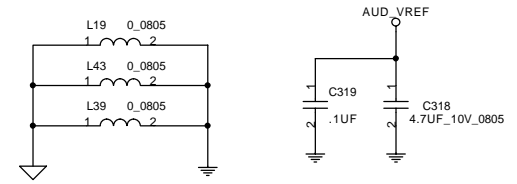
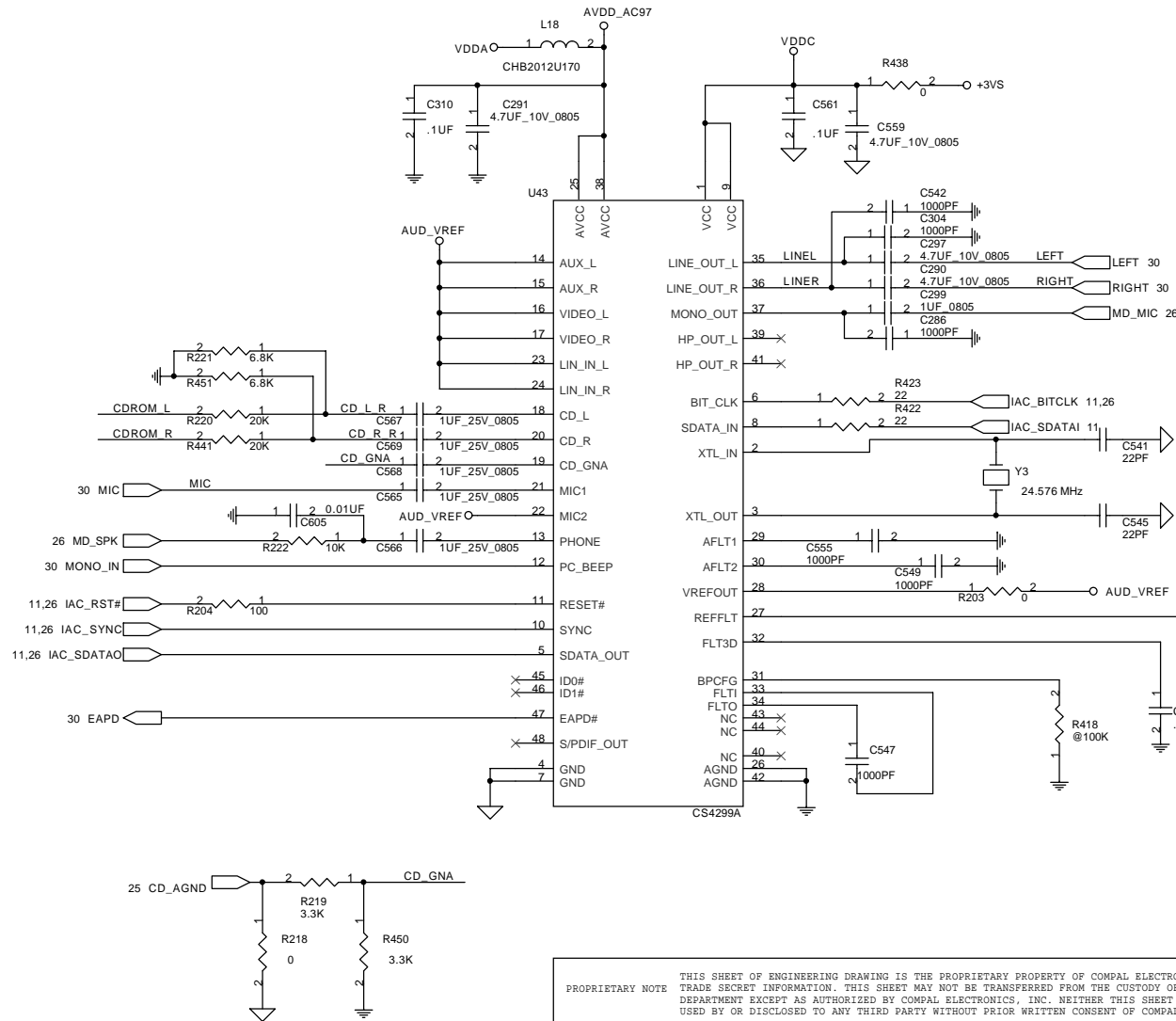
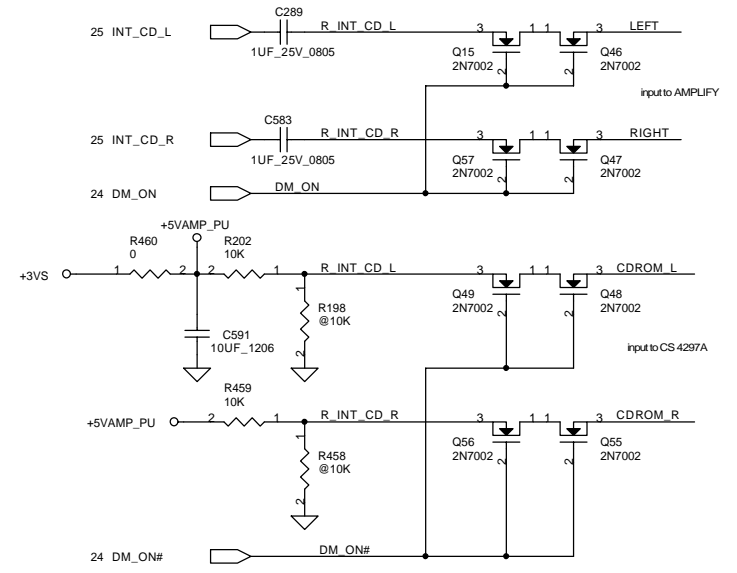
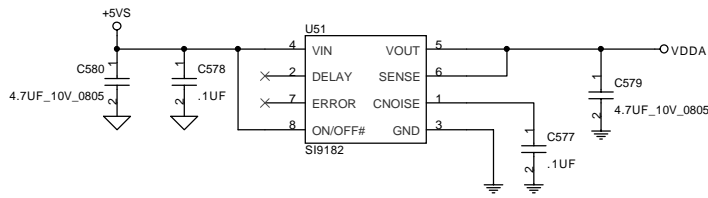
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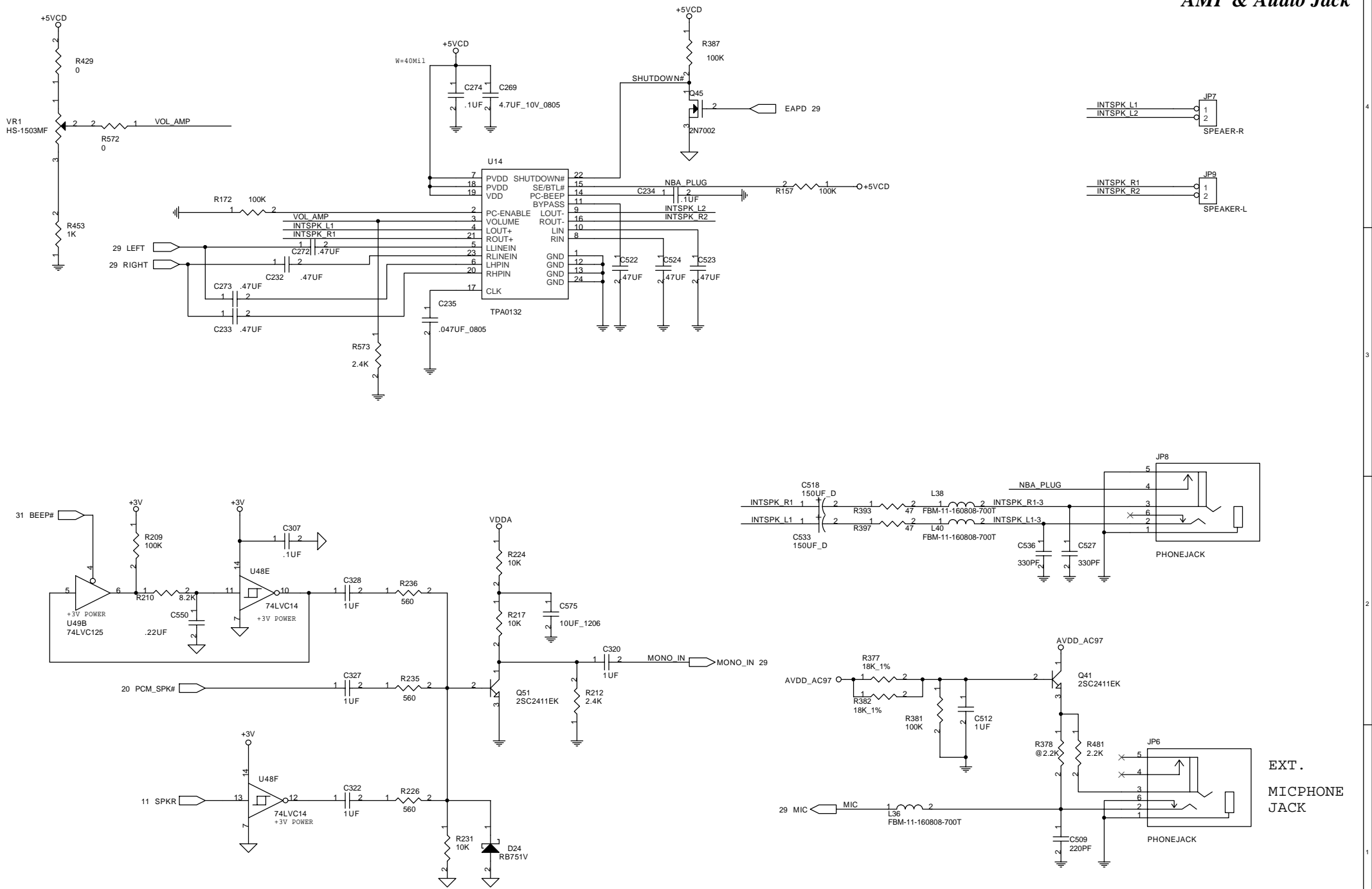
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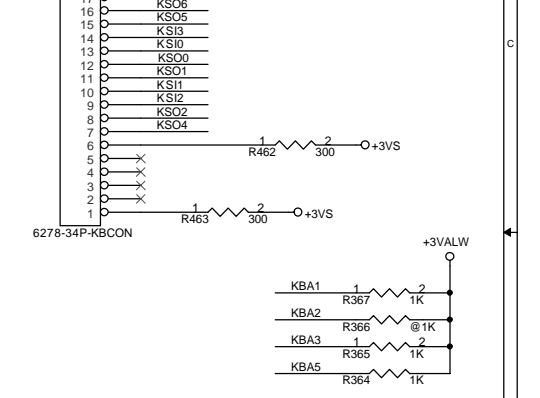
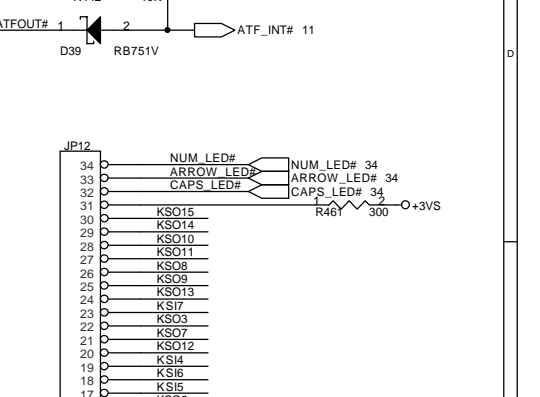
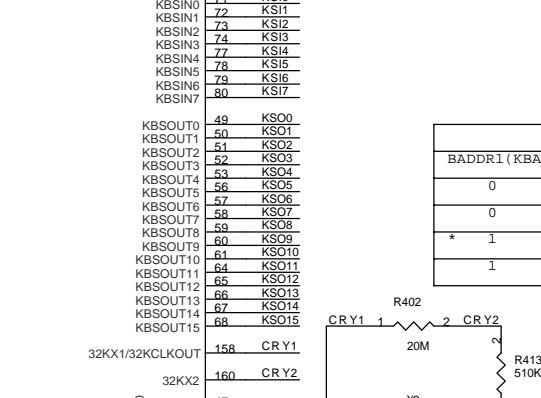
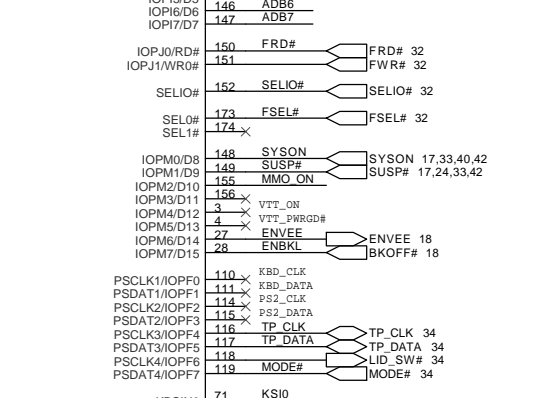
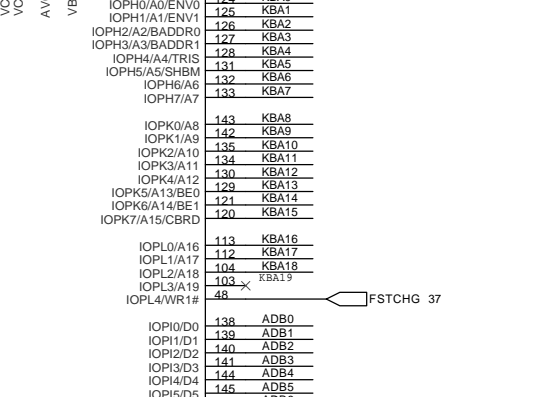
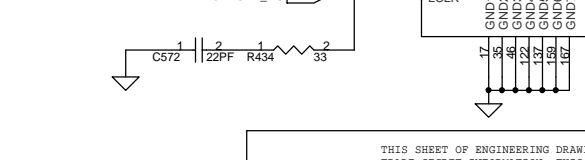
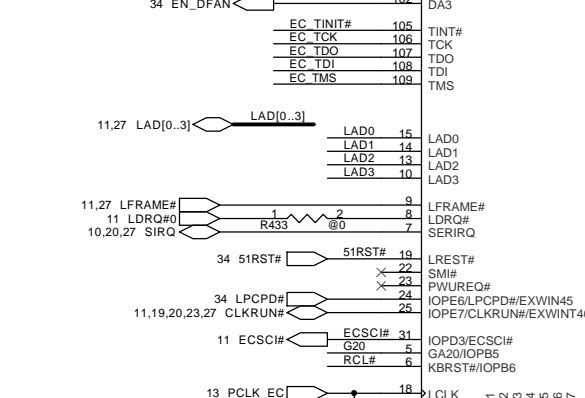
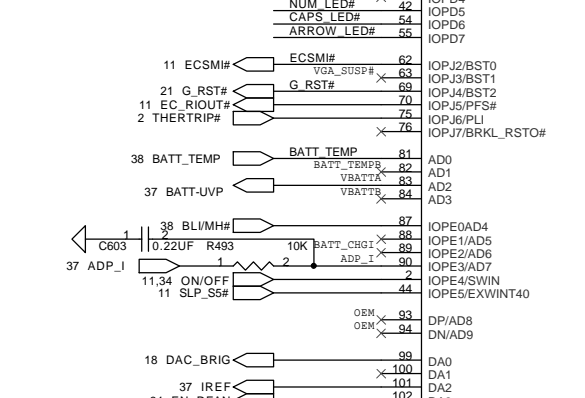
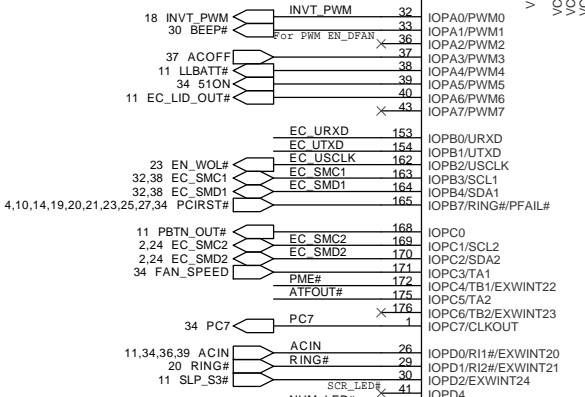
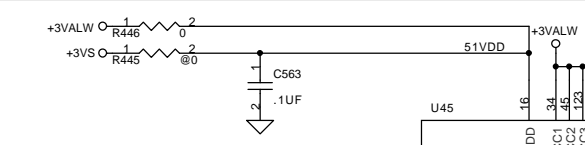
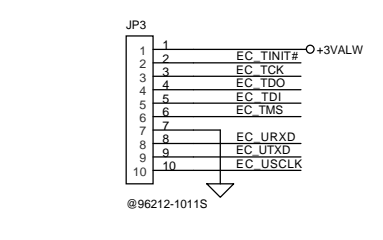
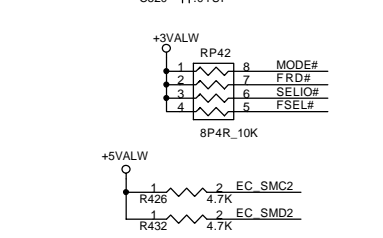
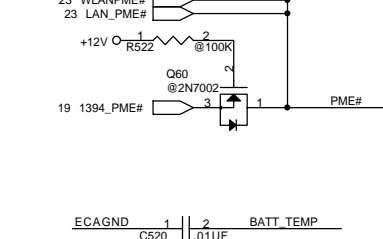
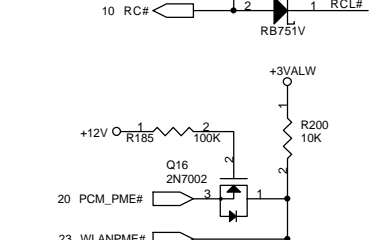
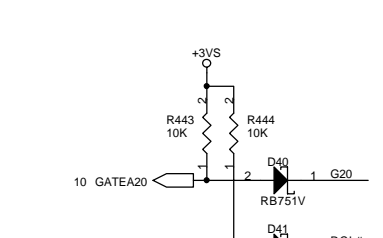
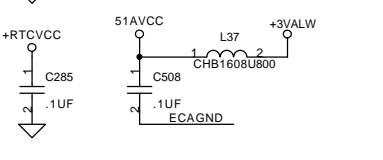
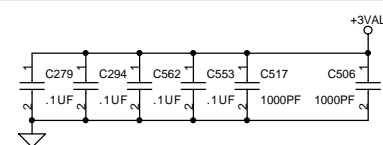
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I/O Address			
BADDR1(KBA3)	BADDR0(KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGGBAH, HCFGGBAL)+1
1	1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

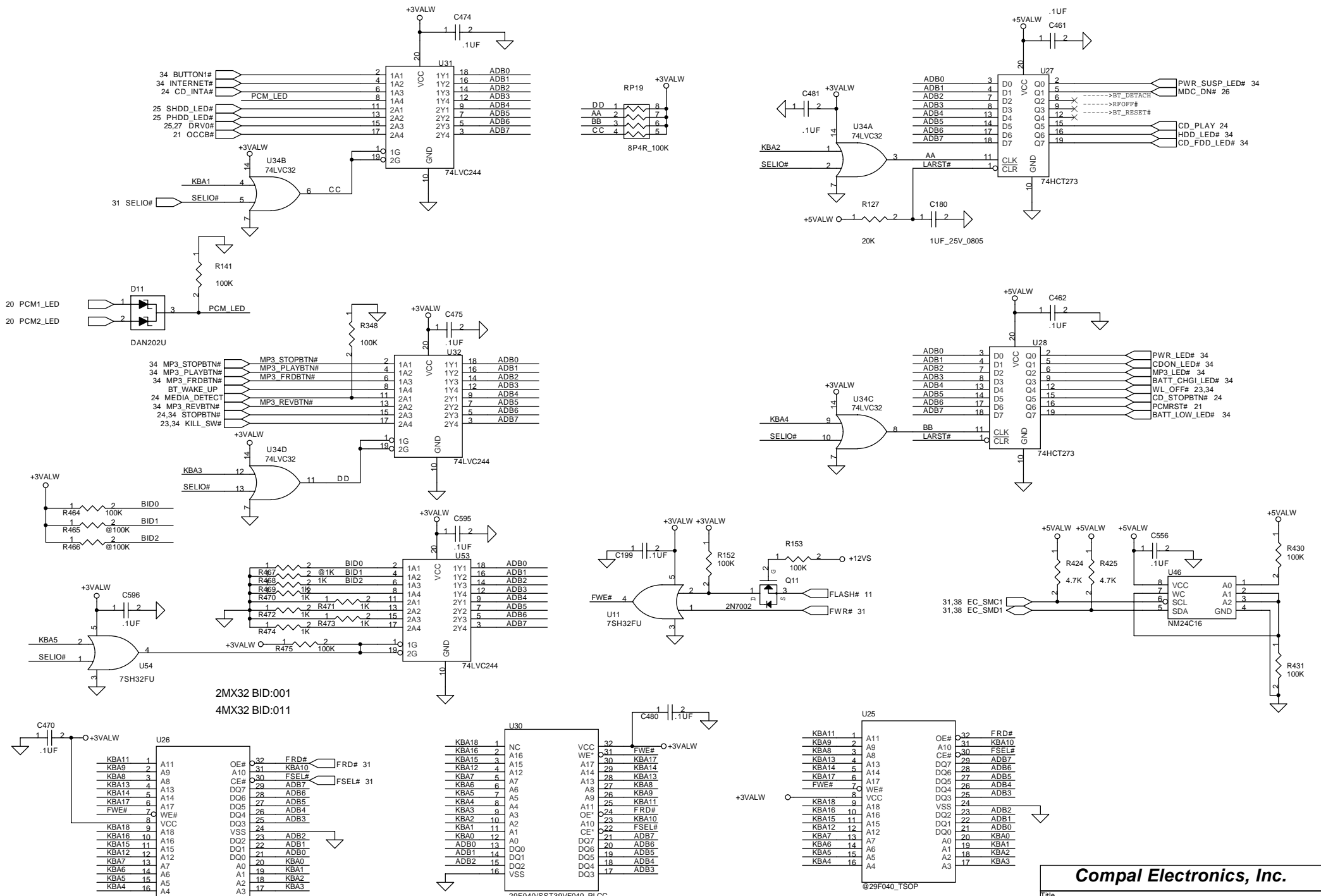
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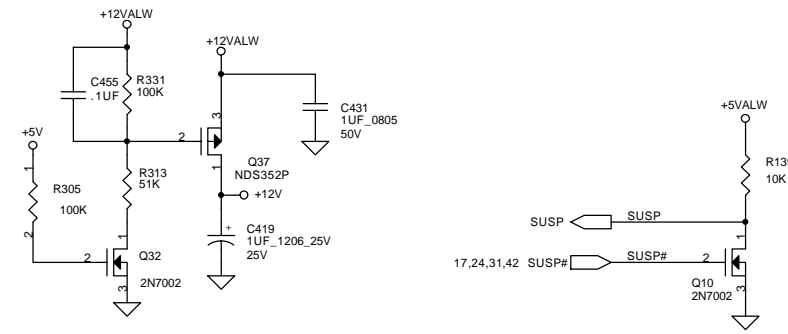
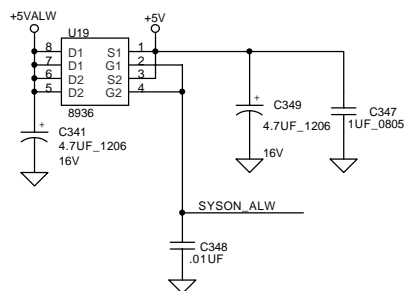
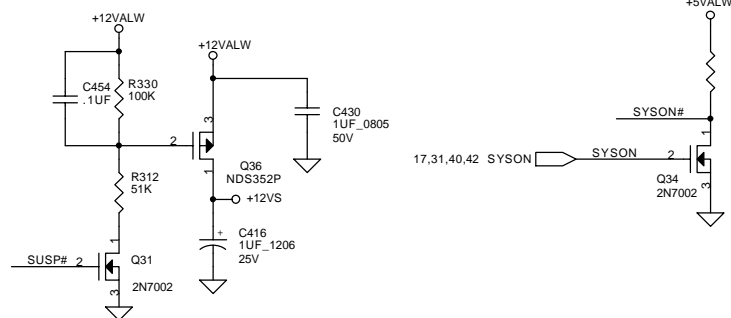
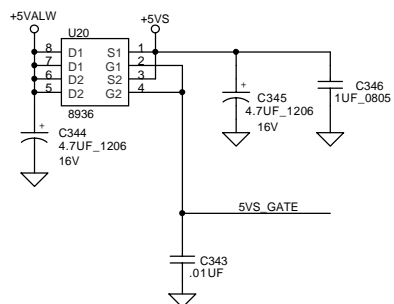
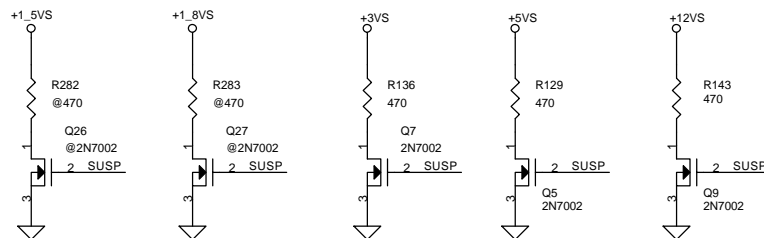
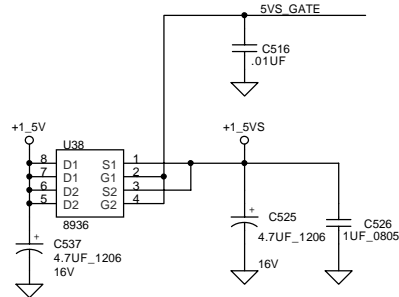
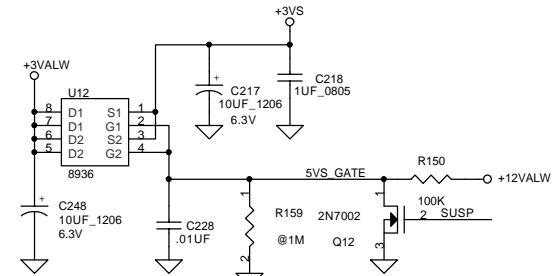
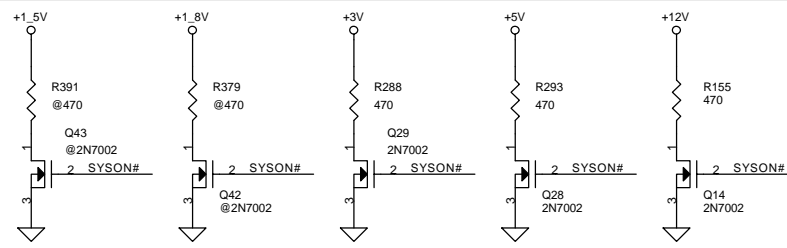
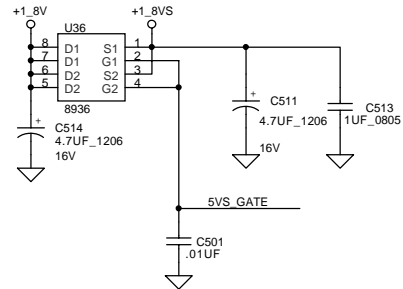
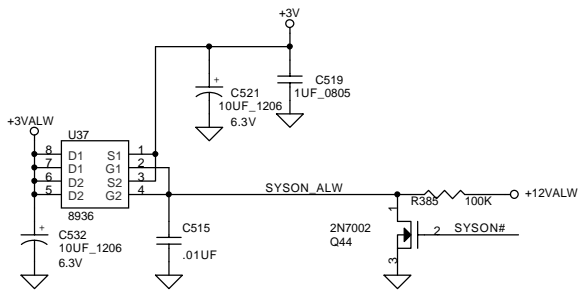
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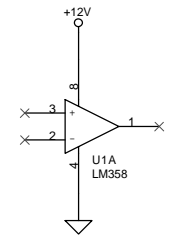
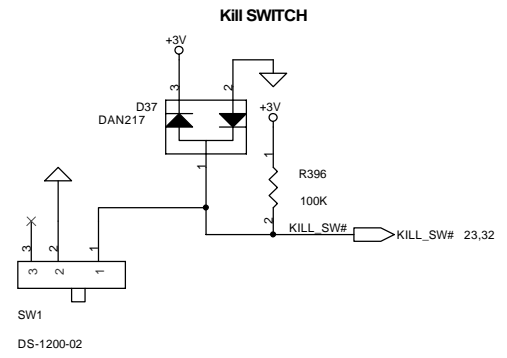
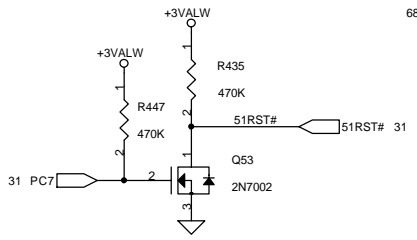
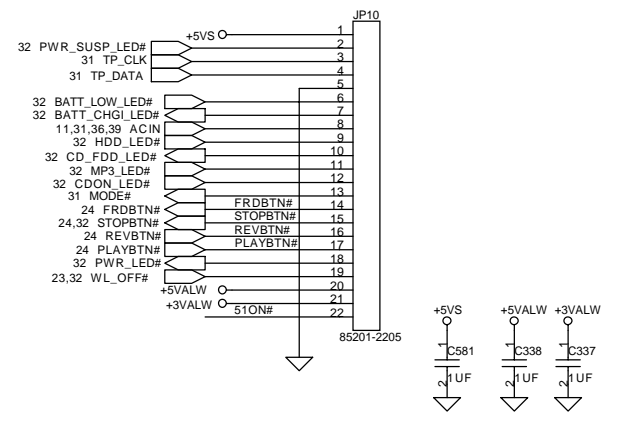
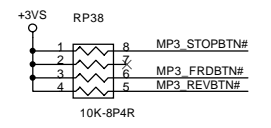
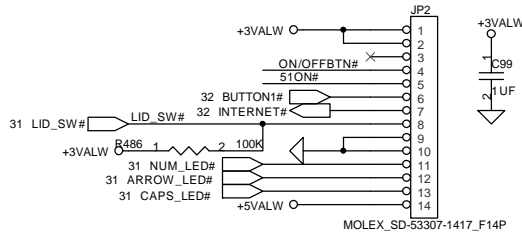
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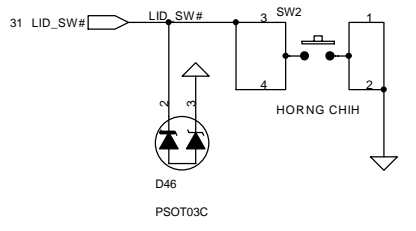
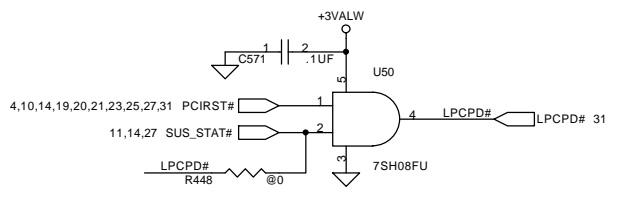
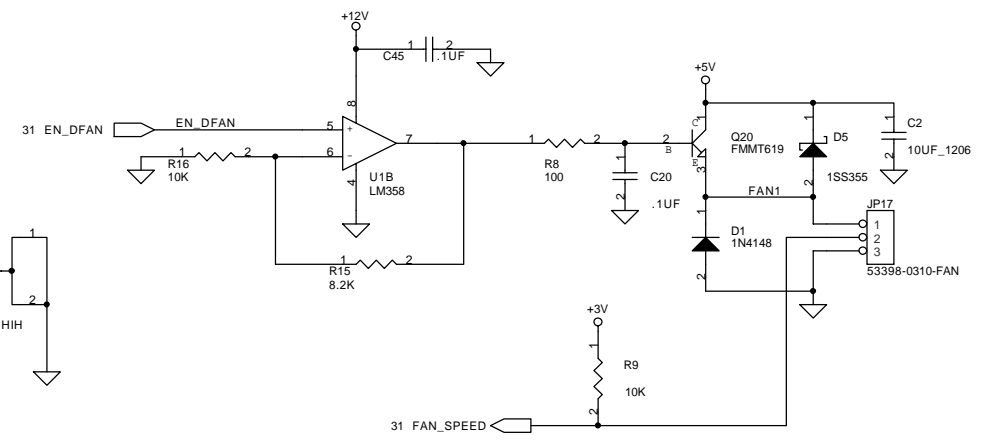
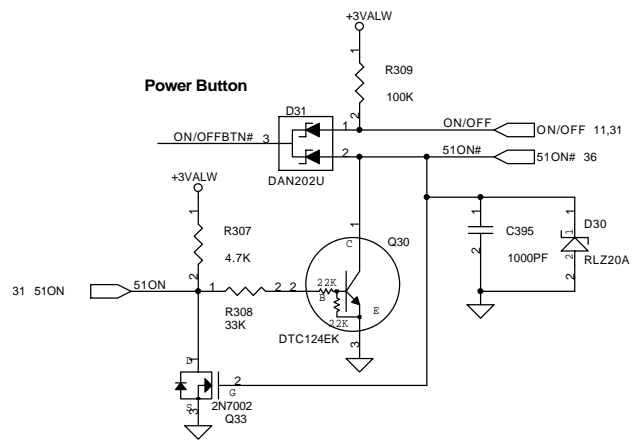


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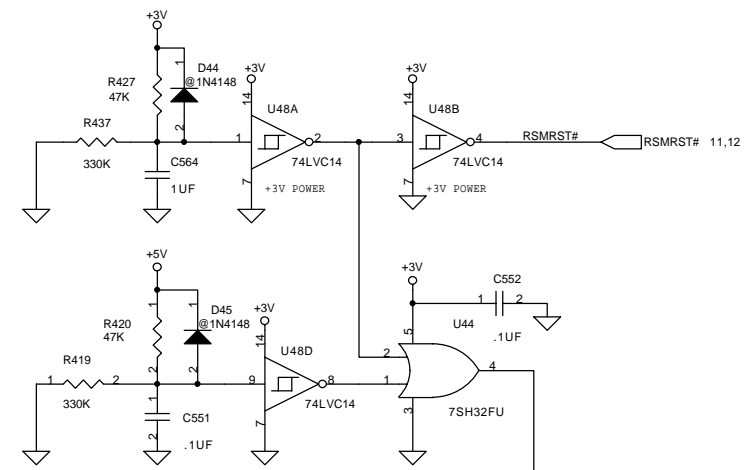
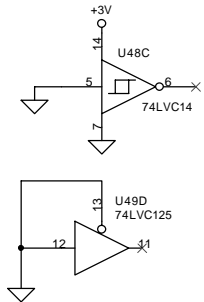
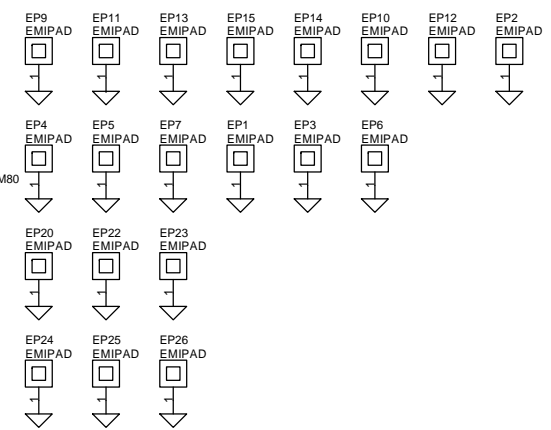
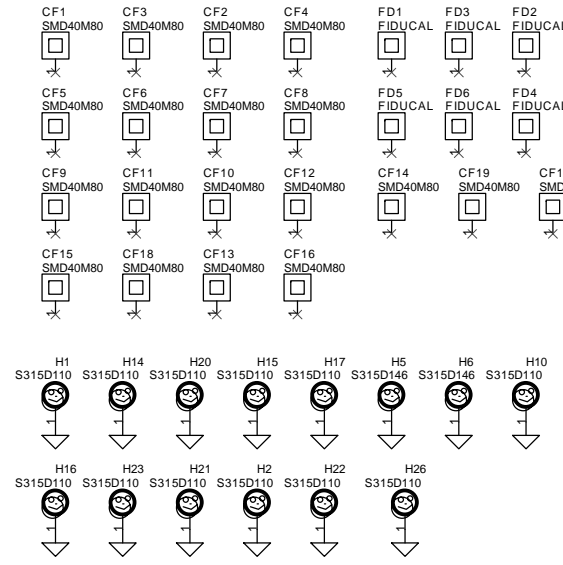
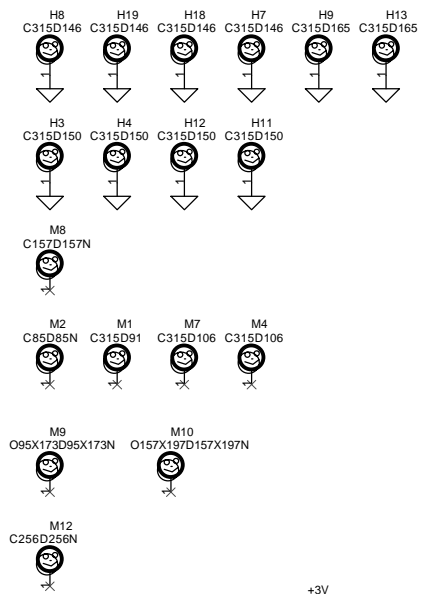


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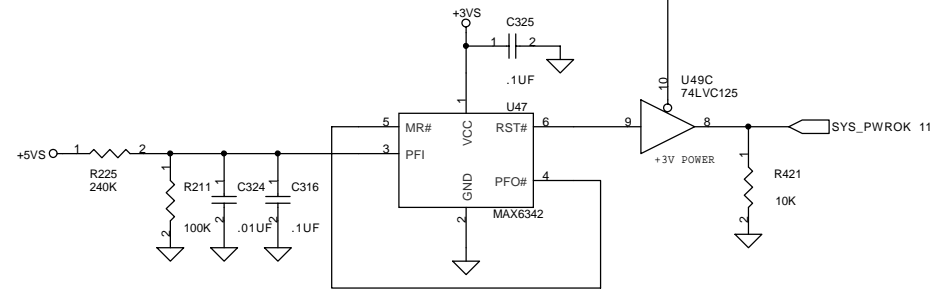
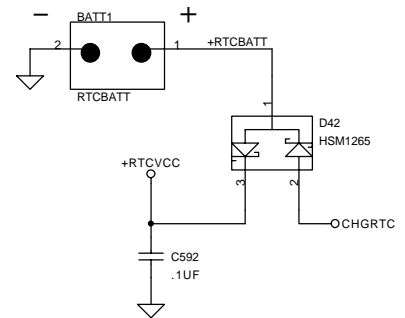
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RTC BATT

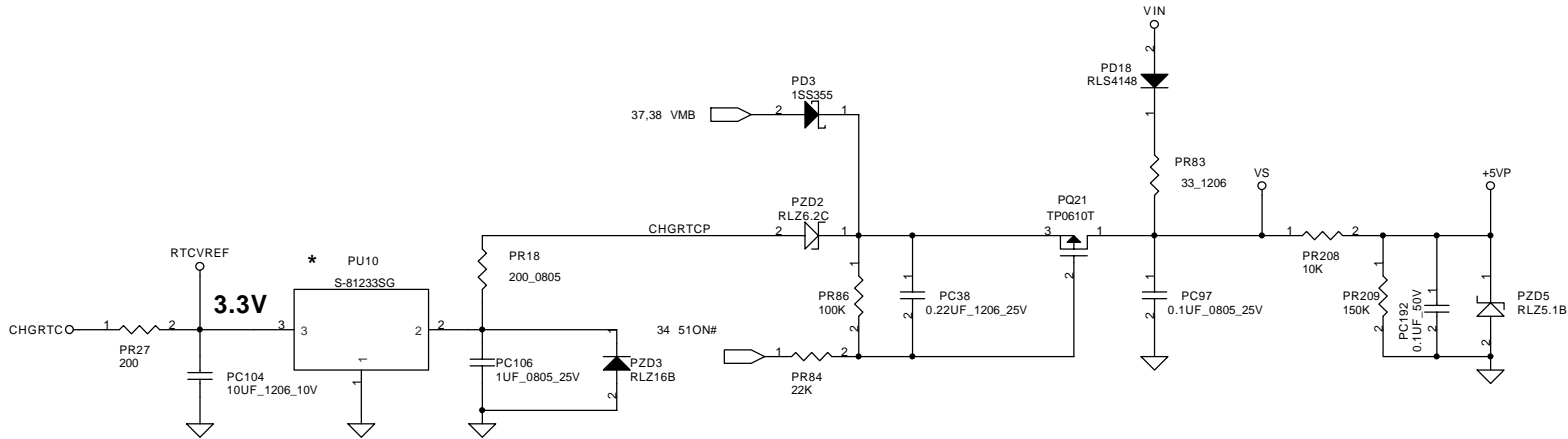
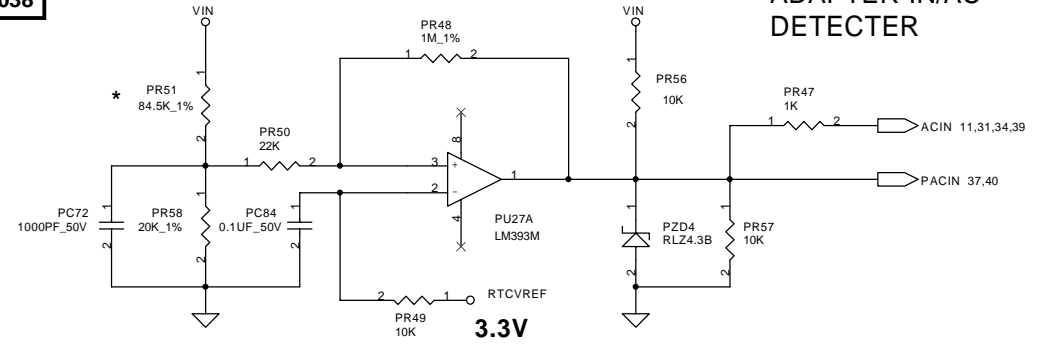
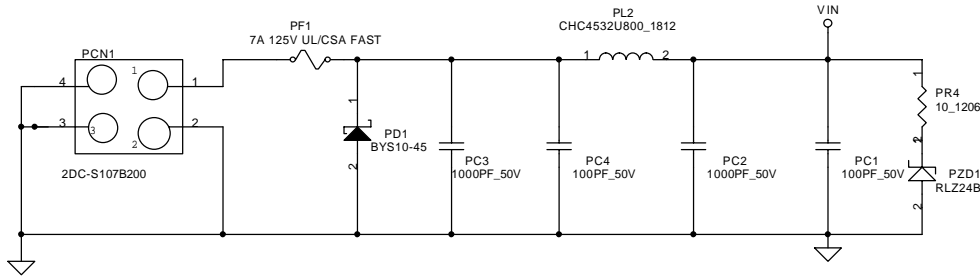


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Vin Detector

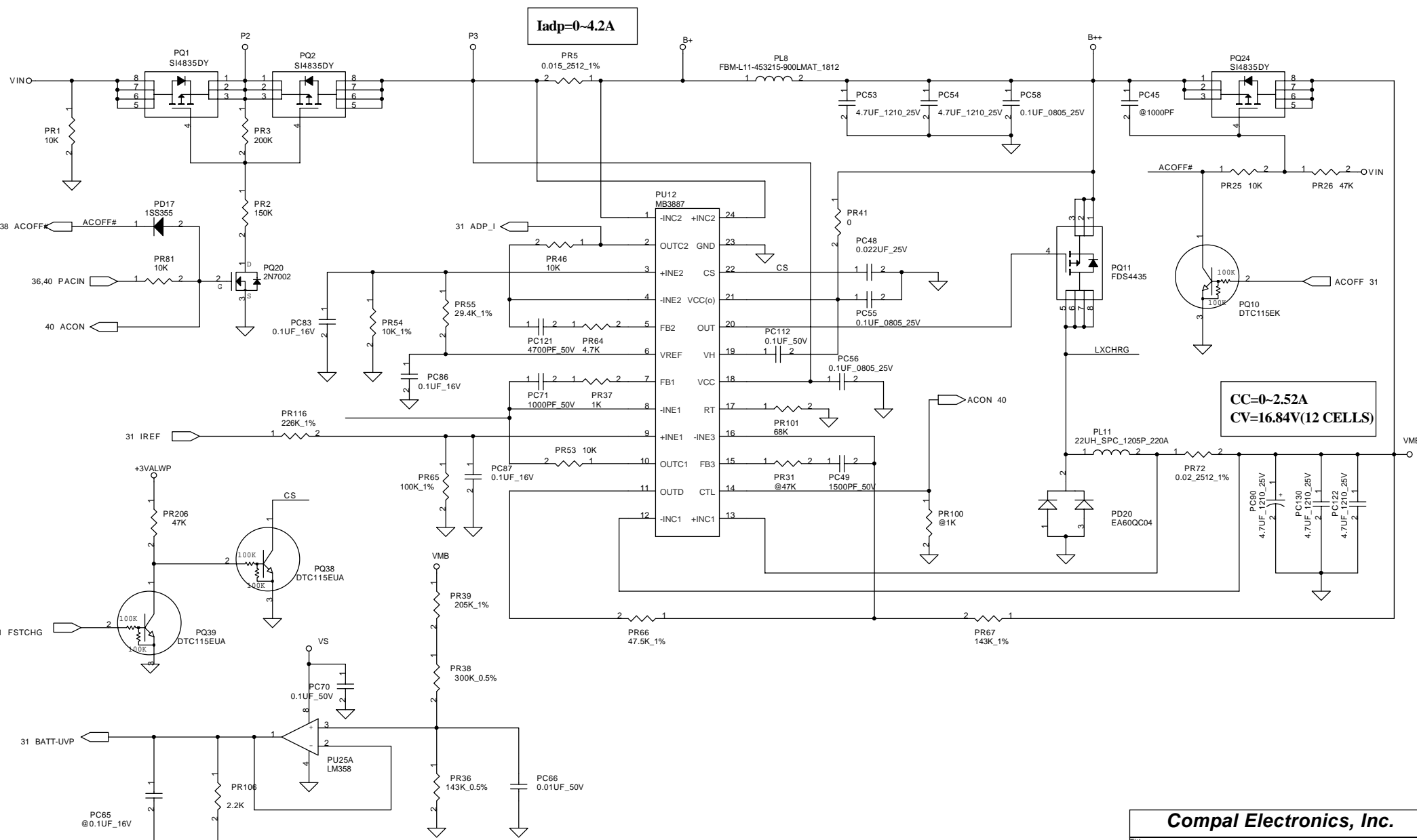
High 18.764 17.901 17.063
Low 17.745 16.903 16.038



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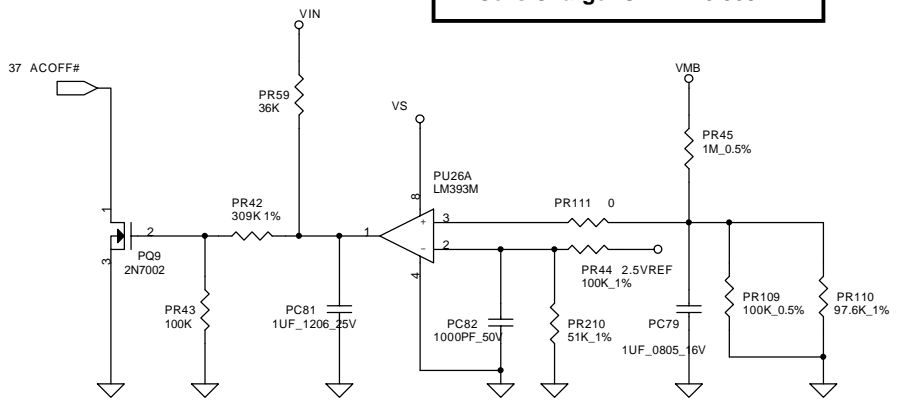
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CC=0~2.52A
CV=16.84V(12 CELLS)

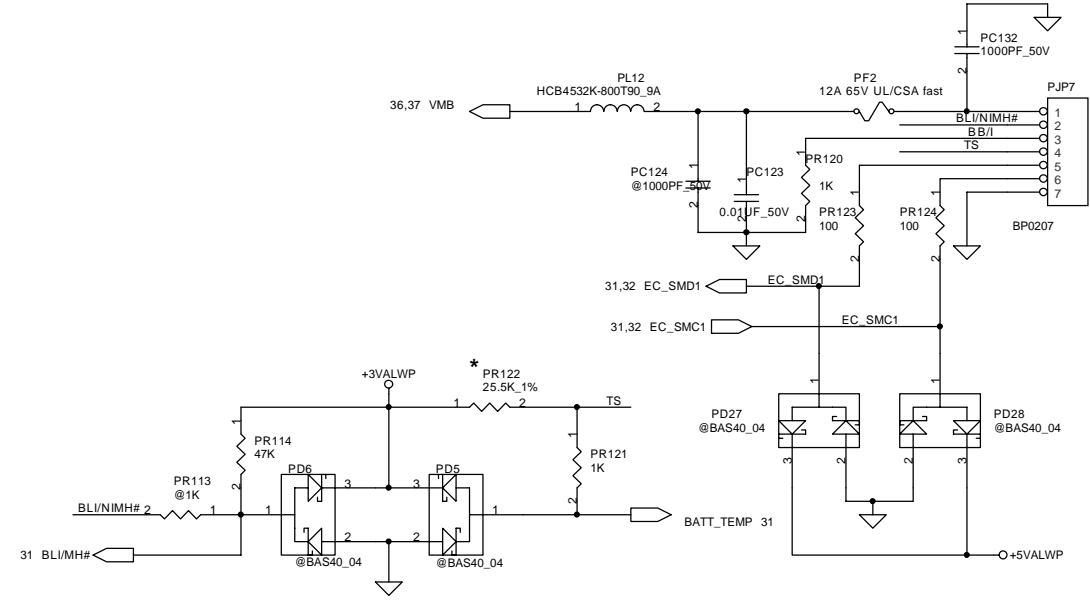
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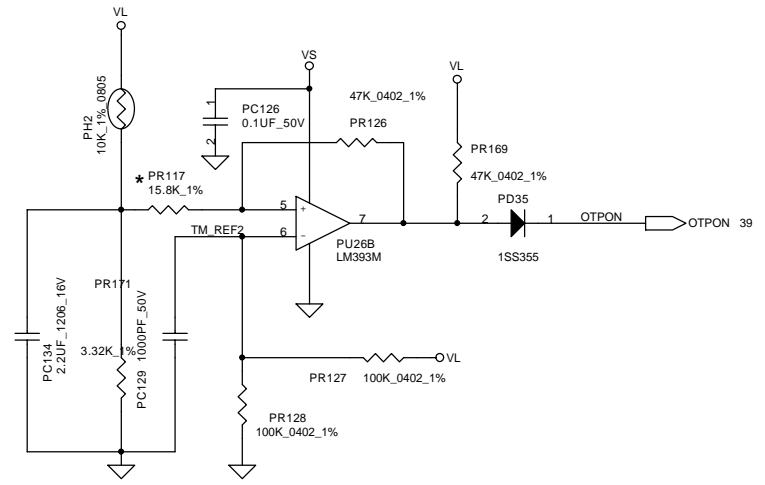
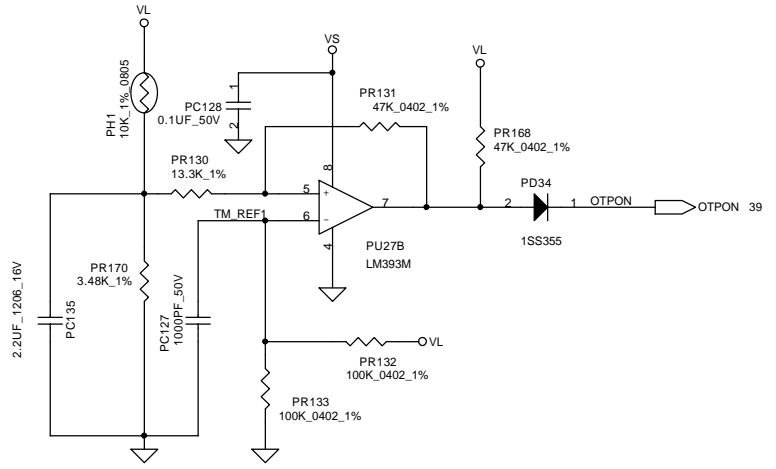
12 Cells Charger OVP : 18.059V



PH1 under CPU botten side :
 CPU thermal protection at 76 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 82 degree C
 Recovery at 45 degree C

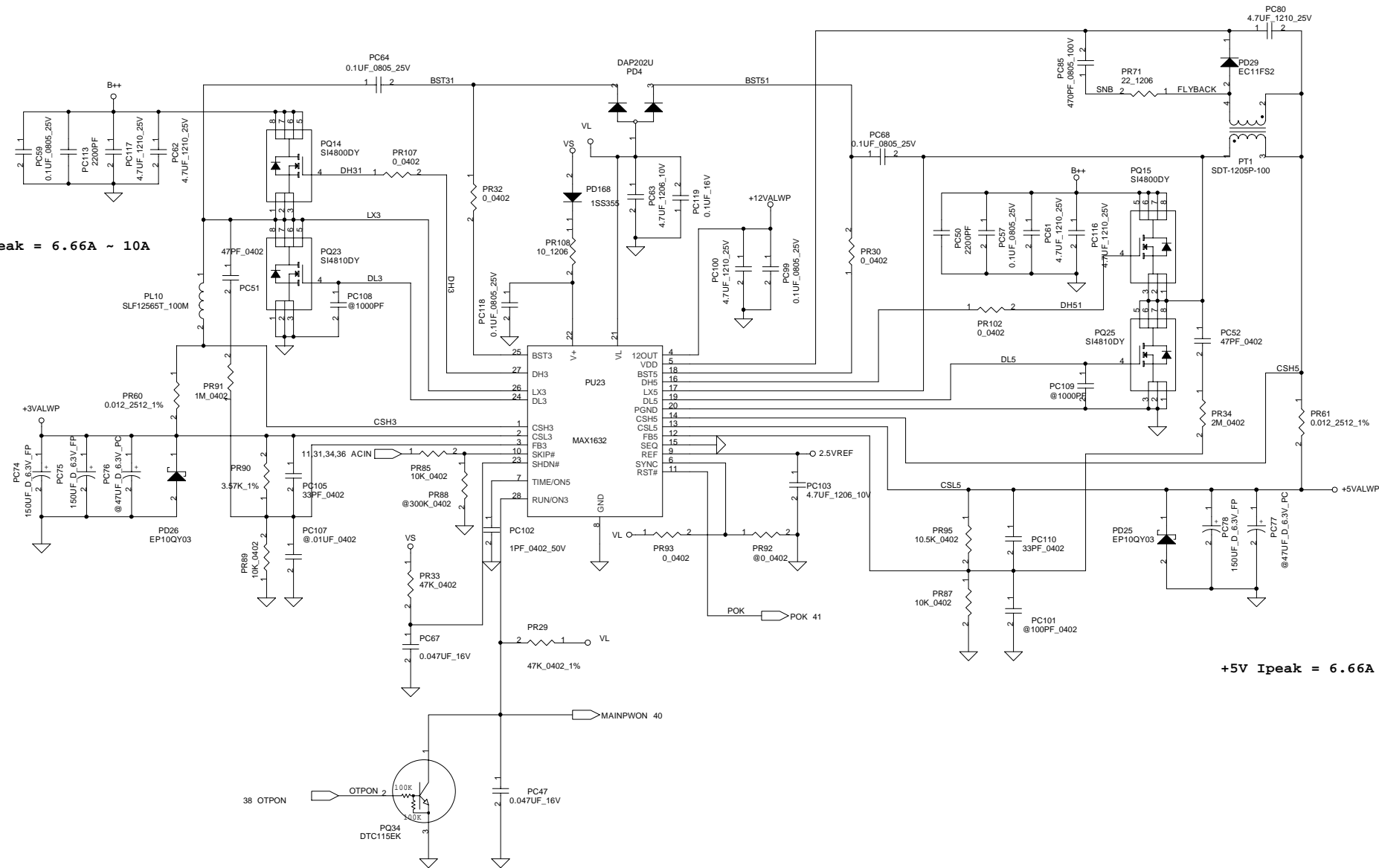


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+3.3V Ipeak = 6.66A ~ 10A

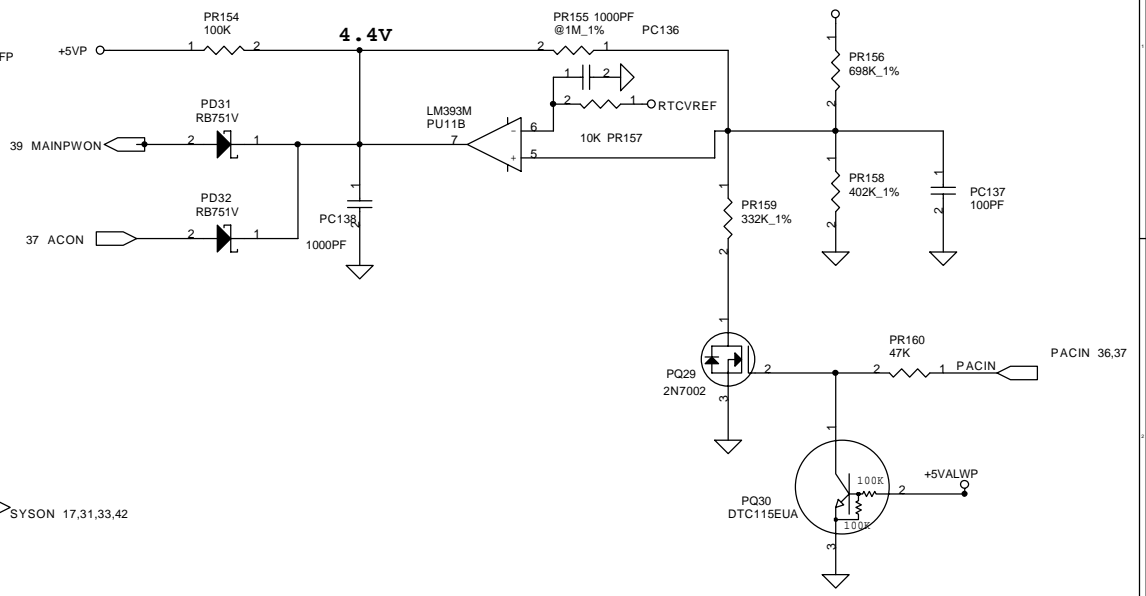
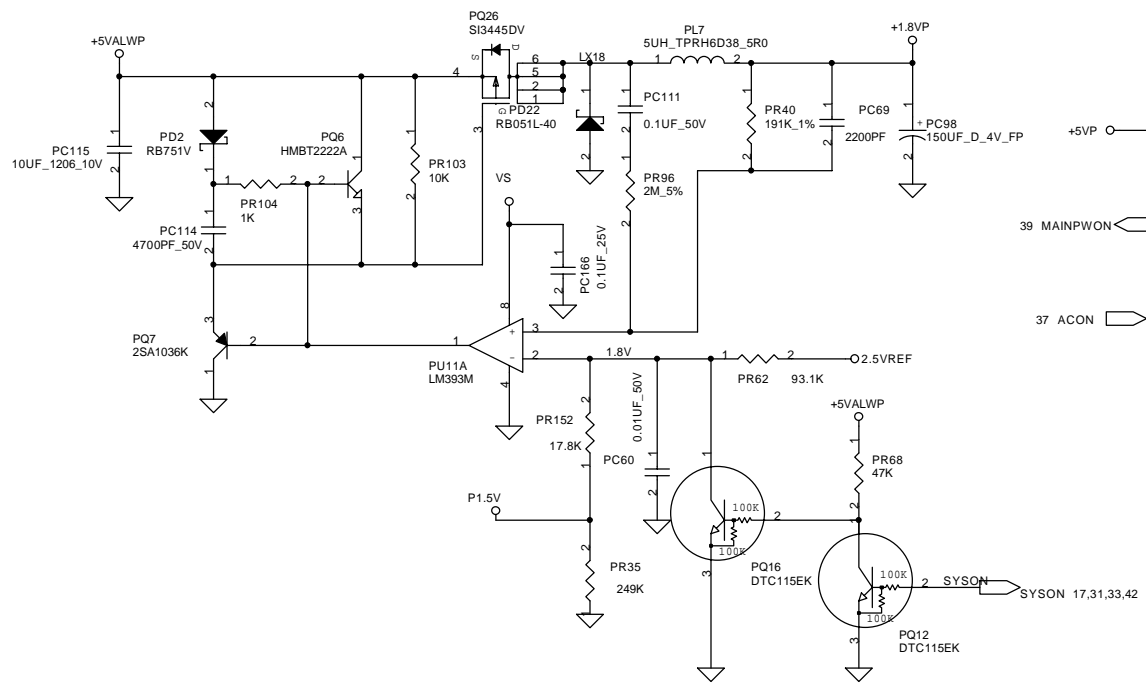
+5V Ipeak = 6.66A ~ 10A



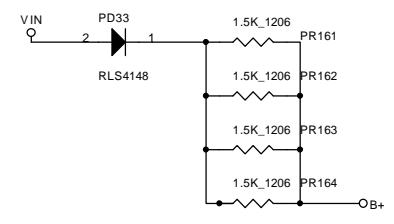
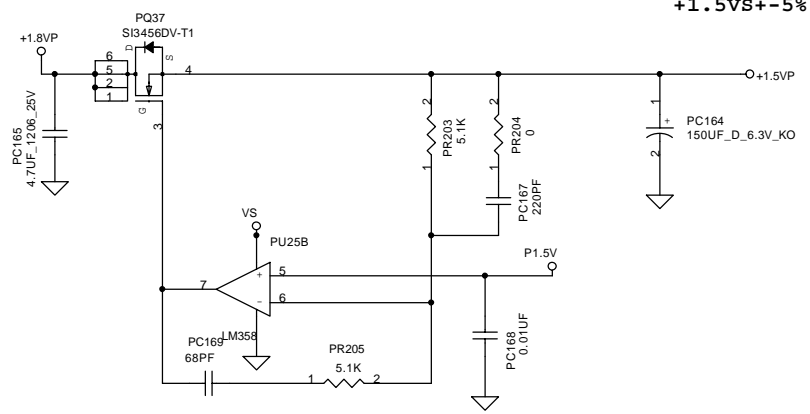
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+1.8VP+-5%

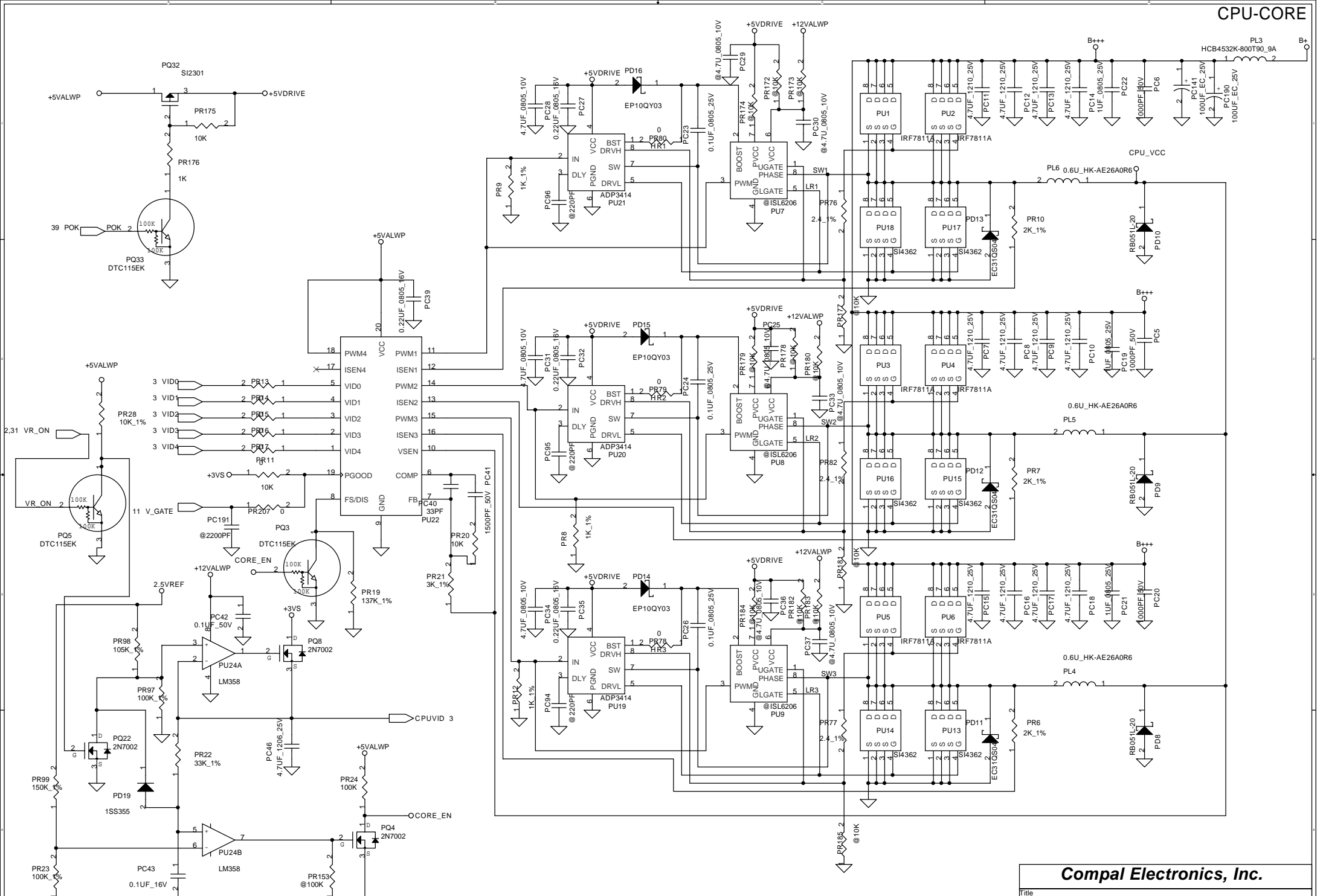


+1.5VS+-5%



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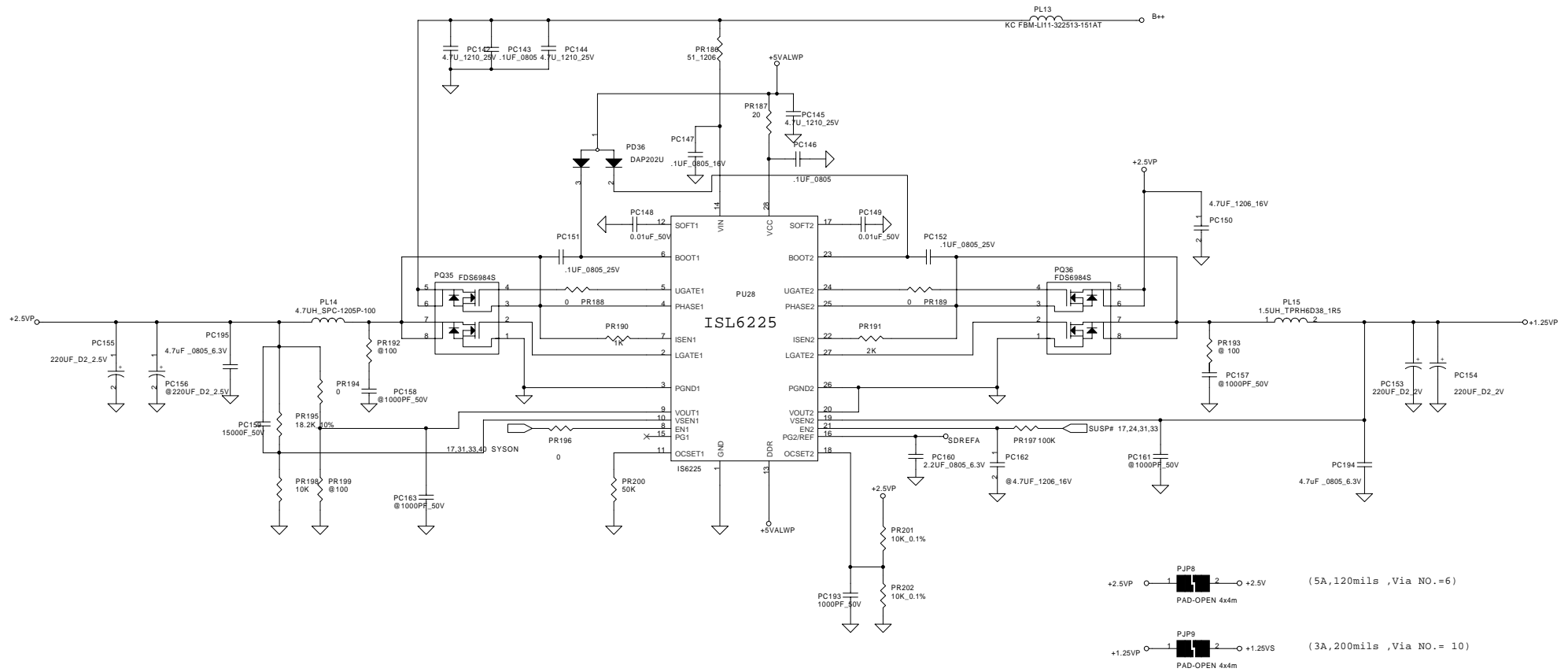
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+2.5V/+1.25V



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ATR11 PIR LIST

HW PIR LIST

PWR PIR LIST

ATEST 9/6~			
1	+2.5V LEVEL ERROR	Remove R111 100ohm Change R108 from 100 to 0 ohm	P15
2	SDRAM BANK select error	Change CLK_SDRAM3 from U22.F3 to U22.E3 Change CLK_SDRAM5 from U22.H5 to U22.G5 Change RRAS#3 from U22.H7 to U22.F7 Change RRAS#5 from U22.G6 to U22.H6	P5
3	Add CPU VCCVID pin	Add R492 connect to U23.AF3	P3
4	TV OUT output error	Change CRMA from U8.AF15 to U8.AF16 Change LUMA from U8.AF16 to U8.AF15	P12
5	Add MK1707 output terminate	Add R494 22 ohm	P12
6	Add low pass filter for MK1707 power pin	Add L47	P12
7	Change VGA option resistor to jumper	Change R284 to J3 Change R286 to J4 Change R295 to J5 Change R296 to J6	P15
8	Reserve +2.5V option control	Add R495 for SYSON control Add R496 for SUSP control	P15
9	Change LCD connector type	Change JP1	P16
10	Add TI TPS2042 for USB protect cicuit	Add U56(TPS2042)	P25

BTEST			

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		Creat +5VP power		36	Add PC192: 0.1UF; PZD5: RLZ5.1B PR208: 10K; PR209: 150K		DVT
2		Meet spec. of ISL6225 DDR2.5V Vsense voltage 0.89V		42	Change PR195 from 17.8K to 18.2K		DVT
3		For CP mode		37	Change PR64 from 10K to 4.7K PC121 from 4700PF to 1000PF		DVT
4		For DDR 1.25V ripple voltage		42	Change PC153, PC154 from 150uF/6.3V to 220uF/2V		DVT
5		For DDR 2.5V voltage		42	Add PC156: 220uF/2V; delete PC155: 220uF/2V		DVT
6		For cost downe		42 40	Change PL15 from 1.5uH SPC_06703 to 1.5UH TPRH6D38 Change PL7 from 5uH SPC_06703 to 5UH TPRH6D38		DVT
7		For DDR 1.25V voltage sense		42	Change PR191 from 6.8K_1% to 2K_1%		DVT
8		For transient response of DDR 2.5V 1.25V		42	Add PC195 PC194 4.7uF/6.3V; de-pop PC153 Change PC193 from 1000pF to 4700pF; PR186 from 10 to 51Ohm		PVT
9		For reduce CP mode noise		37	Change PC121 from 4700PF to 1000PF		PVT
10		Increase voltage margin on CTL of MB1887		37	.De-pop PR100		PVT
11		Change 1.8V to 1.85V P1.5V to 1.73V requested from H/W		40	Change PR62 from 100K to 93.1K PR152 from 43K to 17.8K PR35 from 215K to 249K		PVT

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